First Demonstration of Monolithic Silicon Photonic Integrated Circuit 32×32 Thin-CLOS AWGR for All-to-All Interconnections

First Demonstration of Monolithic Silicon Photonic Integrated Circuit 32x32 Thin-CLOS AWGR for All-to-All Interconnections

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Abstract *We designed, fabricated, and demonstrated the first monolithic silicon photonic Thin-CLOS AWGR. The fabricated Thin-CLOS has 32 ports and four 16-port silicon nitride AWGRs integrated by compact multilayer waveguide routing. Experimental results show 4 dB insertion loss and -20 dB crosstalk.*

Introduction

Next generation data centers and future high performance computing (HPC) applications could benefit significantly from scalable, low latency, and energy-efficient optical interconnects. The arrayed waveguide grating router (AWGR) has become a core component of many proposed optical interconnect architectures for data centers and HPC by virtue of AWGR's intrinsic wavelength routing capability (Fig. 1 (c)). By utilizing wavelength division multiplexing (WDM) technology, AWGR provides strictly nonblocking all-to-all interconnection with significantly lower complexity, as shown in Fig 1 (a) and (b). However, interconnection systems with a single AWGR have limited scalability. Large port-count AWGRs experience significant in-band crosstalk, extremely dense channel spacing, and difficulties in fabrication.

The Thin-CLOS architecture was proposed to increase the scalability of AWGR based wavelength routing interconnect systems[1]. As shown in Fig 1 (d), by using M groups of M AWGRs with W ports, the Thin-CLOS architecture increases the scalability of a single W-port AWGR by a factor of M, and thus resembles the functionality of a $N \times N$ AWGR, where $N = M \times W$. The Thin-CLOS system has been experimentally demonstrated by packing multiple discrete commercial AWGRs and fibers into a 1U rack unit[2]. However, the architecture has never been demonstrated on a silicon photonic (SiPh) platform. State-of-the-art crosstalk values of SiPh AWGR are not low enough for a single AWGR to scale beyond 16 ports. It would be desirable to make scalable monolithic Thin-CLOS AWGR so that SiPh AWGR based systems[3],[4] can be deployed at large scale.

In this paper, we designed, fabricated and demonstrated a 32-port monolithic SiPh Thin-CLOS AWGR consists of four 16-port AWGRs

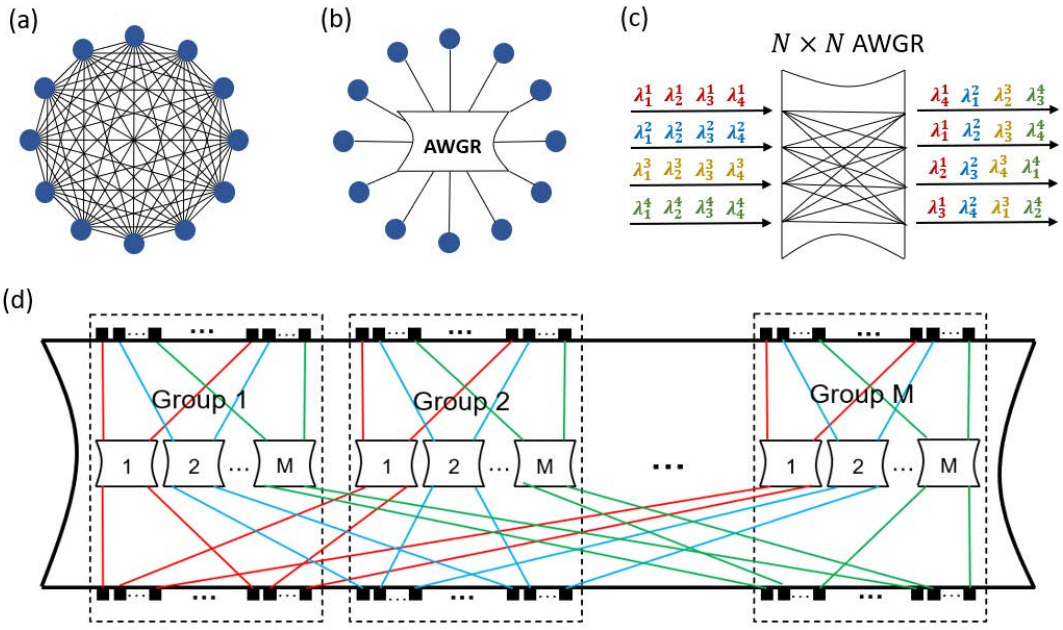

Fig. 1: All-to-all communication based on (a) direct fiber connection and (b) AWGR. (c) AWGR wavelength routing functionality, where λ_i^j represents the light with wavelength λ_i incident at input port j. (d) *N*-port Thin-CLOS AWGR architecture by using *M* groups of *M* AWGRs with *W*-port, being *N*=*M* x *W*.

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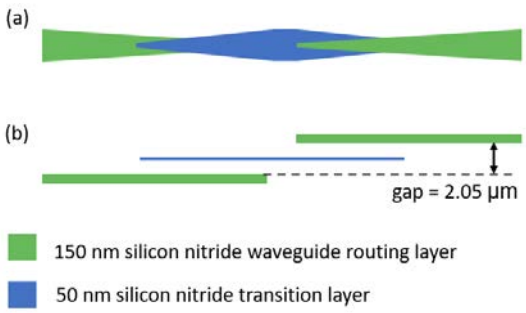

Fig. 2: Tri-layer inverse taper based low-loss vertical couplers. (a) top view, (b) side view.

($W = 16,\ M = 2,\ N = 32$, 64 input waveguides, 64 output waveguides) on a multilayer silicon nitride platform[5],[6]. The measurement result shows 4.0 dB insertion loss and -20 dB in-band crosstalk of the fabricated device when working at C-band. Our proposed on-chip Thin-CLOS solution also shows scalability to larger port-count.

Chip Design

A $N = M \times W$ Thin-CLOS system consists of M^2 AWGRs and $2 \times M^2 \times W$ fiber connections, which translates into $2 \times M^2 \times W$ routing waveguides for a monolithic Thin-CLOS. To make sure the device is scalable and compact even with a large number of routing waveguides, we used five layers of silicon nitride, where layer 1, layer 3, and layer 5 are 150 nm silicon nitride for routing waveguides. Layer 2 and layer 4 are 50 nm silicon nitride for transition waveguides. The existence of transition waveguide doubled the interlayer gap between routing layers (layer 1, 3, and 5) for low crosstalk while preserving high interlayer coupling efficiency. Light coupling between the routing layers is enabled by a tri-layer inverse taper based low-loss vertical coupler[5], as shown in Fig. 2 (a). The coupling loss is estimated at 0.023 dB based on Lumerical FDTD simulations. Thanks to the 50 nm transition layer, the routing layer gap increases to 2.05 μm, which significantly reduced the insertion loss and crosstalk from interlayer waveguide crossing. FDTD simulations show 0.004 dB insertion loss and -49 dB crosstalk per crossing.

In order to make a full use of the 5-layer silicon nitride platform to improve the scalability and reduce the device footprint, we designed a multilayer waveguide routing strategy that is customized for on-chip Thin-CLOS. By making use of three layers of 150 nm silicon nitride, where routing waveguides on each layer have distinct directions, the routing strategy guarantees no intralayer waveguide crossing and reduces the device footprint. The minimum bending radius is chosen to be 150 μm for low bending loss. All the small AWGRs are located on the bottom layer to avoid any possible performance degradation due to nonuniformity of optical thickness or stress across multilayers.

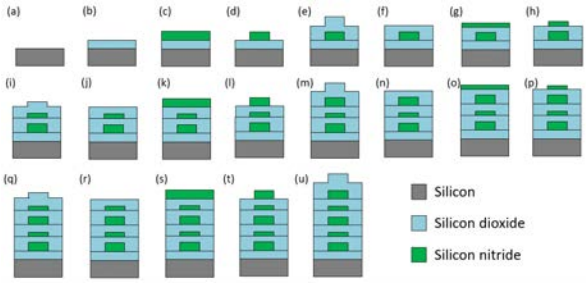

Fig. 3: Fabrication process flow charts

With the multilayer technology mentioned above, we designed a 32-port on-chip Thin-CLOS AWGR composed of four 16-port AWGRs ($W = 16, M = 2, N = 32$). The 16-port AWGR was designed on 150 nm silicon nitride with 1550 nm center wavelength and 200 GHz channel spacing.

Fabrication

We fabricated the SiPh wafer using ASML DUV Stepper Model 5500/300 lithography technology. The fabrication process flow is shown in Fig. 3. (a)-(u). The bottom oxide cladding layer is Low-emperature Oxide (LTO) deposited on 150 mm silicon wafers by Low-Pressure Chemical Vapor Deposition (LPCVD). For all the five waveguide layers we used 800 °C LPCVD silicon nitride and Inductively Coupled Plasma (ICP) etching. LTO was used for interlayer cladding, which was planarized by Chemical Mechanical Polishing (CMP). The top cladding layer is 4 μm LTO. Fig 4. shows the fabricated 32-port Thin-CLOS AWGR.

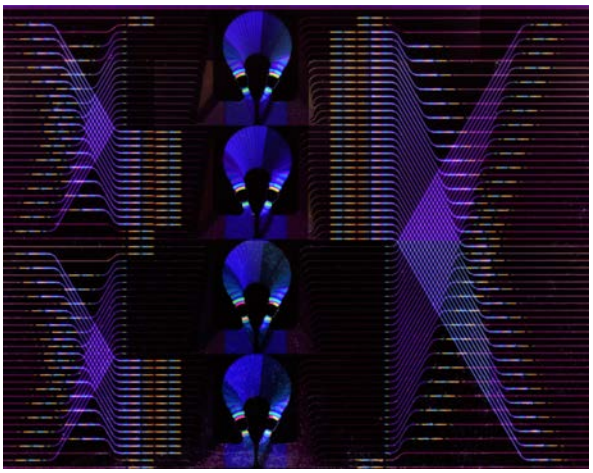

Fig. 4: Fabricated 32-Port Thin-CLOS AWGR. The image is a mosaic of 9 smaller images captured by microscope.

Measurement results

We measured the fabricated devices using an Optical Spectrum Analyser (OSA) with single mode lensed fibers for edge coupling. The coupling loss between on-chip edge coupler and lensed fiber is characterized to be 1.1 dB per facet. As in Fig. 5 (a), at 1550 nm, the straight waveguide insertion loss (fiber edge coupling loss + waveguide propagation loss) for layer 1 is 2.5 dB, which translates to 0.4 dB/cm waveguide propagation loss. The characterized vertical coupling loss is < 0.2 dB per coupler.

For the upper layers, the waveguide insertion loss increased to 4.4 dB for layer 3, and 5.1 dB for layer 5 as in Fig. 5 (a). The extra waveguide propagation loss is 1.9 dB for layer 3, and 2.6 dB for layer 5. Thermal annealing could significantly reduce the waveguide propagation loss on the upper layers. However, annealing was not conducted on the fabricated devices presented in this paper.

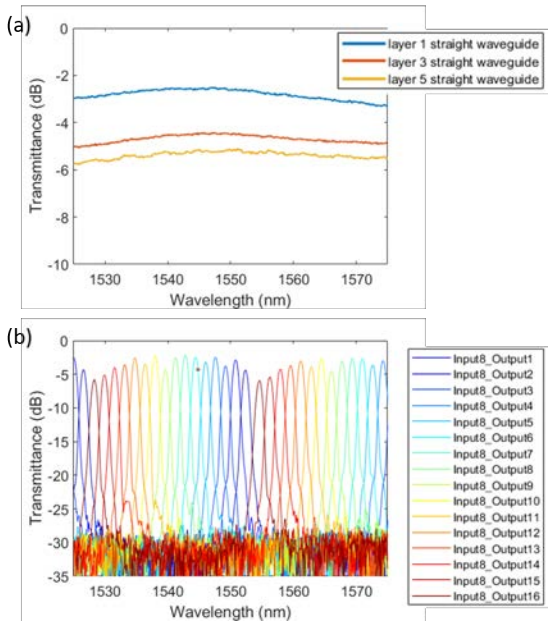

Fig. 5: Measured transmittance of (a) straight waveguides and (b) 16-port silicon nitride AWGR

Fig 5. (b) shows the measrued and calibrated spectrum of a single 16-port AWGR. The measured insertion loss is 2.1 dB (w ith upto 3 dB spectral roll-off) and the channel spacing is 200.6 GHz, which is increased by 0.3% from the designed value. The crosstalk is less than -25 dB.

Fig 6 (a)-(d) shows the measured spectrum of the 32-port Thin-CLOS AWGR with four different input ports. The measurement shows 4.0 dB insertion loss with crosstalk values < -20 dB. The extra insertion loss of the Thin-CLOS AWGR comes from the upper layer waveguide propagation losses, which can be reduced by thermal annealing in our future work.

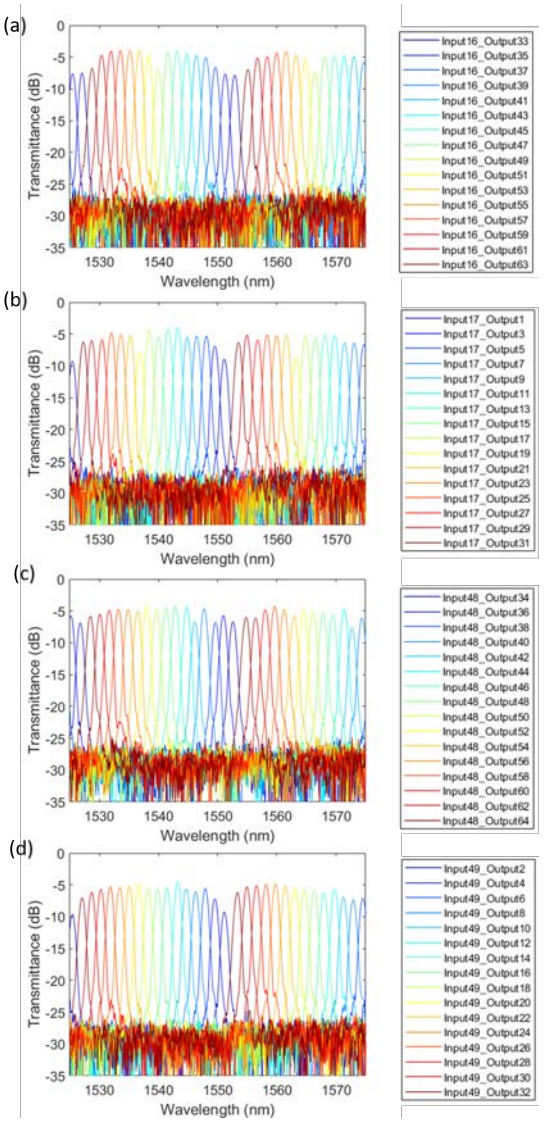

Fig. 6: Measured transmittance of the fabricated 32-port on-chip Thin-CLOS AWGR, with input port to be (a) port 16, (b) port 17, (c) port 48, and (d) port 49.

Conclusions

We designed, fabricated and demonstrated the first monolithic silicon photonic Thin-CLOS AWGR with 32 ports on a 5-layer silicon nitride platform. Measurement results show a 4.0 dB insertion loss and < -20 dB crosstalk values. The monolithic Thin-CLOS solution is scalable and compact. This work shows the possibility of making high performance, large port count SiPh AWGR by 3D photonic integration. The monolithic Thin-CLOS is also a candidate for large scale SiPh AWGR based optical interconnect systems of the future.

Acknowledgements

The devices were fabricated at Marvell Nanofabrication Laboratory (Berkeley, CA) and Center for Nano-MicroManufacturing (Davis, CA). This work was supported in part by US

Government and NSF ECCS award # 1611560.

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