Conversion Time-Power Tradeoff in Capacitance-to-Digital Converters with Dual-Mode Logic

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(Invited paper)

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***Abstract*— In this paper, the tradeoff between conversion time and power in nW-power capacitance-to-digital converters (CDCs) is explored. The CDC in this work leverages the delay-power flexibility of dual-mode logic, is based on swappable oscillators and operates at nW power and low voltage down to 0.3 V without requiring any additional circuitry, reference or voltage regulation. Its self-calibration compensates PVT variations and mismatch at any point of the chip lifecycle, eliminating the need for trimming at testing time. Testchip demonstration of the CDC in 180nm shows that its power consumption can be dynamically adjusted from 1.37 nW down to 418 pW at a conversion time down to hundreds of ms. This makes the CDC suitable for harvested systems with very limited tight power budget and fluctuating voltage.**

Keywords—Capacitive-to-Digital converter (CDC), Power consumption versus Time conversion trade-off, Ultra-Low Voltage, nW Power, Dual-Mode (DM) Logic.

I. Introduction

The increasing demand for low-cost battery-less sensor interfaces stems from the need for ubiquitous and long-lived sensor nodes for the Internet of Things (IoT) [1], [2]. Such systems need to operate under uncertain and aggressively scaled supply voltages and power down to the nW range, especially under direct powering by harvesters where intermediate DC-DC conversion is suppressed to further reduce power [3]-[7].

Among the most common sensor interfaces, capacitive sensor interfaces support a wide range of sensing modalities such as humidity, pressure, proximity and displacement [8], [9]. As their main building block, capacitance-to-digital converters (CDCs) with power within the power budget offered by millimeter-scale harvesters (e.g., solar cell) under realistic light conditions have been recently proposed [1], as shown in Fig. 1. In such directly-harvested CDCs, the challenge is to keep their peak power below the harvested power across its wide fluctuations. In other words, the design target in the above application domain is very different from conventional battery-powered systems, which focus on energy efficiency expressed as energy/conversion step, as evaluated from their average power [1], [2].

Regarding the general power-resolution tradeoff, CDCs with a resolution exceeding 14 bits has been shown at tens of µWs or higher [10]-[14], whereas 10-12bit resolution can be achieved at µW power [15]-[17]. Sub-µW CDC architectures achieve 7- to 8-bit effective resolution or less [18], [19]. The same resolution is achieved in CDCs with a power consumption down to the sub-nW range, although their

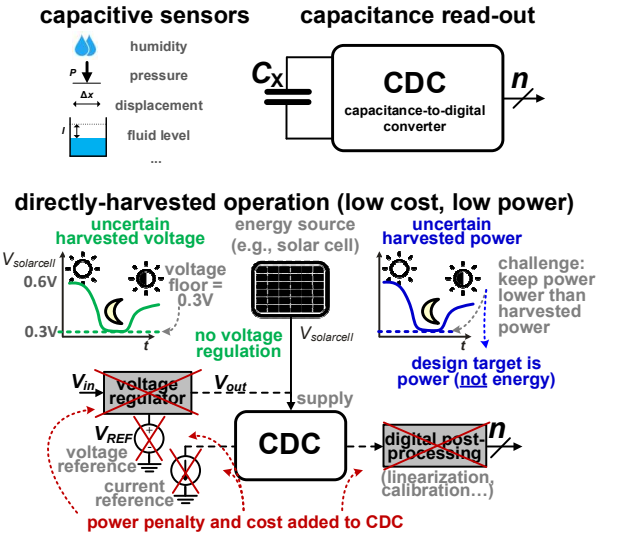

Fig. 1. Pictorial representation of a capacitive sensing in low-cost systems without additional circuitry for direct harvesting with harvester in the millimeter scale.

requirement of supply voltages above 0.6 V makes them unsuited for direct powering from energy harvesters [16].

Other CDCs with sub-nW operation at 0.6 V at ~7 -bit resolution have been demonstrated [19], although their power advantage is offset by the additional contribution of digital post-processing (~nWs), which was not accounted for. A fully-digital CDC operating at 0.45 V was introduced in [21], although it still requires another supply voltages of 1 V, and is therefore not suitable for direct harvesting. A CDC operating at voltages down to 0.3 V was proposed in [22], although its input range is limited, and its power in the hundreds of nWs is not suitable for direct harvesting in the millimeter scale.

In addition to considerations on the resolution, operation at aggressively low power in the nW range and below expectedly comes with conversion times in the sub-second or second scale [19], which are still in the acceptable range for many continuous monitoring applications [20] (e.g., temperature, humidity, proximity, fluid level monitoring). Also, the power budget of CDCs in prior art usually does not include the contribution of voltage and current references, voltage regulators and post-processing circuitry (e.g., linearization), although they are anyhow necessary for their correct operation.

In this paper, a CDC for low-cost directly-harvested systems systems is considered as a starting point [1], as it

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allows to pursue true nW power targets at no additional support (and power) from any of the above additional circuitry, as shown in Fig. 1. In this paper, additional flexibility in the conversion time-power tradeoff is introduced by exploiting the circuit properties of the dual-mode logic style [23].

The paper is structured as follows. In Section II, the principle and the architecture of the CDC are introduced. In Section III, the conversion time-power tradeoff is discussed in view of the experimental results from a 180-nm CDC testchip demonstration. The conclusions are finally drawn in Section IV.

II. Operation of CDC with Dual-Mode Logic

The operating principle of the CDC is illustrated in Fig. 2 and Fig. 3 [3]. The circuit is based on two relaxation oscillators OSC1 and OSC2, which are depicted as gray boxes in Fig. 2. Accordingly, their respective periods T_x and T_{ref} are proportional to their load capacitances, i.e. the unknown capacitance C_x to be measured, and the reference capacitance C_{REF}. For the sake of simplicity, C_x is assumed to be larger than the reference on-chip capacitance C_{REF}, and the CDC is assumed to be properly calibrated as in [3], so that they are made nominally identical within less than 1 LSB. As a result, the ratio of load capacitances is fully reflected in the oscillator period capacitance:

$$\frac{C_x}{C_{ref}} = \frac{T_x}{T_{ref}} \tag{1}$$

Eq. (1) holds regardless of process, voltage and temperature variations since the two oscillators track each other in terms of global process variations, voltage and temperature, whereas mismatch has been compensated through the above calibration.

From (1), the capacitance ratio of the two oscillators is accurately evaluated through the period ratio, which is in turn evaluated by counting the number of periods of one of the two oscillators within a measurement window that is proportional to the other period. In other words, the measurement window $t_{MEASURE}$ consists of an exact digitally-configurable number of periods of the other oscillator, as illustrated in Fig. 3. For this reason, the two oscillators are connected to an up counter (see top-right in Fig. 2) initially reset to zero, and a down counter (see bottom-right in Fig. 2) initially preset to a digitally-configurable integer M.

Assuming that C_{REF} is connected to OSC1 and C_x is connected to OSC2 as in Fig. 3, let n be the number of periods T_{ref} within the duration of the time window $t_{MEASURE} = M \cdot T_x$. Accordingly, the following equality holds within the quantization error of up to $\pm T_{\mathrm{REF}}$

$$M \cdot T_x = n \cdot T_{\mathrm{REF}}. \tag{2}$$

From (1)-(2), the capacitance C_x to be measured can be expressed in terms of the count n and the preset M as

$$C_x = \frac{n}{M} C_{REF} \tag{3}$$

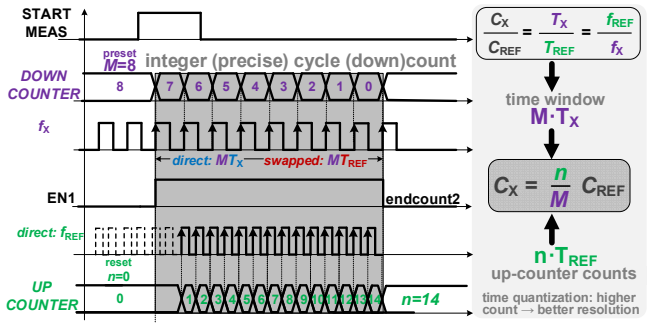

Fig. 2. Digital-based CDC operation and main waveforms.

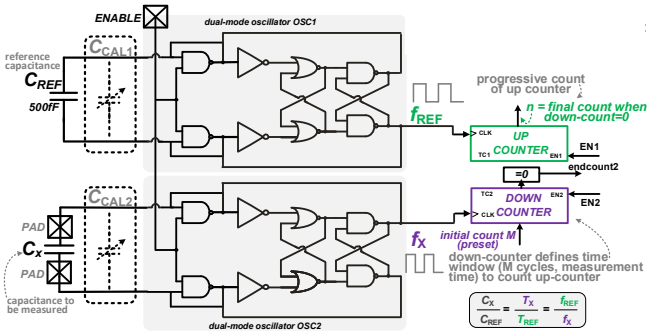

Fig. 3. Digital-based CDC architecture.

with a maximum absolute error below $\delta C_x = C_{REF}/M$, as due to the time quantization of $n \cdot T_{\mathrm{REF}}$ in (2) within the exact time window $M \cdot T_x$. The resulting relative quantization error $\delta C_x/C_x = 1/n$ is inversely proportional to the up-counter count n. From (2), lower quantization error (i.e., higher resolution) is achieved by increasing n and hence the preset M. Accordingly, the latter can be used as a knob to tradeoff the CDC resolution with the conversion time $t_{MEASURE}$, i.e. increasing the former at the expense of the latter. Such flexibility allows the reuse of the same design across different capacitance ranges and applications. In Fig. 3, all logic gates are based on the dual-mode logic style to achieve greater conversion time-power flexibility, as discussed in the following section.

A bitwidth of 12 in both the up and the down counter was chosen to remove the quantization noise limitation from the resolution, making it instead limited by noise. Ideally, this choice makes it possible to achieve a minimum theoretical quantization-limited absolute resolution of

$$C_{LSB} = \frac{C_{REF}}{M} > \frac{C_{REF}}{2^B} = 0.125\mathrm{fF} \tag{4}$$

whereas a worse resolution is expected when considering noise.

Due to its digital and differential nature from Fig. 3, the above CDC enables operation under aggressively low supply voltages, thus suppressing the need for voltage regulation. In particular, dual-mode logic is well known to operate below 0.3 V [23], as required by direct harvesting in this work.

III. Benefits of Dual-Mode Logic in CDC: Conversion Time-Power Tradeoff

Fig. 4 exemplifies dual-mode logic with a simple inverter gate [23]. When the header and footer bias voltage is set at

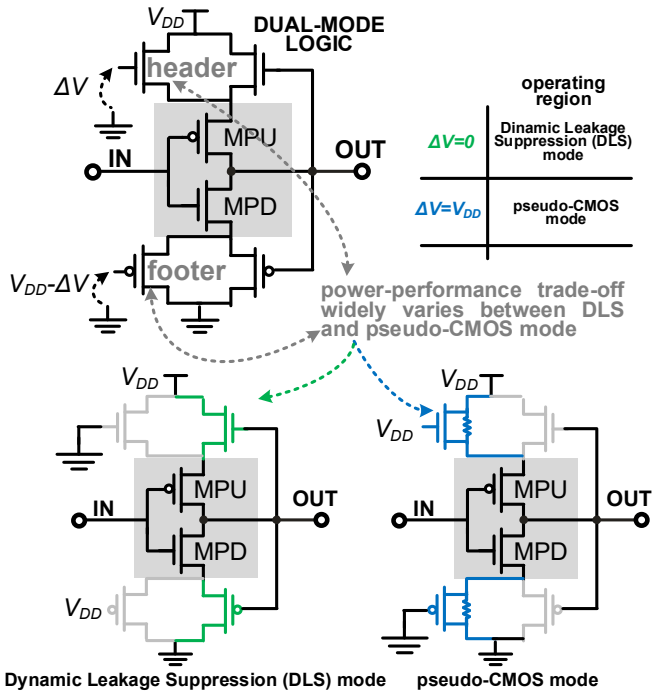

Fig. 4 Dual-mode logic can widely trade off power and performance by swapping the header/footer bias voltage.

ground and the supply voltage V_{DD} (i.e., ΔV=0 in Fig. 4), their strength becomes negligible and the dual-mode logic gate is very similar to the Dynamic Leakage Suppression (DLS) logic style [24], [25]. In this case, its leakage is reduced by 2-3 orders of magnitude compared to the regular transistor leakage, thanks to the super-cutoff operation of transistors MPU and MPD in Fig. 4 (see [23] for details). Although it comes at the cost of ms-scale gate delay, such leakage reduction is crucial in the targeted applications, as the tight power budget available in directly-harvested systems tends to be leakage-dominated [4].

On the other hand, swapping the header/footer biasing (i.e., ΔV=V_{DD}=0.3 V), the header and footer transistors have a strength that is much higher than all other transistors within the gate. Hence, the logic gate operates as source-degenerated standard CMOS logic, and the related mode is named "pseudo-CMOS" in the following. Compared to DLS mode, the pseudo-CMOS mode significantly reduces gate delay while increasing leakage and dynamic power, the latter being mostly due to increase in operating frequency. Compared to standard CMOS logic, dual-mode logic in pseudo-CMOS mode reduces leakage by at least ~4×.

In summary, dual-mode logic in DLS mode favors low power operation at the cost of speed, whereas the opposite holds for the pseudo-CMOS mode. In either mode, dual-mode logic correctly operates across the wide supply voltage range of 0.3-1.8 V, and its delay has a much lower sensitivity to the supply voltage compared to standard CMOS [25].

IV. Measurement Results

The CDC with extended conversion time-power tradeoff in dual-mode logic was implemented in a 180-nm testchip and characterized experimentally. The related tradeoff under different header/footer bias voltage ΔV going from 0 V (DLS

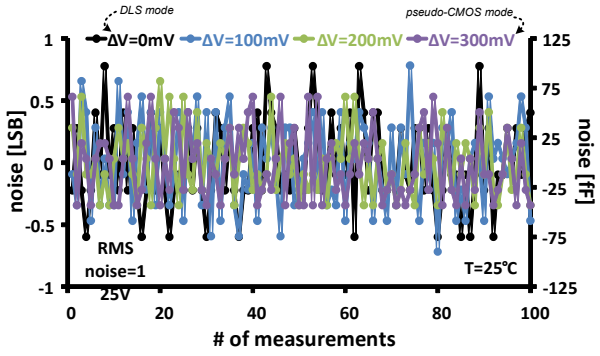

Fig. 5. Impact of noise across repeated measurements for different values of ΔV in Fig. 4 for C_x=10 pF. M=32.

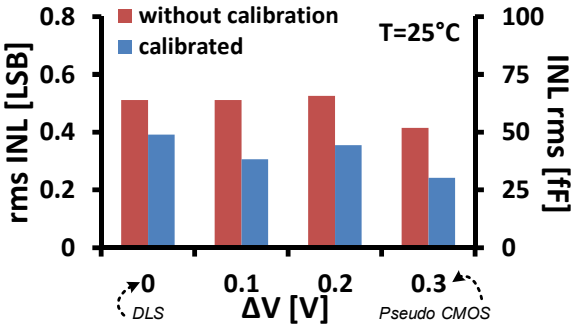

Fig. 6. RMS integral non-linearity (INL) versus ΔV in Fig. 4 for C_x ranging from 2 pF to 30 pF and M=32.

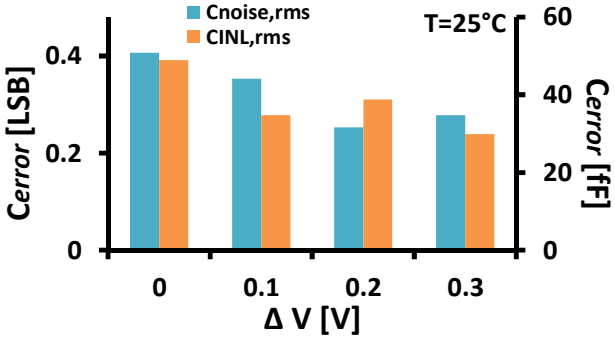

Fig. 7. Capacitance error due to noise and non-linearity vs. ΔV for C_x ranging from 2 pF to 30 pF and M=32.

mode) to 0.3 V (pseudo-CMOS mode) is explored in the following under the effect of the knobs available.

Regarding the down-counter preset M, lower values lead to an improved (shorter) conversion time and energy/conversion at the cost of increased quantization noise, as discussed in Section III. By contrast, the header/footer voltage adjustment through ΔV in Fig. 4 allows to improve the conversion time and the energy without degrading the effect of quantization noise, so that it does not become the dominant noise contribution in the conversion process. Fig. 5 shows the impact of noise for various values of ΔV from 0 to 0.3 V under C_x=10 pF and M=32. From this figure, the output-referred RMS noise decreases when moving from DLS to pseudo-CMOS mode, as expected from the higher transistor current at higher ΔV.

Regarding the integral non-linearity (INL), Fig. 6 shows its RMS value dependence on ΔV over a capacitance range from 2 pF to 30 pF. The minimum value of the considered capacitance is limited by the parasitic capacitance associated with pads and wires, which are connected in parallel and

hence add to the externally connected C_x. From Fig. 6, the post-calibration RMS INL is in the range of 29-48 fF for ΔV ranging from 0 V (DLS mode) to 0.3 V (pseudo-CMOS mode), which corresponds to 0.23-0.34LSB at the nominal LSB capacitance of C_{LSB}=125 fF.

Overall, from Fig. 7 the noise-limited capacitance resolution $C_{noise,RMS}$ ranges from 51 fF to 35 fF (0.28 LSB) for ΔV ranging from 0 V (DLS mode) to 0.3 V (pseudo-CMOS mode). Analogously, the linearity-limited resolution $C_{INL,RMS}$ ranges from 49 fF (0.39 LSB) to 30 fF (0.24 LSB) for ΔV ranging from 0 V to 0.3 V. The resulting SNDR is

$$SNDR = 20\log_{10}\frac{C_{range}}{2\sqrt{2}\,C_{err}} \tag{5a}$$

where the overall error C_{error} including both noise and non-linearity is evaluated as

$$C_{error} = \sqrt{C_{noise,RMS}^2 + C_{INL,RMS}^2}. \tag{5b}$$

From Fig. 7, the overall error capacitance C_{error} in pseudo-CMOS mode is reduced by 1.53X, compared to the DLS mode. The SNDR ranges from 43.5 dB to 45.2 dB after calibration, corresponding to 6.9 bits to 7.2 bits effective bits (ENOB), as detailed in Fig. 8.

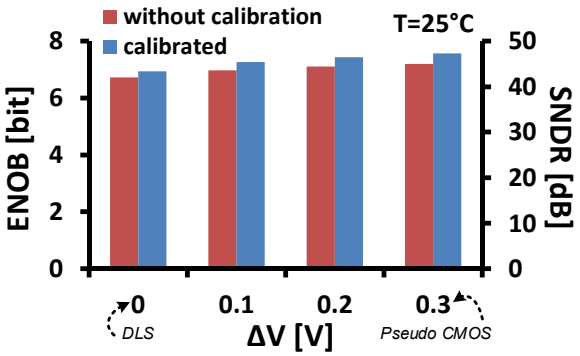

Fig. 8. SNDR and effective number of bits (ENOB) vs. ΔV for C_x ranging from 2 pF to 30 pF and M=32.

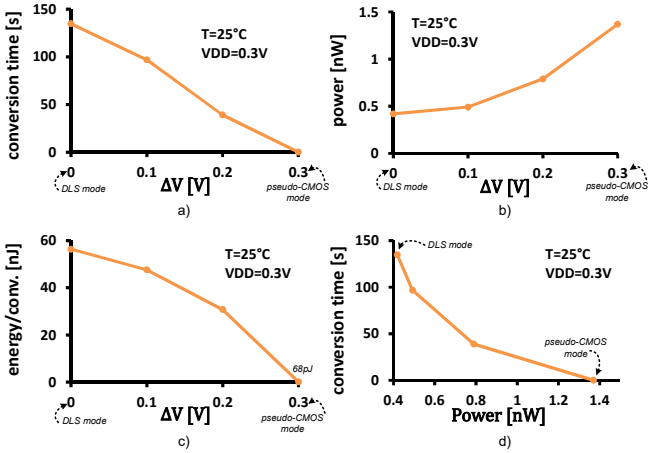

Fig. 9. Measurement results: a) conversion time vs. ΔV, b) power consumption vs. ΔV, c) energy per conversion vs. ΔV, d) conversion time-power tradeoff for M=32 and C_x=10 pF.

The conversion time increases substantially at low ΔV (i.e., DLS mode), whereas it is in the 50-ms range for ΔV values approaching 0.3 V (i.e., pseudo-CMOS mode), as shown in Fig. 9a. Conversely, the power consumption in DLS mode is 418 pW, and is 3.3X lower than in the pseudo-CMOS mode (1.37 nW), as show in Fig. 9b. Accordingly, the sensitivity of the conversion time to ΔV is much higher than the sensitivity of the power consumption, which makes ΔV an effective knob to improve speed at moderate power increase.

In pseudo-CMOS mode, the resulting energy per conversion is minimum and equal to 68 pJ, as illustrated in Fig. 9c. The conversion time/power consumption tradeoff in Fig. 9d confirms the much larger sensitivity of the conversion time to ΔV, as discussed above.

V. Conclusion

In this work, the conversion time-power tradeoff of fully-digital CDCs based on dual-mode logic has been explored. The tuning voltage available in dual-mode logic enables flexible operation across a range of conversion time and power targets, and hence adaptation of the same design to different applications.

Experimental characterization of a 180-nm testchip has shown that dual-mode logic tuning allows to dynamically adjust the power from 418 pW to 1.37 nW. The conversion time can be reduced down to the 50-ms range. In other words, dual-mode logic allows to adjust the conversion time at a graceful power increase. At the same time, the CDC is able to operate at very low voltages, as evidenced by measurements at 0.3-V supply.

The ability to operate at nW (or sub-nW) power and voltages down to 0.3 V makes the CDC suitable for directly-harvested systems without intermediate DC-DC conversion with very tight power budget and uncertain voltage. Also, the ability of the CDC to operate at any voltage in the 0.3-1.8 V range suppresses the need for voltage regulation. In addition, the CDC does not require any additional support circuitry in terms of voltage/current references of digital post-processing, retaining true nW-power operation at the system level.

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