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Cascaded multilevel inverter for vertical stabilization and radial control power supplies

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ABSTRACT

This paper presents the analysis and topology selection for the power supplies of the two DTT equatorial in-vessel coils for plasma vertical stabilization and fast radial control. The physics requirements and assumptions are analyzed in order to identify the system specifications. Since the basic configuration with two independent power supply circuits is too vulnerable to fast plasma events as disruptions, a circuit configuration including both coils is introduced. Two successive solutions, with three or two power converters, are proposed to supply such a common circuit. The adopted topology, based on cascaded H-bridge converters with IGBTs, is simulated by means of a simplified circuital model, that also consider the plasma disruptions. The simulation results show that vertical stabilization and fast radial control functions can be simultaneously achieved with two identical power converters and a passive imbalance branch by using a specific current control scheme.

1. Introduction

The Divertor Tokamak Test (DTT) project, under construction in the ENEA Research Center in Frascati, was mainly conceived as an experimental facility to investigate and solve the problem of the plasma power exhaust and other complex difficulties for the implementation path of nuclear fusion [1]. DTT will approach such issues in a DEMO-relevant configuration with a plasma current of up to 5.5 MA, a magnetic field of 6 T and an additional heating of up to 45 MW coupled to the plasma [1].

As the DTT mission is related to the plasma control and shaping, the in-vessel coils are crucial for its operations and then to its success. In particular, the equatorial coils and their power supply (PS) system shall be able to perform two critical functions [2,3]:

1 The first function consists in the plasma vertical stabilization (VS). It is worth stressing that elongated plasmas and alternative configurations, as those expected in DTT and in future tokamaks, are particularly sensitive to vertical instabilities.
2 Even though the DTT equatorial coils are simply classified as "VS", they can also produce a radial control (RC) action to preserve plasma facing components during fast plasma transients. In the literature, such RC is classified as "fast" with respect to poloidal field (PF) coils, but, especially for the aim of this paper, its response can be slower than that required to the VS function.

This paper focuses on the PS systems analysis and design for the two DTT equatorial coils. This investigation helps define the power supply topologies choice and constraints in VS coils driver. The rationale for selecting the coil circuit and topology is compared with other solutions. The specifications for the VS PS system are identified moving from the physics requirements and assumptions.

In the basic design, the VS function could be implemented by two in-vessel coils placed above and below the equatorial axis. The natural configuration for the control of the current in the two coils consists in connecting each of them to an independent PS. This configuration is effective in normal tokamak operations.

However, the configuration with two independent PS circuits is strongly vulnerable to fast events in the plasma. In particular, plasma disruptions can induce in the circuits currents up to six times with respect to the coil nominal values [2]. At such levels of overcurrent, the system (PSs, coils, busbars, supports, feedthroughs) survival is critical due to the electrical and mechanical stresses. Since the peak currents can be reached in few milliseconds, the time available for the response of

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active control and protection systems is limited, making preferable schemes that are intrinsically poorly affected by plasma disruptions.

In order to mitigate the risks of the two independent circuits, a configuration with a common circuit including both the VS coils is introduced. An upper (VSU) and a lower (VSL) coil are present, but they have a common imbalance branch where the current induced by disruptions is mostly concentrated. Since this branch is not used for the VS, the management of the disruption current can be approached without affecting the VS functions, as described in the next sections.

Two successive solutions are proposed to supply the common circuit:

1 The former solution is based on three power converters. Two fast converters implement the VS function, one slow converter is optimized for the RC and to withstand the disruption current.
2 The latter solution is even more simplified by removing the PS in the imbalance branch. Then, both the VS and the (fast) RC functions are achieved through two power converters, denoted as VSA and VSB, respectively.

The adopted solutions are analyzed and simulated by means of a circuital model, that takes into account also the plasma disruptions. The implementation of the two PS units, using cascaded H-bridge power converters based on insulated gate bipolar transistor (IGBT) switches, is also described.

2. Overview of the DTT in-vessel system

Fig. 1 sketches a cross-section of the DTT vessel and axisymmetric coils. The functions of the VS coils are alternative or complementary to those of the other active and passive structures, as summarized in the following:

1 The DTT ex-vessel superconducting coils include six PF coils and the central solenoid (CS) is divided in six modules [4].
2 A group of copper coils is placed close to the divertor to locally modify the plasma configuration in this region and to implement a sweeping control. These coils will be fed by three or four independent PSs, depending on the selected divertor configuration [5].
3 An array of non-axisymmetric (saddle) copper coils, not shown in Fig. 1, are installed inside the vessel to correct the static error fields (EFs) and to mitigate edge-localized modes (ELMs) [6,7].
4 A relevant contribution is provided by the passive (not connected to a PS) stabilizing plates, shaped as two large copper saddle coils with anti-parallel currents.

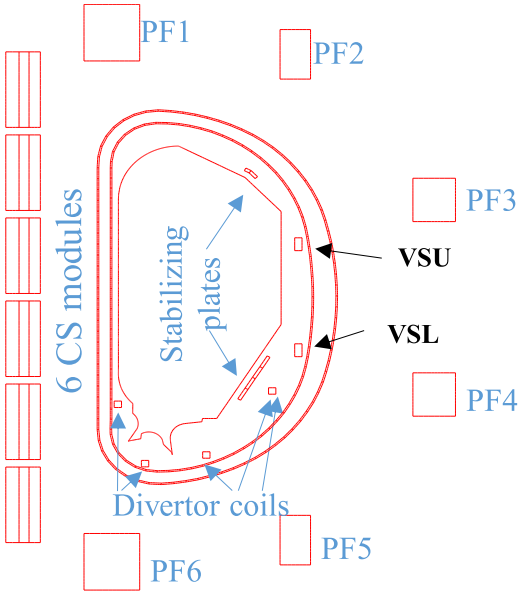

Fig. 1. Cross-section of the DTT vessel, active axisymmetric coils and stabilizing plates.

3. VS PS configurations and requirements

As sketched in Fig. 1, the two equatorial coils are denoted as VSU and VSL, respectively. Mostly for physical and mechanical reasons, each coils consists of 20 turns [2]. As two independent circuits are hard to be protected by the effects of the plasma disruptions, two configurations with a common imbalance branch are proposed in the following. In case of counter-serial connection without the imbalance connection, the VS coil system would be less vulnerable to centered disruptions and a single PS would be sufficient. The imbalance circuit is needed for the RC, especially during H-L transitions.

3.1. Configuration with three power converters

The first considered circuital solution is shown in Fig. 2. The optimized includes three power converters (VSA, VSB, and VLIM) acting on the three branches of a common circuit for both VS and RC functions. The three power converters are represented as DC/AC converters, because their desired currents are expected to have rapid variations.

The two magnetically coupled coils VSU and VSL must have opposite currents i_{VSU} and i_{VSL} to produce a radial field, while the current imbalance i_{LIM} in the common branch provides the vertical field for the RC. The power converters VSA and VSB produce the currents i_{VSU} and i_{VSL} flowing also in the corresponding VS coils, while the converter VLIM produces the current imbalance i_{LIM}. An additional inductor L_{IM} is inserted in the imbalance branch to limit the current during the plasma disruption.

Fig. 3 shows the standard time variations for the i_{VSU} and i_{VSL} currents and for the imbalance current when a VS is performed. As can be noted in Fig. 3, the imbalance current is zero, while the other two currents exhibit triangular waveforms with a peak value (I_{peak}) of 4.4 kA and a maximum frequency (f) of 40 Hz.

For the RC, the total maximum imbalance current is 3 kA for each coil, leading to a maximum of 6 kA for the imbalance current i_{LIM} during a total time of 250 ms.

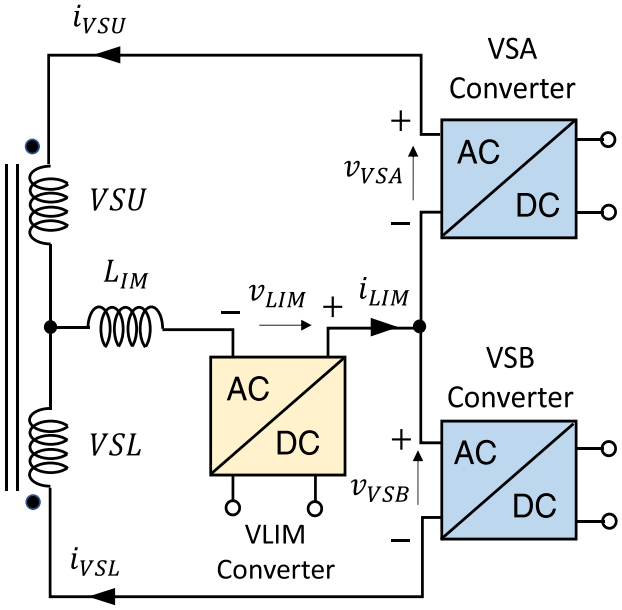

Fig. 2. PS configuration for the VS coils with a common imbalance branch and three power converter units, denoted as DC/AC converters.

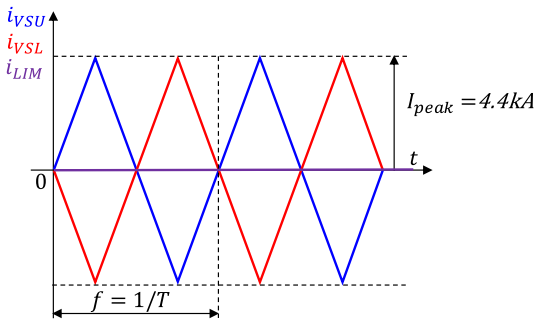

Fig. 3. VSS coils currents and imbalance current during normal operation.

Therefore, the main specifications for the VS coils could be summarized as:

- The maximum current in the VSU and VSL coils and in the VSA and VSB PSs is 4.4 kA.
- The maximum frequency requested for the previous currents is 40 Hz, with a di_{VS}/dt=704 A/ms.
- The maximum imbalance current is 6 kA to be obtained for 250 ms, with a di_{LIM}/dt=24 A/ms.
- All the PS voltage is 3.5 kV.

3.2. Configuration with two power converters

In the previous configuration, the currents in the three converters are not totally independent. Therefore, a proper control scheme could obtain the same results with only two power converters. Two options with two converters were considered:

1 Keeping only VSA (or VSB) together with VLIM. This option has the advantage of assigning each of the VS and RC functions to a specific converter.
2 Removing the VLIM. With this option, two identical converters should be designed and built, and none of them would be subjected to disruption.

The second solution was preferred for DTT. Of course, the control is more complicated with respect to the three-converters case and to the previous option, as presented in the next section.

4. Control of the VS PSs

4.1. Configuration with three power converters

The three DC/AC power converters are equivalent to current-controlled dependent voltage sources (Fig. 4a). The adopted scheme controls the VS coils currents and the imbalance current simultaneously, as shown in Fig. 4b. The control scheme needs only two measured currents (for example i_{VSU} and i_{VSL}) and uses two proportional-integral (PI) controllers.

The reference current for the differential mode (DM) controller corresponds to the reference current for the VSU coil $i^*_{DM} = i^*_{VSU}$. The feedback current is the DM current

$$i_{DM} = \frac{1}{2}\cdot(i_{VSU} - i_{VSL}) \quad (1)$$

The controller output is the reference voltage for the converters VSA and VSB. The bandwidth of the controller is in the range 150-200 Hz.

The reference current for the common mode (CM) controller is the imbalance current reference $i^*_{CM} = i^*_{LIM}$. The feedback current is the common mode current

$$i_{CM} = i_{VSU} + i_{VSL} \quad (2)$$

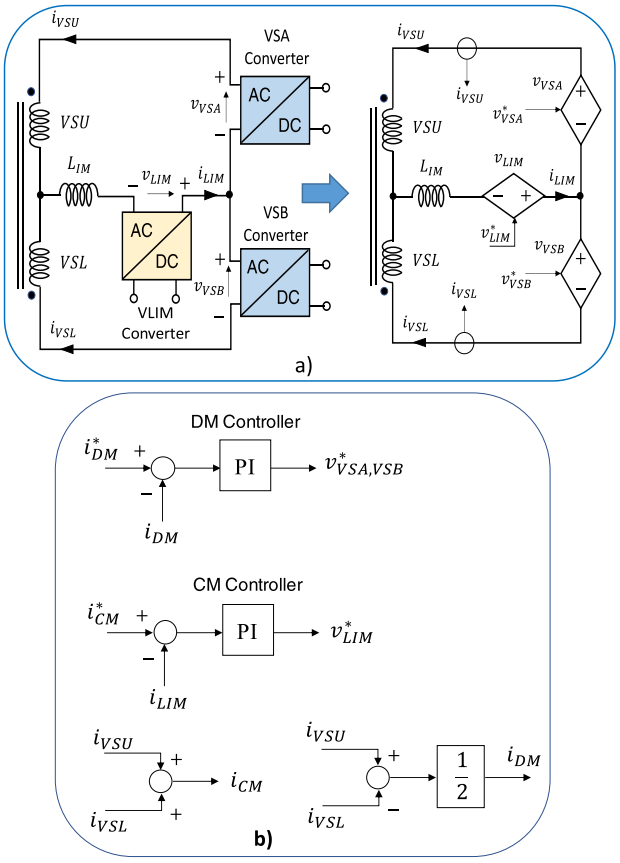

Fig. 4. a) Equivalent electrical schematic circuit of the supply configuration with three DC/AC converter units. b) Control scheme for this configuration.

The controller output is the reference voltage for the VLIM converter. The bandwidth of the controller is in the range of 25-50 Hz.

As noted in the introduction, the previous bandwidth is compliant with what is generally referred to as a fast RC, but the required response can be slower with respect to the VS. In practice, the high inductance L_{LIM} can protect the imbalance branch without affecting the RC performances [2]. Moreover, the VLIM converter can be slower and made of devices with higher overcurrent capabilities. The inductance of L_{LIM} is a fundamental parameter to be optimized [2]: higher values reduce the disruption overcurrent, but limit the RC response and may lead to an inductor with excessive dimension to be built. While [2] simulates the effect of 33.5 mH yielding an imbalance overcurrent lower than 5 kA, the value adopted in the following is set as three times the self-inductance of a VS coil, i.e., L_{LIM}=20.2 mH.

The control scheme for this configuration was simulated in the PLECS® tool using the simplified circuit model shown in Fig. 4a and dependent ideal voltage sources. The inductance for L_{LIM} was set at 20.2 mH, while the bandwidths of the DM and CM controllers were set at 200 Hz and 50 Hz, respectively. The startup of the PSs with zero imbalance current is shown in Fig. 5 for triangular reference DM current with a frequency of 40 Hz and a peak value of 4.4 kA. As it can be noted in Fig. 5, the currents in the VS coils are well controlled, being always of opposite sign and having the same absolute value.

The voltage request for the VSA and VSB converters is below 4 kV (about 3.8 kV). The needed voltage is higher than the case with three converters for the need to implement the RC action simultaneously with the VS action.

The regulation of the imbalance current is shown in Fig. 6. The CM reference current increases from zero to 6 kA (3 kA imbalance current for each VS coil) in 250 ms. As can be noted in Fig. 6, the imbalance current is well regulated, while the reference voltage for the imbalance

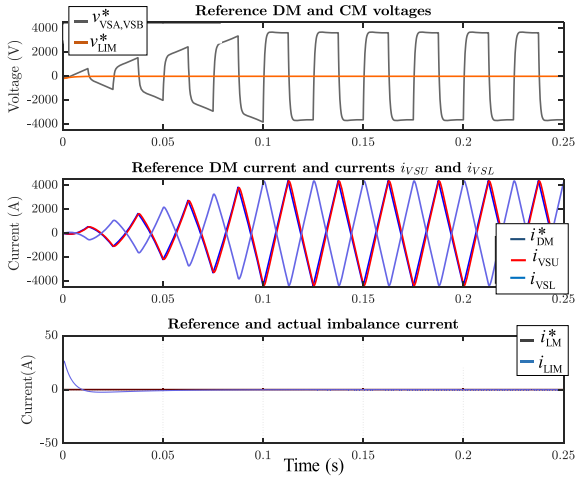

Fig. 5. Start-up of VS PSs for zero imbalance current and using a triangular reference current with a frequency of 40Hz and a peak value of 4.4 kA.

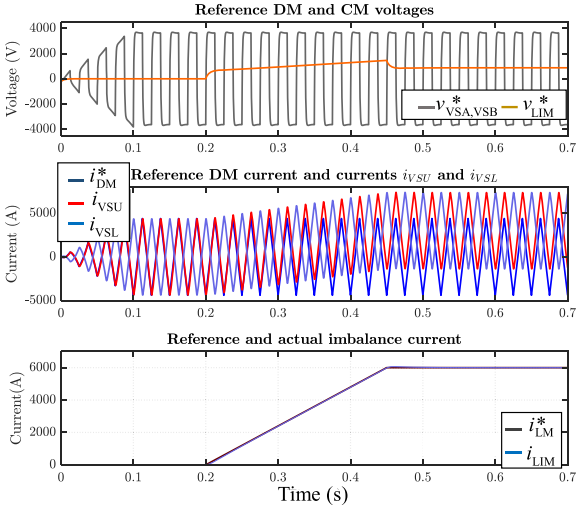

Fig. 6. Start-up of VS PSs using a triangular reference current having a frequency of 40 Hz and a peak value of 4.4 kA, followed by an increase if imbalance current up to 6 kA.

converter is about 1.5 kV.

4.2. Configuration with two power converters

With a proper control scheme, the PS system can be reduced to only two DC/AC power converters, as shown in Fig. 7 a. The two DC/AC converters are equivalent to current-controlled dependent voltage sources. With minimal modifications, the control scheme from Fig. 4b for the three-converters configuration is able to control the currents in the coils and the imbalance current simultaneously. The new control scheme is shown in Fig. 7b.

As can be noted in Fig. 7b, also this control scheme uses a DM PI controller and a CM PI controller, like the previous scheme depicted in Fig. 4b. The only difference is related to the calculation of the reference voltages for the two voltage sources VSA and VSB, that is

$$\begin{cases} v^*_{\mathrm{VSA}} = v^*_{\mathrm{DM}} + v^*_{\mathrm{CM}} \\ v^*_{\mathrm{VSB}} = v^*_{\mathrm{DM}} - v^*_{\mathrm{CM}} \end{cases} \tag{3}$$

where: v^*_{DM} is the output of the DM current controller for the regulation

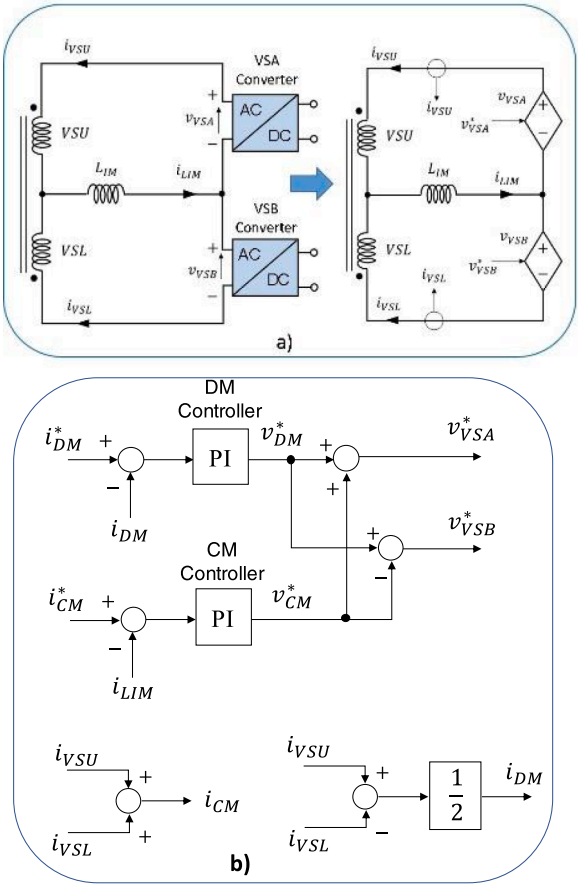

Fig. 7. a) Reduced PS configuration (left) and its equivalent electrical schematic (right). b) A proposed control scheme for the new arrangement based on two power converters.

of the DM current i_{DM}, while v^*_{CM} is the output of the CM current controller for the regulation of the total imbalance current i_{LIM}.

The proposed supply control scheme has been simulated in the PLECS® tool. As for the previous case, L_{LIM} was set as three times the self-inductance of a VS coil, i.e. L_{LIM}=20.2 mH, and the bandwidths of the DM and CM controllers have been set at 200 Hz and 50 Hz, respectively.

The simulation results obtained with this control scheme are perfectly equivalent to the arrangements with three converters. For the sake of simplicity, the results relative to the imbalance current of 6 kA are reported in Fig. 8. The only difference is the higher voltage required for the power sources VSA and VSB (about 5 kV). Therefore, the VS system with only two power converters is able to perform the required current regulation for both the VS and the RC functions.

5. VS PS topology

The power converters that can be used to drive the VS coils are medium voltage inverters with high output currents. As shown in the previously described simulation results, the maximum output voltage can reach 5 kV, while the current reaches 7400 A in the most severe current unbalance conditions (3 kA). In addition, the required current regulation bandwidth is quite high, in the range of 100-200 Hz.

Given the value of output voltage, multilevel solutions must be adopted. The most employed multilevel voltage-source converters include [8,9]:

- Cascaded H-bridge converter.
- Neutral point clamped (NPC) multilevel converter.

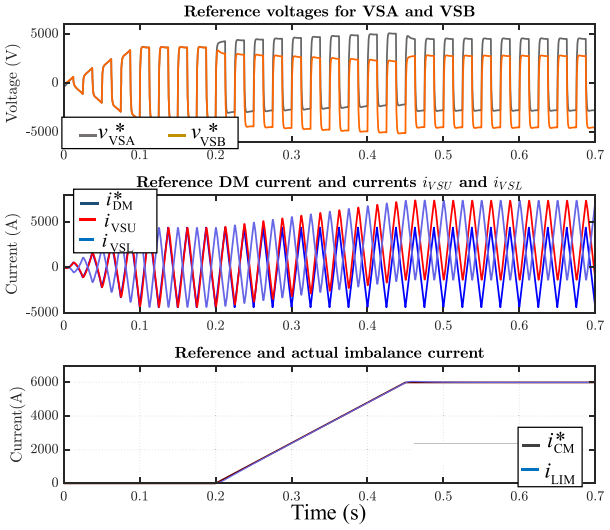

Fig. 8. Start-up of new VS PSs using a triangular reference current having a frequency of 40 Hz and a peak value of 4.4 kA, followed by an increase if imbalance current up to 6 kA.

- Modular multilevel converter (MMC).
- Flying capacitor (FC) multilevel converter.

Among all the solutions, the cascaded H-bridge converter is more suitable for single-phase inverters and offers more flexibility to increase the output current capability. Therefore, the solution adopted for this application is the cascaded H-bridge single-phase inverter, as shown in Fig. 9. As shown in Fig. 9, each DC/AC converter consists of n H-bridge converters operated as single-phase inverters.

The power switch technology adopted in the H-bridges is the IGBT, as the market already provides mature and highly reliable power module solutions available for voltage levels up to 6500 V and current levels up to 2400 A. Each H-bridge unit consists of 2 $\times N_c$ switching cells (legs) connected in parallel and using interleaving pulse-width modulation (PWM) to achieve the required output current. The interleaving allows the reduction of the PWM current ripple at the output. Starting from an analysis of the available IGBT solutions on the market, the main characteristics of each VS PS are reported in Table 1.

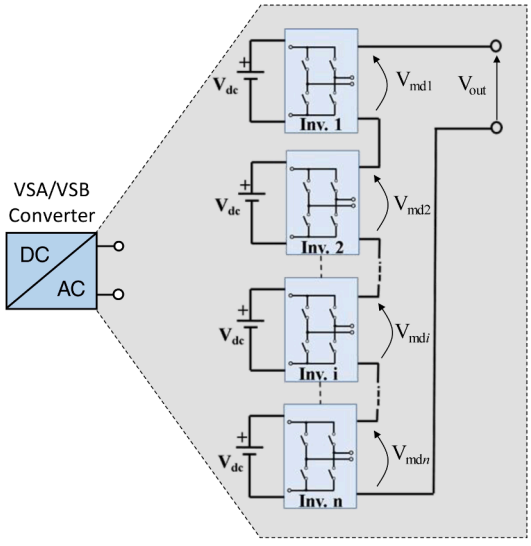

Fig. 9. Internal topology of each DC/AC converters shown in Fig. 7a. It is a multi-level converter with full-bridge single module topology.

Table 1
Main characteristics of each VS PS.

Parameter description	Value
Number of separated H-bridge units	4
H-bridge unit rated output voltage (peak value)	1.25 kV
Number of switching legs for each phase of one H-bridge unit	5
H-bridge unit maximum output current	7.5 kA
IGBT rated voltage V_{CES}	3.3 kV
IGBT rated collector current I_{Dnom}	2.4 kA

Each H-bridge unit is fed by a 12-pulse rectifier supplied by a transformer with double secondary windings using star and delta connections, respectively [10]. This is also expected to improve the power quality of the DTT electrical distribution system, which is rather critical [11]. Crowbar circuits [12] are needed both at the input and at the output of each H-bridge unit to avoid overvoltage during abnormal operating conditions, including plasma disruption. The resulting general power supply scheme is summarized in Fig. 10.

The crowbars at the H-bridge output protect from overvoltage, but the induced voltages could turn into additional currents, which can be critical for the circuit. Several fast transients, such as vertical displacement events and disruptions, were simulated in worst-case conditions [2]. The estimated currents resulted to be compatible with the mechanical constraints of the coils and of the connection busbars.

6. Simulation results

The simulations were carried out by arranging a circuit schematic in the PLECS® environment reported in Fig. 11.

The differential and common voltages references for a fixed CM current profile are reported in Fig. 12a. The DM reference current i_{refDM} and the measured currents i_{VSU} and i_{VSL} are reported in Fig. 12b. The differences of the i_{refDM} and the i_{VSU} and i_{VSL} (relative to VSU and VSL coils) in the mid area are due to the common mode current profile that add a CM current other than zero that modifies the i_{VSU} and i_{VSL} amplitudes. Fig. 12c shows the CM reference current i_{refCM} and the measured current i_{LIM} profiles. As shown in Fig. 12, the implemented current control acts accurately and effectively.

The modulation technique is based on the PWM technique arranged for multilevel converters [13]. The modulation is obtained by

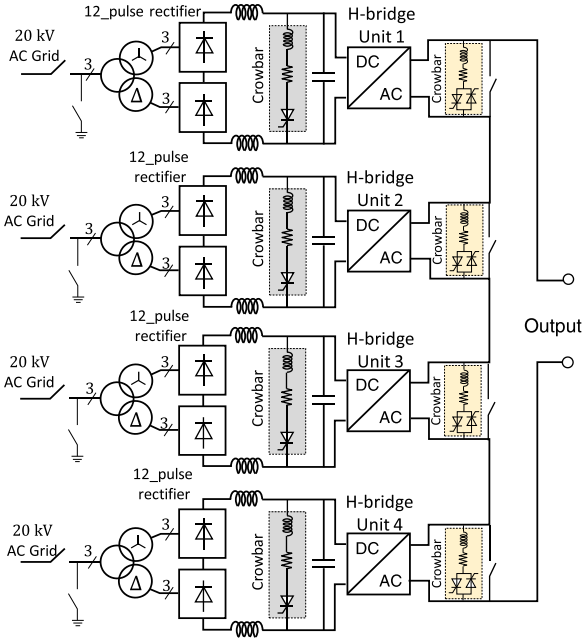

Fig. 10. Proposed general scheme for each of the VSA or VSB PSs.

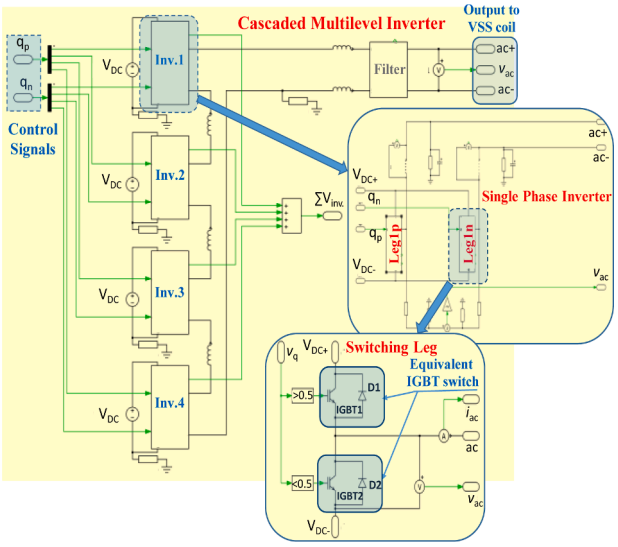

Fig. 11. PLECS® schematic of the scheme proposed for each of the VS PSs.

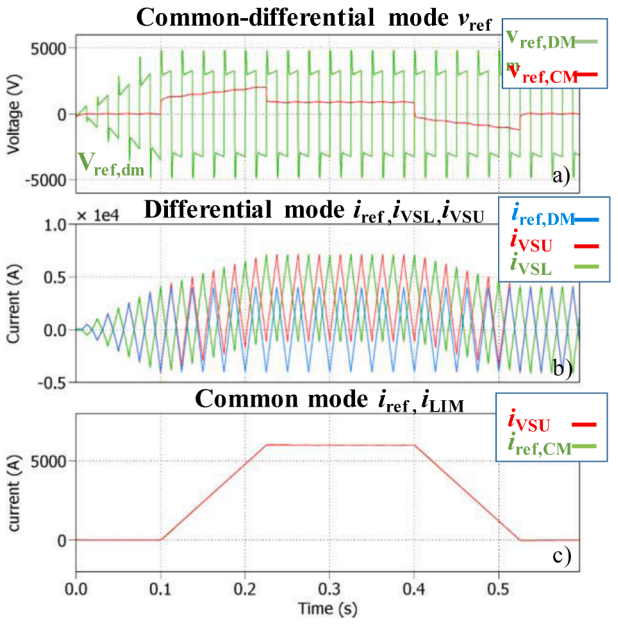

Fig. 12. a) CM and DM reference voltages from 0 to steady-state fixed profiles. b) DM reference current with both the currents measured in the VSU and VSL coils. c) CM reference current with the CM measured current i_{LIM}.

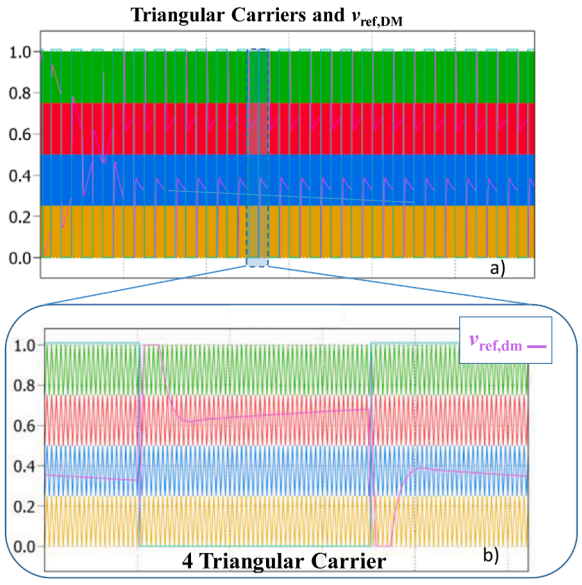

Fig. 13. a) triangular carriers and voltage reference. b) detailed view of the waveforms of the four triangular carriers and reference voltage profile for the frame considered.

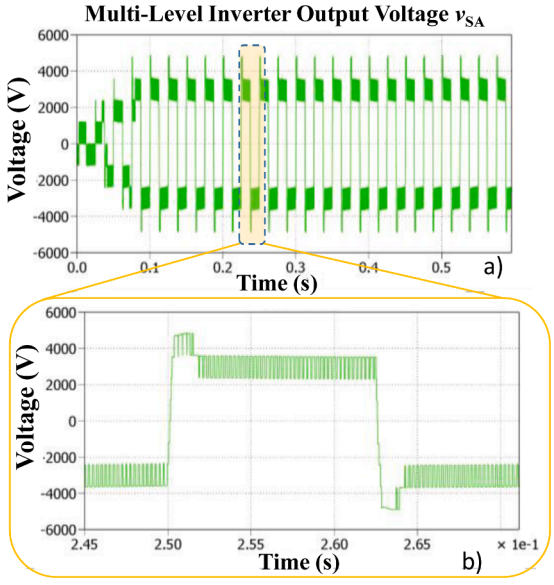

Fig. 14. a) Output voltage v_{SA} waveforms. b) zoomed view of the v_{SA} obtained in the frame considered.

comparing a modulating signal according to the desired profile (v_{refDM}) and four triangular waveforms (carriers) in order to obtain the command signals for the four inverter units. The multilevel inverter output voltage relative to the VSU coil (v_{SA} in Fig. 7) resulting from the simulations is reported in Fig. 13a. The comparison among the reference voltage and the four triangular carriers is depicted in Fig. 13a with a dotted line frame zoomed view (Fig. 13b). In Fig. 14b the output voltage v_{SA} is shown with the zoomed view reported in Fig. 14b.

Finally, Fig. 15 shows a detail of the modulation technique: Fig. 15a reports the four triangular waveforms as carriers and the reference voltage signal, while Fig. 15b reports the obtained output voltage.

7. Conclusions

This paper presented the analysis and simulation of the selected topology for the PS circuit of the in-vessel copper coils VSU and VSL for the VS and the fast RC of the DTT plasma.

The main requirement for the circuit selection was the mitigation of the disruption effects. Instead of two independent circuits, a configuration with a common circuit including both the VS coils and an imbalance branch is introduced. The three resulting branches can be controlled by only two power converters with simultaneous control of two branches.

The proposed implementation is based on two identical AC/AC power converter units. The DC/AC stages of the converter units are the most critical part of the design, in particular, due to the voltage and control specifications. The selected design for this part consists of cascaded H-bridge multilevel inverters with IGBT devices. The current control of the two DC/AC units use a CM loop and a DM loop, ensuring the requirements for VS and fast RC.

The proposed topology was simulated using the PLECS® simulation

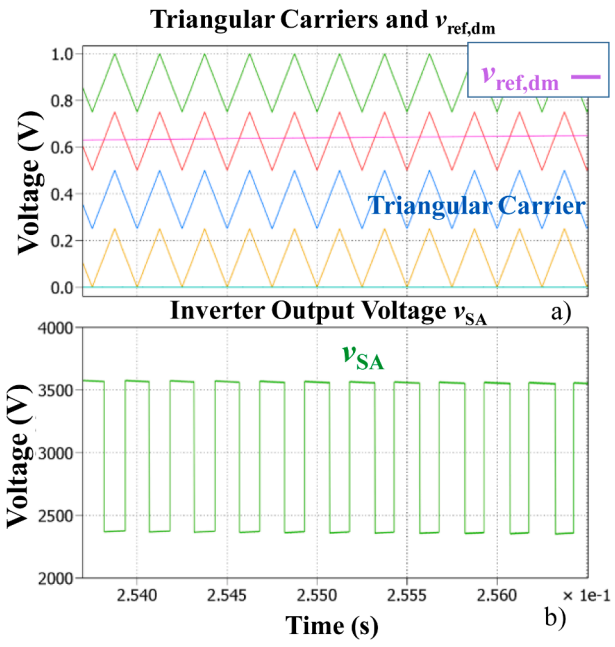

Fig. 15. Detailed view of the modulation technique. a) 4 triangular carriers requested and the voltage reference. b) Obtained output voltage v_{SA}.

software. The simulation results show the good dynamic performance of the adopted control scheme for the regulation of the currents flowing in the VS coils to implement the VS and the fast RC functions simultaneously.

Even though the proposed schemes and the presented results moved from the DTT specifications, they could be easily adapted for the design of the in-vessel coils of any tokamak.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request, if DTT gives the permission

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