5-55 GHz Watt-level Gallium Nitride Stacked FET Travelling-Wave Power Amplifier

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***Abstract* — Two well-known ultra wide-band topologies, the travelling-wave amplifier and the stacked cell, are gainfully employed to demonstrate a decade bandwidth behaviour (5-55 GHz) in conjunction with watt-level saturated output power. The selected technology is OMMIC's Gallium Nitride on Silicon, featuring the possibility to simultaneously insert 60-nm and 100-nm gate length FETs in the same MMIC.**

***Keywords* — travelling-wave amplifiers, millimeter wave integrated circuits, Gallium Nitride, broadband amplifiers, power amplifiers, FET stacking.**

I. Introduction

Ultra Wide-Band (UWB) amplification is needed in several applications such as instrumentation and electronic defence [1]. Although a design methodology for UWB Power Amplifiers (PA) employing a single-ended topology has been recently proposed [2], the Travelling-Wave Amplifier (TWA) architecture remains the most commonly adopted solution. Initial pioneering TWA designs date back to the early 50s [3]. Since then, several variations and improvements have been proposed. More recent solutions employ a combination of common-drain (CD), common-source (CS) and common-gate (CG) transistors to improve the gain-bandwidth product [4]. Among these, the stacked PA architecture has been exploited in different technologies, as a technique to improve gain and output power, without compromising bandwidth and efficiency [5]–[7]. High frequency applications often rely on extremely high f_{T} technologies, as GaAs m-HEMTs or InP p-HEMTs. These technologies are practically unrivalled in terms of operating frequency and noise performance. However, GaAs and InP suffer from low breakdown voltage levels, in the order of a few volts, making them unattractive when output power becomes a key design requirement even resorting to device stacking. For high-power applications, GaN becomes an interesting solution since it features high breakdown voltage values in combination with noteworthy f_{T} behaviour. Scaling down to gate lengths of 40-nm and 60-nm has been lately developed, and 100-nm GaN is becoming an interesting solution even for industrial-grade applications [8].

In this context, a test vehicle is proposed aimed at fulfilling the following requirements: decade bandwidth, from 5 GHz to 55 GHz, as demanded by modern electronic defence or instrumental equipment and output power in the order of 1 W with reasonable PAE and linear gain values (around 10% and 10 dB respectively). Several GaN-on-SiC technologies are available featuring high breakdown voltage and high output power at high frequency [9]. However, we opted for the OMMIC (now MACOM) GaN-on-Si process [8] operating at a lower drain voltage, bartering this limitation for a higher f_{T} and f_{MAX} to increase the operating bandwidth of the TWA. This technology also presents other interesting aspects. First, adopts a Silicon substrate making it an inexpensive solution for high-volume applications and possibly providing, in the future, integration with CMOS technology. The price to pay is an higher thermal resistivity of Si with respect to SiC, which could be critical in high-power amplifiers for spaceborne applications if dedicated design procedures are not applied. Most noticeably, it offers the distinctive option to simultaneously provide 100-nm and 60-nm gate length transistors in the same MMIC.

II. Demonstrator Design

The demonstrator's circuit diagram is depicted in Fig. 1. The proposed schematic advantageously applies the inherent benefits of two topologies well-known for their ultra wide-band behaviour: the travelling-wave amplifier and the stacked cell.

A. Technology selection

The technology selected for this demonstrator is the short gate length OMMIC's GaN-on-Si HEMT process [10], which well cover the target frequency range of this project and moreover offers the distinctive feature of making both the 60-nm gate length technology (D006GH) and 100-nm one (D01GH) available on the same MMIC. This feature is profitably exploited in the design of the stacked cell to simultaneously optimize bandwidth and power. The main figures of merit of the D01GH/D006GH technologies are: cut-off frequency f_{T} of 105/130 GHz, extrinsic trans-conductance g_{m} of 800/950 mS/mm, and maximum drain current density of 1.3/1.6 A/mm. Breakdown voltage and RF power density are in excess of 40 V and 3 W/mm for both gate lengths. The recommend drain-to-source voltage for high power is between 9 V and 11 V, while lower voltages are preferred for high-gain and low-noise behaviour.

B. Travelling Wave Amplifier

The TWA is designed considering $n = 8$ cells as best trade-off between the contrasting goals of gain, output power, size and complexity. A previous design attempt focusing on

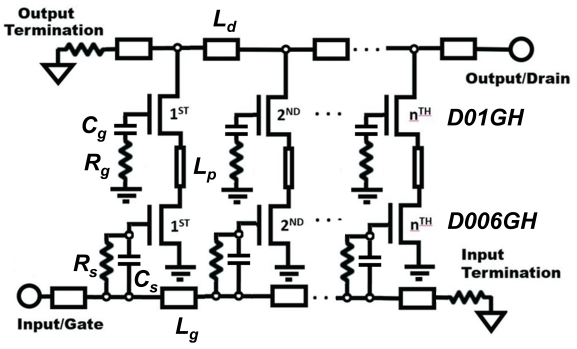

Fig. 1. Simplified AC electrical schematic of the Travelling Wave Amplifier employing stacked FETs as active cell. Bias circuitry is not shown.

linear performance and using a smaller number of cells is reported in [11]. Indeed, due to the ohmic losses of the transmission lines incorporated in $L_{\rm g}$ and $L_{\rm d}$ in Fig. 1, rather high on a Si substrate, performance deterioration is observed when using more than 8 cells. For the sake of simplicity we adopted identical cells. Admittedly, solutions adopting transmission line impedance and device size tapering are presented in the literature to improve PAE. However, these topologies are more complex since all cells are different.

The selection of the transistor size for the unit cell is a crucial aspect in a TWA. Larger devices would be preferable to increase gain and output power, being the latter heavily dependant on the total drain RF current, and the available gain of an ideal lossless element TWA given by:

$$G_{\rm av,TWA} = \frac{1}{4}(n \cdot g_{\rm m} \cdot Z_0)^2 \tag{1}$$

assuming identical and real input and output impedance $Z_0 = 50\,\Omega$. Therefore, since n cannot be arbitrarily increased due to losses, the designer would prefer to increase $g_{\rm m}$. This can be accomplished by increasing the device size, however at the expense of increasing also the transistor's parasitic capacitances that appear between the intrinsic gate, source and drain terminals, i.e. $c_{\rm gs}$, $c_{\rm ds}$ and $c_{\rm gd}$, which affect the TWA's bandwidth performance. The bandwidth-limiting effect of the total input capacitance, usually larger than that related to the drain side counterpart, has been mitigated both at cell level through the stacked approach, reducing the impact of $c_{\rm gd}$, and at TWA level by inserting an external capacitor, $C_{\rm s}$ in Fig. 1, between the gate transmission line $L_{\rm g}$ and the common source FET's gate terminal. Consequently, the overall shunt capacitance appearing along gate Artificial Transmission Line (ATL) is reduced, hence improving the bandwidth of the TWA. In fact, as a first approximation we can assume that the TWA's maximum operating frequency is close to $1/3$ of $f_{\rm T,TWA}$, being the latter the cut-off frequency of the ATL:

$$f_{\rm T,TWA} = \frac{1}{\pi\sqrt{L_{\rm g} \cdot C_{\rm g}}} = \frac{1}{\pi\sqrt{L_{\rm d} \cdot C_{\rm d}}} \tag{2}$$

where $C_{\rm g}$ and $C_{\rm d}$ are the total shunt capacitance values appearing in the gate and drain ATL, respectively.

The drawback of inserting $C_{\rm s}$ is the reduction of the TWA gain due to the partitioning of the driving signal across $C_{\rm s}$ and $c_{\rm gs}$, thus reducing the control voltage $v_{\rm gs}$: an acceptable price for bandwidth improvement, which is essentially the main goal of this design. As a design goal, we set an $f_{\rm T,TWA}$ in the order of 150 GHz so to have a maximum TWA operating frequency in excess of 50 GHz. This is accomplished by imposing 60 pH on $L_{\rm g}$ and 75 fF for the overall capacitance seen by the gate ATL, $C_{\rm g}$. The corresponding values on the drain side are determined to fulfill the phase synchronicity condition in the TWA, while guaranteeing a match to $Z_0 = 50\,\Omega$, being this parameter proportional to $\sqrt{L/C}$.

C. Stacked Cell

As shown in (1), in a TWA is of paramount importance to maximize the voltage gain of the unit cells while keeping the widest possible bandwidth: a requirement in contrast with the fact that any given transistor has a constant gain-bandwidth product. The classical cascode structure overcomes the bandwidth limitation by lowering the load seen by the input device, hence lowering the Miller component of the input capacitance. However in a cascode the achievable output power is limited by the drain-to-source voltage. This limitation can be overcome by resorting to the stacked configuration [12] than can operate at higher drain voltage, thus boosting both power and gain for the same given output impedance. Indeed, in a classical stacked cell design [13], [14], the load is considered as a free parameter, matched to m times the optimum load of the first, common-source (CS), stage (where m is the total number of devices in the stack). This typically represents an advantage in terms of achievable matching bandwidth since at high frequency the optimum load for power of a single device is usually lower than 50 Ω. Reversing the perspective, in the TWA the load of each cell is defined, thus the increase of the optimum load with transistor stacking allows to increase output voltage and power while keeping high efficiency.

Accounting for a target maximum frequency in the order of 50 GHz and the $f_{\rm T}$ of the technology, a 2-stacked structure was selected for this design [15]. For the CS stage the 60-nm transistor available in the OMMIC technology was preferred considering its higher intrinsic $f_{\rm T}$: as best trade-off between achievable power and bandwidth, a 2x50 μm periphery has been chosen, bias at a drain voltage of 6 V, while to maximize efficiency a 25%-class-AB quiescent drain current is achieved with -1.1 V at the gate. For the common-gate (CG) stage, the same device periphery was maintained but the 100-nm version has been exploited, which shows a better large-signal behaviour than the 60-nm counterpart. The total drain voltage was fixed in simulations at 15 V to accommodate for a larger swing in the CG device.

In a stacked cell the gate capacitance C_G of the CG is tuned to achieve best loading condition for the CS stage. In fact, $C_{\rm G}$ determines, through capacitive voltage division with $c_{\rm gs}$, the real part of the load seen by the CS element. The optimum value should be however selected accounting also for the stability of the cell, which is critically depending on $C_{\rm G}$, too. Fig. 2 shows how the maximum available gain (MAG) of the stacked cell vary with the gate capacitance: for

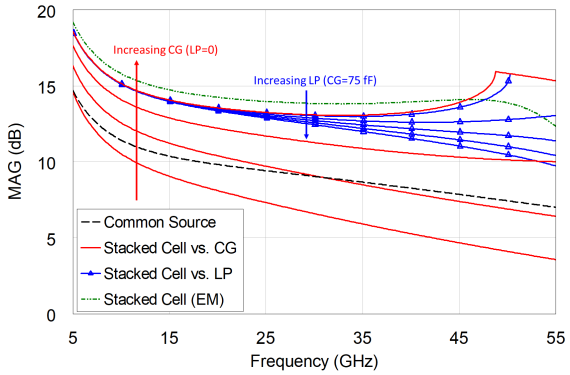

Fig. 2. Maximum Available Gain of CS stage alone (black dashed), stacked cell without L_P with C_G swept from 15 pF to 75 pF (red solid), stacked cell with fixed C_G and L_P swept from 5 pH to 85 pH (blue with symbols) and final stacked cell embedding EM passives (green dash-dotted).

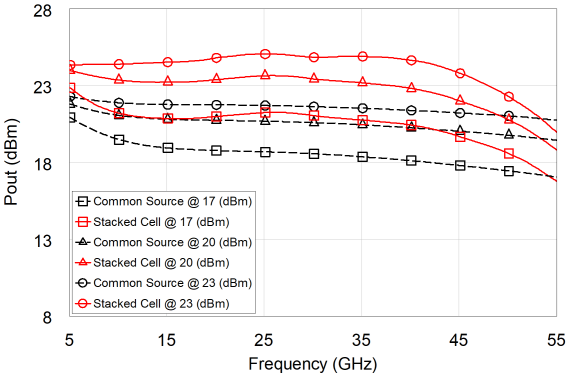

Fig. 3. Large-signal output power at fixed load for 3 fixed available input power levels: CS stage alone (black dashed) vs. stacked cell (red solid).

very low capacitance values the cell performs worse than the CS alone, while increasing it a sensibly higher gain can be achieved. However, for too high values the cell is no more unconditionally stable. This effect can be mitigated by adding an inter-stage peaking inductance L_P allowing for the uses of higher C_G values. At circuit-level, the optimum values found for the two components are 95 fF and 35 pH. The latter has been implemented optimizing the layout of the transmission line that connects the two transistors. The gain values obtained with the final cell optimized through electromagnetic (EM) simulations are also reported in Fig. 2.

Fig. 3 shows a large-signal comparison at unit cell level between the CS and the stacked cell: to this aim, a fixed load of 50 Ω has been selected while the imaginary part was chosen so as to optimize the dynamic load lines on the entire band. The stacked cell can achieve an output power up to 3 dB higher than that of the CS on the whole 5 GHz to 55 GHz band and better compressive behaviour.

To maintain some flexibility in circuit testing we avoided to develop a self-biased cell [15], so the common gate transistors' gate voltage is provided through a dedicated high impedance bias line, not appearing in Fig. 1.

III. Demonstrator Characterization

The MMIC, whose micro-photograph is depicted in Fig. 4, is characterized on wafer to verify its performance against

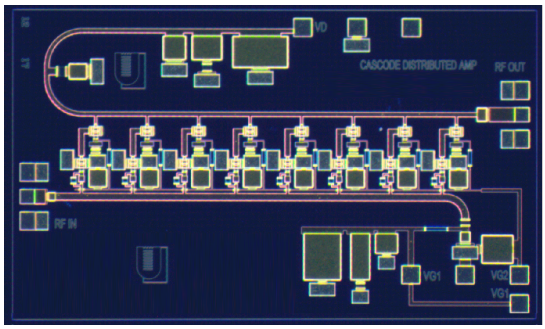

Fig. 4. MMIC micro-photograph. Chip size is 3.5 mm × 1.5 mm

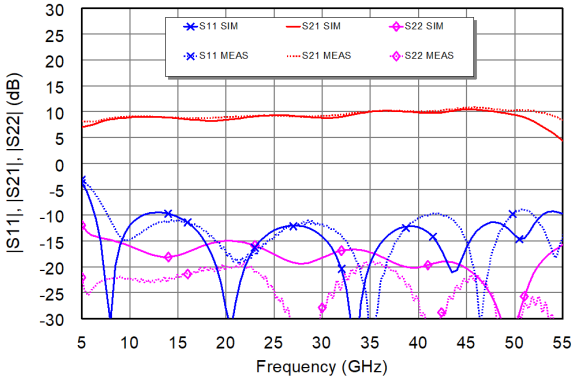

Fig. 5. Stacked TWA measured (dotted lines) and simulated (solid lines) linear parameters in the operating bandwidth.

target requirements and simulations. The common-source and common-gate FETs gate voltages are adjusted respectively to obtain the nominal drain current value and the desired portioning of V_D in $V_{DS,1} = 6$ V and $V_{DS,2} = 9$ V. V_{GS} on both FETs is around -1.1 V. Linear measurements are performed through Anritsu MS4640B VectorStar VNA that offers broad coverage in a single instrument (70 kHz to 70 GHz). Fig. 5 reports the measured and simulated liner parameters over the 5 GHz to 55 GHz bandwidth. The measured linear gain is typically 10 dB over the entire range, while input and output return loss are better than 10 dB. The agreement between measured and simulated values is good apart from a slightly higher gain observed experimentally around 55 GHz. This difference is likely due to the preliminary models used in simulations extracted on a technology not fully mature at the time. Nonlinear characterization is provided in Fig. 6. The actual measured frequency span is less than the nominal bandwidth due to limitations in the test set-up. This partial bandwidth characterization is rather typical of UWB designs. For the same reason, it was not possible to saturate the TWA below 18 GHz where only 0.5 dB gain compression was verified. Above 18 GHz instead the amplifier was close to saturation (1.75 dB gain compression). The typical saturated power is 28-31 dBm and the corresponding PAE is 11-16%. The drain DC current is practically doubled in saturated condition with respect to the nominal operating mode. The demo circuit here presented compares very well with similar circuits reported in the literature as described in Table 1. The output power is very high, despite being the only UWB circuit operating on a Silicon substrate, and the maximum operating

Table 1. State-of-the-art table of UWB GaN power amplifiers

param./ref.	[16]	[17]	[4]	[18]	[19]	[19]	[20]	T.W
BW (GHz)	2–32	8–42	0.1–45	0.1–44	1-57	1-50	DC-65	5–55
Gain (dB)	10–12	12–16	10–19	10–19	14.5	16	12-13	9–12
P_{OUT} (dBm)	30	27	31.5	31.5	26	27	29	28-31
P_{DC} (W)	6.3	8.0	5.2		3	3.5		6
PAE (%)	16	6	27		13	15		15
gate length (nm)	200	100	150	150	40	40	90	60 /100
Substrate	SiC	SiC	SiC	SiC	SiC	SiC	SiC	Si

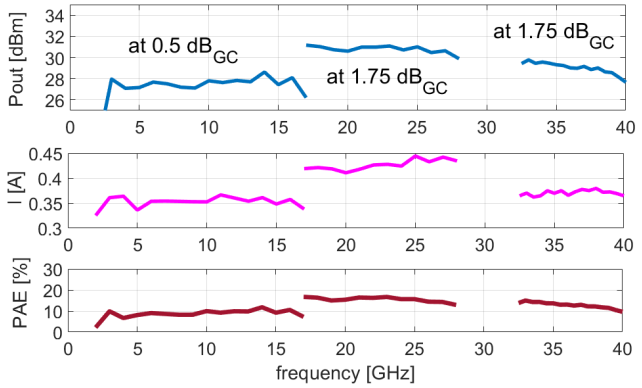

Fig. 6. Stacked TWA nonlinear characterization: output power (top), total drain DC current (middle) and PAE (bottom).

frequency is one of the highest reported.

IV. Conclusion

Design strategies and preliminary characterization of a GaN-on-Si stacked-cell-base TWA are presented. The two topologies are exploited to simultaneously obtain high-power, around 30 dBm, and large-bandwidth, from 5 GHz to 55 GHz. Demonstrated results are state-of-the-art in terms of maximum operating frequency and saturated output power, also thanks to the simultaneous use of 100-nm and 60-nm gate length FETs in the stacked cell to improve performance.

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