Capacitance-to-Digital Converter for Harvested Systems Down to 0.3 V With No Trimming, Reference, and Voltage Regulation

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Capacitance-to-Digital Converter for Harvested Systems down to 0.3V with No Trimming, Reference and Voltage Regulation

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Abstract— **In this work, a capacitance-to-digital converter (CDC) suitable for direct energy harvesting is introduced. The nW peak power and the ability to operate at any supply voltage in the 0.3-1.8 V range allow complete suppression of any intermediate DC-DC conversion, and hence direct supply provision from the harvester, as demonstrated with a mm-scale solar cell. The proposed CDC architecture eliminates the need for any additional support circuitry, preserving true nW-power operation, and reducing design and integration effort. In detail, the architecture is based on a pair of double-swappable oscillators, and avoids the need for any voltage/current/frequency reference circuit in the oscillator mismatch compensation. The digital and differential nature of the architecture counteracts the effect of process / voltage / temperature variations. A load-agnostic one-time self-calibration scheme compensates mismatch, and can be run from boot to run stage of the chip lifecycle. The proposed self-calibration scheme suppresses any trimming or testing time for low-cost systems, and avoids any input capacitance disconnection requirement. A 180-nm testchip shows 7-bit ENOB down to 0.3 V and 1.37-nW total power, when powered by a 1-mm^2 indoor solar cell down to 10 lux (i.e., late twilight).**

Index Terms— **Capacitance-to-Digital converter (CDC), Ultra-Low Power, Energy Harvesting, Ultra-Low Voltage, IoT**

I. INTRODUCTION

Capacitive sensing is required in a wide range of applications to monitor humidity, pressure, linear and angular displacement, fluid level, among the many others [1]-[3]. In low-cost energy-harvested systems for distributed monitoring [4]-[6], sensor interfaces including capacitance-to-digital converters need to operate under uncertain and possibly very low voltage and peak power levels. This is even truer under direct harvesting schemes [4]-[6], where intermediate DC-DC conversion between the harvester and the system supply is suppressed to reduce cost and power. Such aggressive power reductions are necessary to consistently fit the power harvested from the environment even when scarcely available (e.g., solar cell in the ~nW/mm^2 range [4]). This is quite different from
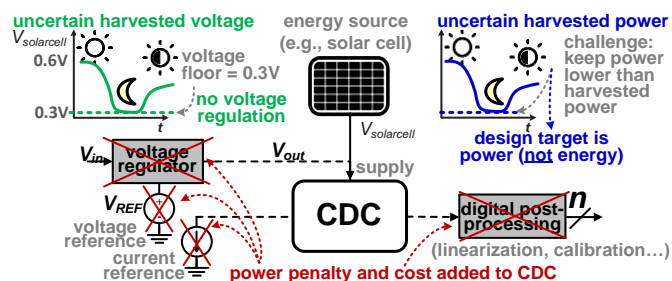

Fig. 1. Capacitive sensing in low-cost harvested systems requires operation under uncertain and low power and voltage levels, as well as the removal of power and voltage limitations imposed by conventional additional circuitry.

conventional battery-powered systems, whose design generally pursues low energy and low average power (rather than peak power). To date, several solutions have been proposed to enable operation at the nW power range and very low voltages in various sub-systems, although not in capacitive-to-digital conversion (see, e.g., [6] and the broad survey in [4]).

Focusing on capacitive-to-digital converters (CDCs), additional support circuitry such as voltage regulation, analog reference circuits and digital post-processing need to be suppressed to remove their additional power and voltage limitations at the system level. To preserve system cost effectiveness, trimming should also be removed to keep testing time minimal. In state-of-the-art CDCs, resolutions exceeding 14 bits are achieved at tens of µW power or higher [7]-[10]. 10-12-bit resolution can be achieved at µW power [11]-[15], whereas sub-µW CDC architectures typically achieve 7- to 8-bit effective resolution or less [16]. CDCs with a power consumption down to the sub-nW range have also been recently demonstrated [17], although their supply voltage above 0.6 V does not allow direct powering from energy harvesters under practical fluctuating environmental conditions (e.g., on-chip solar cell down to 0.3 V at dim indoor light). Sub-nW operation at 0.6 V and ~7-bit resolution has been demonstrated in [18], although the power of the additional digital post-processing is not accounted for (at least nWs, when optimistically considering only the leakage contribution). Sub-0.6 V operation has been shown in a portion of the fully-digital CDC architecture in [19], although its architecture requires an extra 1-V supply. Similarly to the CDC presented in this paper, the

CDC in [20] presents a dual-oscillator architecture that does not require external references and also operates down to 0.3 V, but its power is in the range of hundreds of nWs and hence two orders of magnitude higher.

The above CDCs with power at the lower end of the available range routinely come with conversion times in the sub-second or second scale (see, e.g., [7], [18]) and 7-8 bit resolution. Such specifications are certainly sufficient to support continuous monitoring in several applications of capacitive sensing, such as temperature, humidity, proximity, fluid level monitoring. Their power generally does not account for the additional consumption of voltage/current references, voltage regulators and other ancillary circuitry that are necessary for operation across harvested voltages, such as digital post-processing for linearization (see Fig. 1). Hence, their power does not directly reflect the actual impact at the system level.

In this work, a CDC for low-cost energy-harvested systems with true nW power is demonstrated. The proposed architecture is fully digital and is based on swappable oscillators to enable operation under uncertain supply voltages down to 0.3 V [21]. The CDC is equipped with a load-agnostic self-calibration scheme that reduces system cost by removing the need for any accurate test load, voltage, current or clock reference, while being executable any time (i.e., at boot and run time) without disconnecting the available load. Operation under a 1mm^2 solar cell at indoor lighting level is demonstrated. Such features make the proposed CDC highly suitable for capacitive sensing in applications where the temporal scale is in the second range, such as touch sensor, environmental (e.g., humidity), proximity, displacement and pressure monitoring in the built environment.

The rest of the paper is structured as follows. Section II introduces the architecture of the proposed CDC. Design tradeoffs are discussed in Section III. The proposed self-calibration scheme is described in Section IV. The testchip demonstration and its experimental characterization are discussed in Section V, along with the comparison with prior art. Conclusions are finally drawn in Section VII.

II. OPERATING PRINCIPLE AND ARCHITECTURE OF CDC BASED ON SWAPPABLE OSCILLATORS

The operating principle of the proposed CDC is illustrated in Fig. 2a. The CDC architecture is based on two relaxation oscillators OSC1 and OSC2, whose load can be swapped through proper switch box configuration. Under direct connection, OSC1 is connected to the unknown capacitance C_x to be digitized, and OSC2 is connected to the on-chip capacitance C_{REF}, and vice versa under swapped connection.

When $C_x > C_{REF}$, the direct connection is adopted and the oscillation period of OSC1 (OSC2) is hence proportional to C_x (C_{REF}). In particular, the oscillation period of OSC1 (OSC2) can be expressed as $T_x = R_{OSC1}C_x$ ($T_{REF} = R_{OSC2}C_{REF}$), being R_{OSC1} (R_{OSC2}) the PVT variation-dependent capacitance-to-period gain[1] of OSC1 (OSC2). Since the two oscillators are
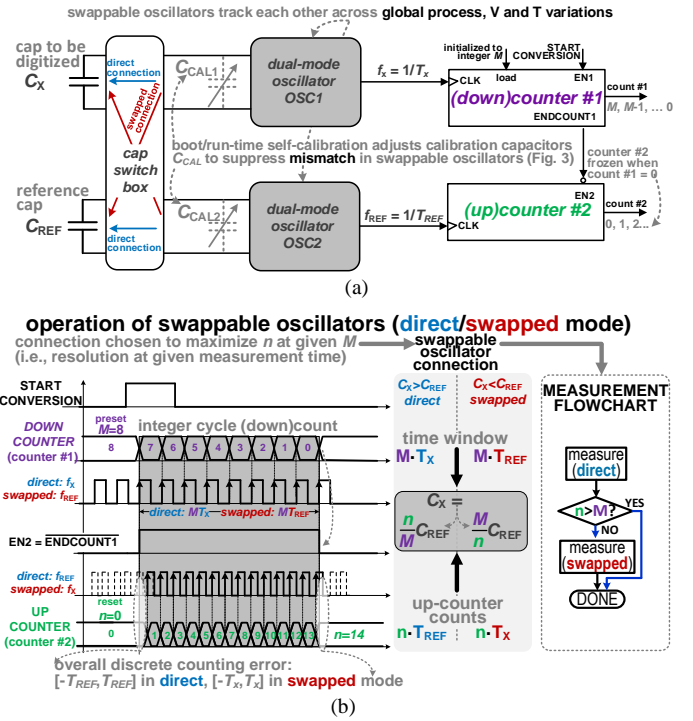

Fig. 2. (a) CDC architecture based on swappable oscillators, (b) operating principle and simplified timing in direct and swapped connection mode.

designed to be nominally identical, they are equally impacted by global process variations, voltage and temperature fluctuations. Assuming the mismatch between OSC1 and OSC2 has been compensated through the self-calibration procedure in Section IV, the condition $R_{OSC1} = R_{OSC2}$ is enforced and the capacitance ratio can be expressed as

$$\frac{C_x}{C_{REF}} = \frac{R_{OSC2}}{R_{OSC1}} \cdot \frac{T_x}{T_{REF}} = \frac{T_x}{T_{REF}}. \quad (1)$$

From (1), C_x/C_{REF} can be measured directly from the period ratio, and hence by counting the periods of OSC2 within a time window defined by OSC1, as illustrated in Fig. 2a. To this purpose, OSC1 is connected to a down-counter (counter #1 in Fig. 2a) that is initially reset at a pre-selected integer M, whereas OSC2 is connected to an up-counter (counter #2) that is initially preset at 0. The former defines an adjustable measurement time window $t_{MEASURE}$ consisting of exactly M periods T_x of OSC1, and ending when its count reaches $00\dots0$.

During the $t_{MEASURE}$ time window (Fig. 2b), the up-counter is enabled and its count increases by one at every OSC2 rising edge, reaching the final value n at the end of the window. Accordingly, the time covered by the integer number n of cycles of OSC2 period T_{REF} is approximately equal to $t_{MEASURE} = M \cdot T_x$, excepting for a residual time quantization error $\delta_{T_{REF}}$ associated with the discrete counting of OSC2 oscillations. Such quantization error invariably lies in the $]-T_{REF}, T_{REF}[$ interval[2]. As a result, the ratio of the two oscillation

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[1] Capacitance-to-period gains have the dimensions of a resistance and are therefore indicated with the letter R.

[2] This is the well-known time quantization error due to the inability of digital counters (in this case counter #2) to capture residual fractions of the period T_{REF} within a window $t_{MEASURE}$, compared to the exact ratio $t_{MEASURE}/T_{REF}$.

periods T_x/T_{REF} in (1) can be expressed directly as a function of the counter #1 setting M and the final count n of counter #2:

$$\frac{T_x}{T_{REF}} = \frac{n}{M} + \delta_{T_x/T_{REF}} \approx \frac{n}{M} \tag{2a}$$

$$\text{with} \quad \left|\delta_{T_x/T_{REF}}\right| \le \frac{1}{M} \tag{2b}$$

From (1) and (2a-b), the digitized value of the capacitance C_x under direct connection can be expressed as

$$C_x|_{direct} = \frac{n}{M} C_{REF} + \delta_{C_x} \approx \frac{n}{M} C_{REF} \tag{3a}$$

$$\text{with} \quad \left|\delta_{C_x}\right| \le \frac{C_{REF}}{M}. \tag{3b}$$

From (3a-b), the choice of M defines the absolute accuracy of the C_x readout and the conversion time, as set by the window $t_{MEASURE} = M \cdot T_x$.

When $C_x < C_{REF}$, the swapped connection is adopted as in Fig. 2a. Compared to the above case, the role of the two counters is reversed, hence counter #2 counts the periods of the oscillator output at frequency f_x, and reaches the final value n within a window $t_{MEASURE} = M \cdot T_{REF}$. Thus, the digitized value of the capacitance C_x under swapped connection is

$$C_x|_{swapped} = \frac{M}{n} C_{REF} + \delta_{C_x} \approx \frac{M}{n} C_{REF} \tag{4a}$$

$$\text{with} \quad \left|\delta_{C_x}\right| \le C_{REF} \frac{M}{n \cdot (n+1)} \approx C_{REF} \frac{M}{n^2}. \tag{4b}$$

It is worth noting that the above choice of direct (swapped) connection when $C_x > C_{REF}$ ($C_x < C_{REF}$) was implicitly made to minimize the relative error in the digitization of C_x. Indeed, from (3b) and (4b) the relative error $\left|\delta_{C_x}\right|/C_x$ turns out to be

$$\left|\frac{\delta_{C_x}}{C_x}\right| \le \frac{1}{n} \tag{5}$$

both in the direct and the swapped connection, and it is hence reduced under larger values of the final up-counter count n. Indeed, when $C_x > C_{REF}$ ($C_x < C_{REF}$), $n > M$ ($n < M$) in direct connection from (3a), whereas $n < M$ ($n > M$) in swapped connection from (4a). Accordingly, the choice of direct (swapped) connection under $C_x > C_{REF}$ ($C_x < C_{REF}$) invariably makes n larger than the opposite choice, minimizing the relative readout error for a given setting M. This choice also makes $n > M$ under any value of C_x, hence higher values of the setting M translate into larger n and hence lower relative error. This confirms that the digital setting M is as an effective knob whose increase improves the CDC resolution at longer conversion time, since $t_{MEASURE}$ is proportional to M from Fig. 2b.

In general, the swappable oscillators in Fig. 2a allow to digitize C_x whether it is larger or smaller than C_{REF}. If C_x ranges from values below to values above C_{REF}, the capacitance-to-digital conversion is executed according to the flowchart in Fig. 2b. A measurement is first performed with direct connection by assuming $C_x > C_{ref}$, and checking if this assumption is correct by verifying that $n > M$. Otherwise, the measurement is repeated after swapping the connection, keeping the relative error minimum as in (5).

III. Circuit Design and Tradeoffs

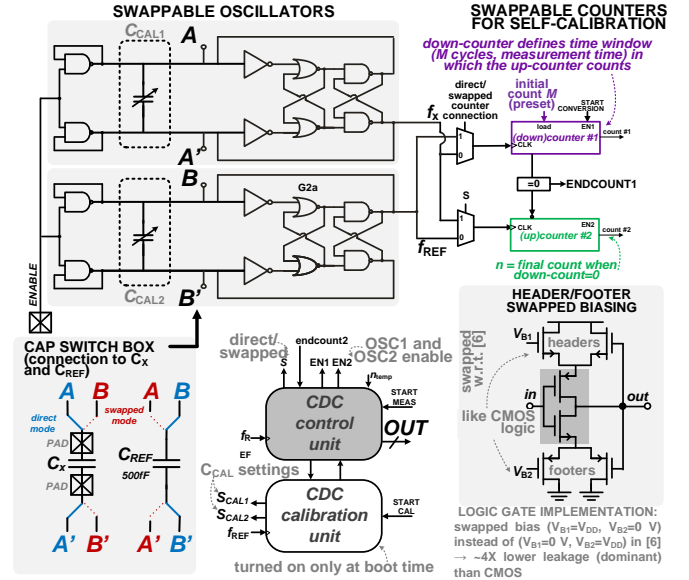The architecture in Fig. 2a employs two nominally equal

Fig. 3. Schematic of the CDC architecture in Fig. 2a detailing swappable oscillator circuits (top-left), swappable counters for self-calibration (top-right), switch box (bottom-left), and dual-mode logic gate with swapped biasing (bottom-right).

oscillators, whose power and frequency profile directly affect the conversion time-power tradeoff in the CDC. To reduce the power consumption of the latter well below CMOS logic, the two relaxation oscillators OSC1 and OSC2 are chosen to be based on the general topology in [22]. Differently from [22], in this work the header/footer gate bias voltages are swapped as in Fig. 3. Such swapped biasing avoids the unacceptably slow oscillation frequency in the Hz range under dual-mode logic with direct biasing, while maintaining rail-to-rail logic swing. In turn, this avoids very long conversion times, while retaining its main advantage in terms of ~4× leakage reduction (and hence power), compared to standard CMOS. Also, swapped biasing in Fig. 3 preserves the low supply sensitivity of the dual-mode logic gate delay, suppressing voltage regulation across a wide supply voltage range from 0.3 V to 1.8 V (see later). Swapped biasing is adopted in all counters, the CDC control unit coordinating the various phases of the conversion, and the calibration unit that orchestrates the self-calibration sequence described in Section IV for oscillator mismatch compensation. Regarding the counters in Fig. 2a, their bitwidth is chosen as a tradeoff between power, area, minimum achievable resolution and capacitance dynamic range, as detailed below. In the silicon demonstration in Section V, the bitwidth was set to 12 bits.

The CDC architecture in Fig. 3 makes the two oscillators double-swappable in terms of both load and counter. On one hand, the load capacitors C_x and C_{REF} are connected to the oscillators via pass gates, which select the direct and the swapped connection mode (as highlighted in blue or red in Fig. 3). The two modes are necessary both for normal conversion as in the previous section, and for the self-calibration scheme in the next section. As required by the self-calibration scheme, the counters are also made swappable through two digital multiplexers, which allow to connect each counter to either oscillator. Such second level of swapping allows to exchange the role of the oscillators in the counting process between, i.e.

which oscillator defines the time window, and which one is counted in it. The self-calibration strategy compensates oscillator mismatch by adjusting the two banks of binary weighted configurable calibration capacitors C_{CAL1} and C_{CAL2} in Fig. 3, which are respectively connected in parallel to the load of OSC1 and OSC2. Their capacitance dominates over the switch parasitics in view of their small transistor sizing since speed is not a primary concern in the targeted applications, making the switch parasitics ininfluent.

Given the operation in deep sub-threshold needed for nW-power targets, the input range of the architecture in Fig. 2a is limited by considerations on noise and conversion time. On the low side, the minimum detectable input capacitance $C_{x,min}$ is lower bounded by noise, as experimentally evidenced in Section V. $C_{x,min}$ can be lowered by reducing the effect of the RMS noise, and hence through longer conversion times and/or higher capacitance C_{REF}. In both cases, lower $C_{x,min}$ is achieved at the cost of longer conversion time, since higher C_{REF} proportionally increases $t_{MEASURE}$ in any case. In turn, not much margin is available to increase $t_{MEASURE}$ since the nW power target naturally comes with increased conversion time. Similarly, the maximum detectable input capacitance $C_{x,max}$ is set by considerations on $t_{MEASURE}$, since the latter proportionally increases when increasing C_x and is thus upper bounded by the maximum conversion time allowed by the application.

IV. LOAD-AGNOSTIC ANY-TIME SELF CALIBRATION WITH SWAPPABLE OSCILLATORS AND COUNTERS

In the architecture in Fig. 2a, the effect of global process variations, voltage and temperature fluctuations is mitigated by its ratiometric nature from (3a) and (4a), as well as the adoption of swapped-biased oscillator delay stages with inherently low delay sensitivity to the supply voltage. The residual effect of oscillator mismatch makes the ratio R_{OSC2}/R_{OSC1} deviate from its nominal value of one in (1), and hence needs to be compensated through calibration. In detail, the capacitance-to-time gains R_{OSC1} and R_{OSC2} of OSC1 and OSC2 in Fig. 2a are adjusted by adding digitally tunable capacitors C_{CAL1} and C_{CAL2} to their load capacitance port. C_{CAL1} and C_{CAL2} comprise four binary-weighted capacitors to fine-tune the oscillator input capacitance in the 0-160fF range with a resolution of 10fF, whereas C_{REF} was set to 500 fF.

In this work, calibration suppresses testing/trimming cost to suppress oscillator mismatch via any-time calibration (e.g., at boot and run time), with no requirement of a specific reference load or any extra time reference, and executable without disconnecting the capacitance being digitized. To this aim, swappable counters and a proper self-calibration strategy are introduced as in Fig. 4. Load-agnostic self-calibration is enabled by making the counters swappable as well, as achieved by connecting OSC1 and OSC2 to two digital multiplexers. In direct (swapped) counter mode, OSC1 is connected to counter #1 (counter #2), and OSC2 is connected to counter #2 (counter #1).

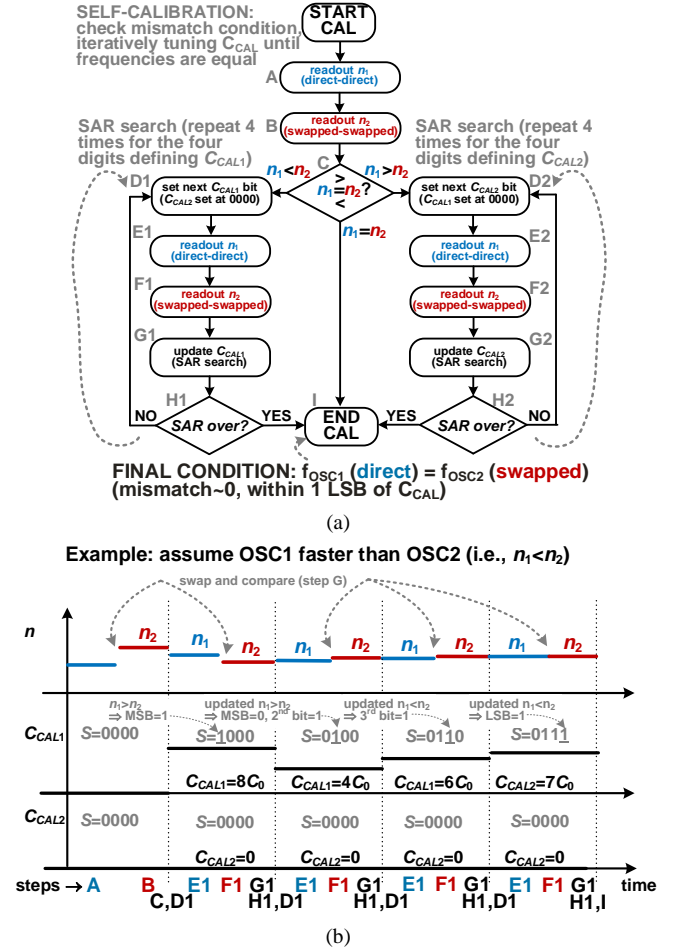The combination of swappable load (Section II) and

Fig. 4. (a) Self-calibration flow chart to suppress mismatch between the oscillators, based on the test condition in (7) from comparison of n in direct-direct and swapped-swapped connection. (b) Example assuming that mismatch makes OSC1 faster than OSC2, and step-by-step execution of self-calibration.

swappable counters results in CDC operation in four modes, as defined by the different combinations of direct/swapped mode in loads and counters. From (1)-(2a), the capacitive ratio readout in direct-direct mode is given by $(R_{OSC2}/R_{OSC1}) \cdot (n_{direct-direct}/M)$, whereas it is $(R_{OSC1}/R_{OSC2}) \cdot (n_{swapped-swapped}/M)$ in swapped-swapped mode. Accordingly, non-zero mismatch is easily signaled by the difference in the final count n of counter #2 in these two modes. Such difference monotonically decreases when R_{OSC1}/R_{OSC2} becomes closer to one, and it becomes zero when mismatch is suppressed. In other words, the difference in the final count n between the two modes is a mismatch test that does not require any specific load condition to be evaluated.

The above property in direct-direct and swapped-swapped mode enables the simple self-referenced and load-agnostic self-calibration of oscillator mismatch in Fig. 4a. Under a given and unknown C_x, the final count in direct-direct mode is first evaluated (step A in Fig. 4), which from (2a) results to

$$n_1 = \frac{M \cdot T_{x,direct-direct}}{T_{REF,direct-direct}} = M \frac{R_{OSC1}}{R_{OSC2}} \frac{C_x}{C_{ref}}. \quad (6)$$

Then, the same measurement is repeated in swapped-swapped mode (step B), resulting in the final count n_2 given by (6) with swapped R_{OSC1} and R_{OSC2}. The resulting difference $n_1 - n_2$ is

$$n_1 - n_2 = M \cdot \left(R_{OSC1}/R_{OSC2} - \frac{1}{R_{OSC1}/R_{OSC2}} \right) \cdot \frac{C_x}{C_{ref}}, \quad (7)$$

which is evaluated at step C in Fig. 4a.

If $n_1 > n_2$, from (7) R_{OSC1} turns out to be larger than R_{OSC2} (i.e., OSC2 is faster than OSC1 at same load), thus OSC2 needs to be slowed down by increasing its calibration capacitance C_{CAL2} as in Fig. 4a. The increase in C_{CAL2} can be adjusted by following a simple binary search, while maintaining C_{CAL1} at its minimum value associated with its 0000 digital setting. This corresponds to steps D-H in Fig. 4a, in which the calibration capacitance is tuned according to a successive approximation register (SAR) logic, and is either increased or decreased by half of the capacitance added at the previous step to progressively equalize n_1 and n_2 and thus compensate the effects of mismatch. Opposite conclusions are drawn if $n_1 < n_2$, under which a SAR optimization of C_{CAL1} is executed. The SAR optimization ends after four SAR search steps, pushing the difference $n_1 - n_2$ to its minimum value corresponding to a mismatch below the LSB of C_{CAL1} and C_{CAL2}.

An example of the proposed self-calibration procedure is presented in Fig. 4b. An initial measurement of n_1 (n_2) is performed in direct-direct mode at step A, and in swapped-swapped mode at step B. In this example, the comparison at step C reveals that $n_2 > n_1$, which means that OSC1 is faster than OSC2 and C_{CAL1} needs to be increased by setting its MSB to 1, while keeping C_{CAL2} at its minimum as in step D1. Then, the readout in direct-direct and swapped-swapped mode with the updated C_{CAL1} are executed in steps E1-F1, at which n_1 is found to be larger than n_2. This means that C_{CAL1} has been increased too much, requiring the SAR search needs to make its MSB equal to 0, and then tentatively set its subsequent bit to 1. The above procedure is repeated four times, and ends when the LSB is evaluated.

As desired, the above calibration scheme compensates mismatch independently of the specific value of C_x, and can hence be executed at any point of time from at boot or run time, without having to disconnect the capacitance being digitized. The absolute accuracy of the reference capacitance C_{ref} with process (i.e., across dice), voltage and temperature variations is shown to be compatible with the absolute accuracy target of 125 fF (i.e., kept within the LSB). In principle, such calibration procedure can be occasionally repeated to further reduce the residual impact of temperature variations. This opportunity will not be pursued in the following, as the intrinsic temperature sensitivity is already lower than other inaccuracy sources.

V. CDC TESTCHIP IN 180 NM AND CHARACTERIZATION

A test chip implementing the proposed CDC was designed and fabricated in 180 nm, occupying 0.2 mm² area as shown in Fig. 5. The 0.3-mm² logic for self-calibration is usually not necessary as it can be easily implemented in software within the on-chip microcontroller, when available. The test chip was powered with a sourcemeter for characterization across voltages, and by a 1mm² light harvester under controlled light intensity (as measured by a light meter) to demonstrate direct harvesting capabilities.

Unless specified otherwise, the measurements were performed with the down-counter preset M=32 as a compromise between $t_{MEASURE}$ and resolution, which was targeted to be C_{LSB}=125 fF (see below). The considered dynamic range of the off-chip capacitance to be digitized is 30pF. As measured with an LCR meter (Precision E4980AL), the minimum overall capacitance seen by the CDC is 2 pF, due to the additional parasitic capacitance associated with pad, bonding wire, and PCB. Such capacitance is routinely treated as an offset contribution, which can be hence suppressed through subtraction from any measurement.

The CDC linearity characterization across voltages, temperatures and dice is presented in Figs. 6a-b. To this aim, the capacitance to be digitized was tuned with a step of approximately 500 fF, and measured with fF-range resolution through a Precision E4980AL LCR meter. From Fig. 6a, the post-calibration maximum (RMS) integral non-linearity INL for the worst-case die #1 is 125 fF (48 fF), corresponding to 1 LSB (0.39 LSB). From the same figure, the proposed self-calibration enables a 1.4× improvement over the CDC without calibration, whose maximum (RMS) INL is 177 fF (64 fF), corresponding to 1.4 LSB (0.51 LSB). From Figs. 6b-c, the above experimental results were found to be consistent across
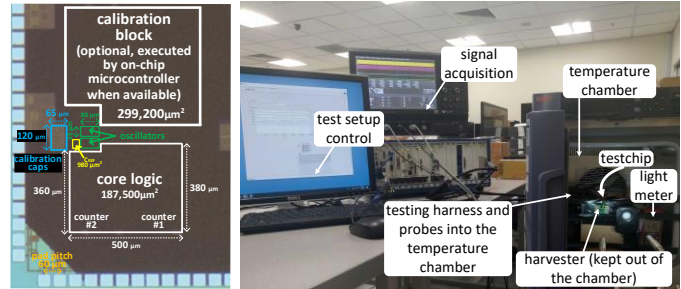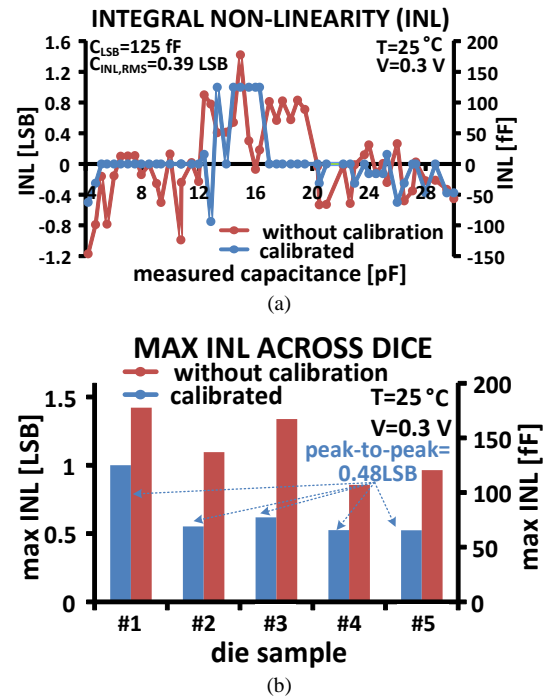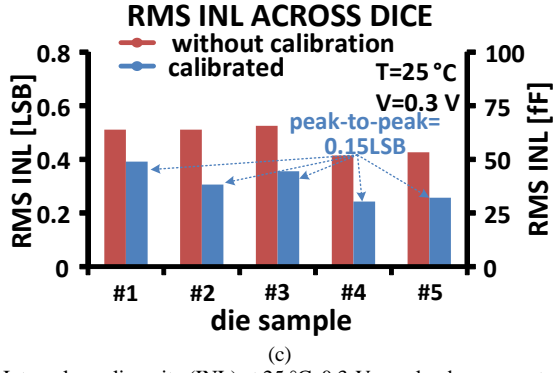

Fig. 5. Die micrograph and testing setup.

(a)

(b)

Fig. 6. Integral non-linearity (INL) at 25 °C, 0.3-V supply, down-counter preset M=32, with and without calibration: (a) INL versus code (die #1 having highest INL), (b) maximum INL vs die sample, (c) RMS INL vs die sample.
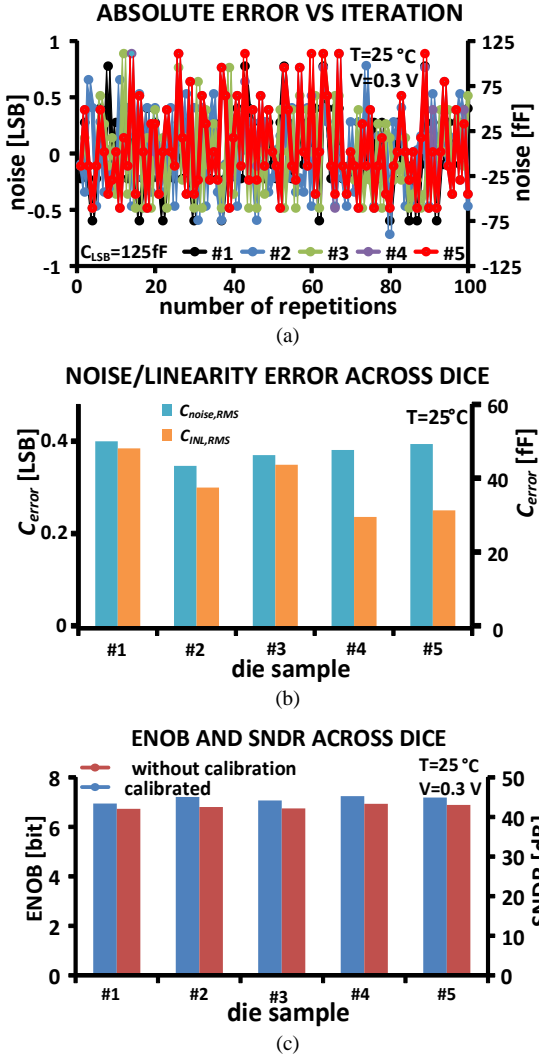

Fig. 7. (a) Noise characterization across readout repetitions (25 °C, 0.3 V), (b) noise/linearity error across five die samples, (c) resulting ENOB and SNDR.

the five measured dice, whose maximum (RMS) INL has a worst-case deviation from the average of 0.29 LSB (0.08 LSB).

Noise was characterized by repeating the readout under the same environmental conditions, as reported in Figs. 7a-c.

Across the measured die samples, from Fig. 7a the maximum (RMS) error is expectedly consistent and ranges from 89.8 fF to 97 fF (from 43.5 fF to 50.5 fF). The resulting noise-limited resolution $C_{noise,RMS}$ across 100 measurements at $C_x=20C_{REF}$ is 45.7fF (i.e., 0.36 LSB) from Fig. 7a. Combining both (supply and transistor) noise and linearity[3] as broken down in Fig. 7b, the resulting SNDR in Fig. 7c is again consistent across the five measured dice, ranging from 43.5 dB to 45.2 dB (from 42.3 dB to 43.5 dB) with (without) calibration, corresponding to 6.94 bits to 7.24 bits effective bits (6.73-6.93).

The effect of supply voltage on the overall error is plotted in Fig. 8a. When the supply voltage varies from 0.3 V to the nominal voltage 1.8 V, from Fig. 8a the error magnitude after self-calibration is well below the LSB and decreases to 0.16 LSB. From the same figure, calibration reduces the maximum error magnitude across voltages by 47%. This plot confirms the unique ability of the proposed CDC to operate at nearly-constant linearity and resolution under unregulated supply, as enabled by its differential nature, swapped-biasing logic and self-calibration. This also confirm that one-time self-calibration is sufficient to mitigate the effect of voltage variations.

The effect of temperature on the error is shown in Fig. 8b under a temperature range from -25°C to 75°C. This figure shows that the total error is again well below the LSB after one-time self-calibration, and ranges from -0.66 LSB to 0.21 LSB. From Fig. 8b, one-time self-calibration improves the maximum error magnitude by 3X. In other words, the self-calibration in Section IV provides a more pronounced benefit in terms of temperature sensitivity reduction, compared to voltage and process sensitivity.

The above results expectedly tend to improve at larger down-counter preset values M, thanks to the improved accuracy and noise immunity at longer $t_{MEASURE}$ (see Sections II-III). The benefits of larger M were experimentally quantified by increasing its value from 32 (as relevant to all above results) to 64 and 128. Compared to the INL=0.39 LSB at M=32 in Fig. 6a, the RMS value of the INL=0.23 LSB at M=64 in Fig. 9a is reduced by 1.7X, and further doubling of M to 128 further reduces the RMS INL=0.18 LSB by another 1.3X from Fig. 9b. This improvement comes at a proportionally higher conversion time, or equivalently at a smaller capacitance dynamic range for a given maximum conversion time. For example, the maximum capacitance to keep the conversion time at 1 s is respectively 64 pF for M=32, 32 pF for M=64, and 16 pF or M=128.

To gain a deeper insight into each of the above effects, the impact of M on noise immunity and linearity was separately studied in Figs. 10a-c. From Fig. 10a, the RMS noise under M=32, 64 and 128 respectively decreases from $C_{noise,RMS}$=50.8 fF down to 41.5 fF and 24.5 fF. This corresponds to a decrease that is proportional to $1/\sqrt{M}$, as shown in Fig. 10b. such trend is expectable from the proportionality of the conversion time to M (i.e., more time averaging) and the uncorrelated nature of

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[3] SNDR was evaluated by definition as $20 \log_{10} \frac{C_{range}}{2\sqrt{2} \, C_{error,RMS}}$, being C_{range}=30 pF the maximum considered capacitance, and $C_{error} = \sqrt{C_{noise,RMS}^2 + C_{INL,RMS}^2}$

the equivalent capacitance error due to both noise and non-linearity [25]. The resulting ENOB is defined as (SNDR – 1.76)/6.02 dB as usual [26].

thermal noise.

Fig. 10c shows the overall resolution improvement at larger values of M, when including both noise and non-linearity into the effective number of bits (ENOB). For the considered range of C_x up to 30 pF, the post-calibration ENOB improves by 0.2 bits (0.69 bits) at M=32 (M=64), compared to pre-calibration. The resulting post-calibration ENOB improvement from M=32 to 64 is 0.53 bits. In other words, increasing M leads to a direct linear increase in the conversion time, while improving ENOB more slowly and in a sub-linear manner. For fair comparison with the case M=128 under the same 1-s maximum conversion time, its maximum capacitance was halved compared to M=64, as discussed above. Accordingly, the range of C_x up to 15 pF was considered in Fig. 10c for M=128, as well as for 64 and 32 for fairness. The comparison of the respective results in Fig. 10c shows that ENOB improves by 0.47 bit/oct when increasing M.

In summary, the results in Figs. 9a-b and 10a-c confirm that the down-counter preset M can be adjusted to dynamically trade off quantization- and thermal noise-limited contributions with the overall resolution and the conversion time. The implications in terms of energy per conversion will be discussed in the next section.

VI. POWER, CONVERSION TIME AND COMPARISON WITH PRIOR ART

The ability of the proposed CDC to operate across a wide voltage range without needing any voltage regulation makes it suitable for direct harvesting, in addition to the suppression of any support circuitry that is conventionally needed by CDCs.

Fig. 11 shows the power consumed by the proposed CDC versus the harvested voltage provided by a commercial 1-mm^2 solar cell [23]. The 0.3-0.6 V voltage range in the x-axis

Fig. 8. Error vs. (a) temperature, (b) supply voltage (down-counter preset M=32, with and without calibration).
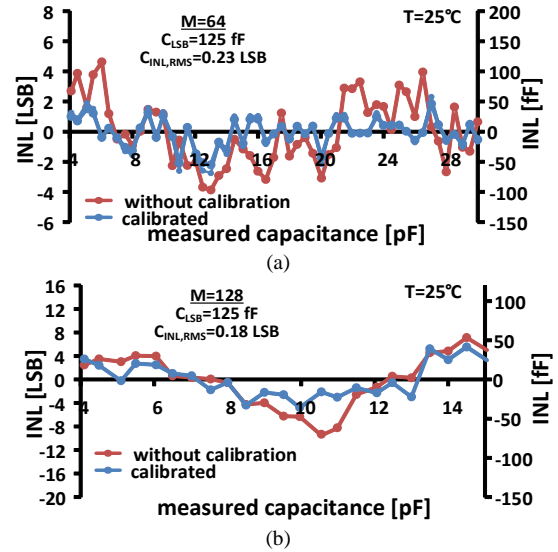

(a)

(b)

Fig. 9. Integral non-linearity (INL) at 25 °C and 0.3-V supply with and without calibration with M pre-set at (a) 64, (b) 128.
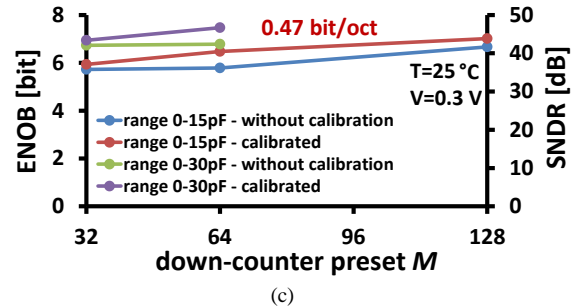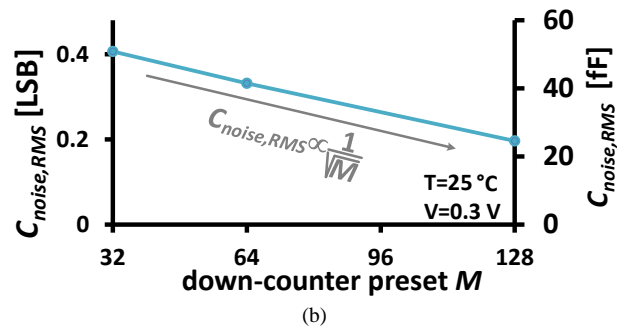

(a)

(b)

(c)
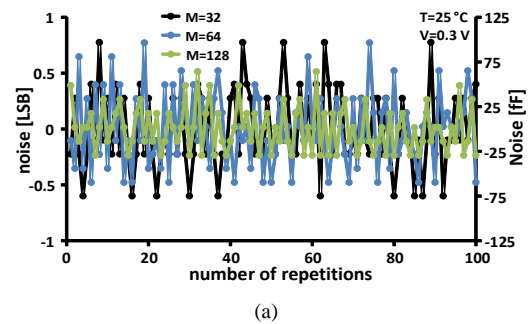
Fig. 10. (a) Noise characterization across readout repetitions for different preset values of M (25 °C, 0.3 V), (b) resulting RMS error due to noise vs. M, (c) resulting ENOB and SNDR with and without calibration,

ERROR VS SUPPLY VOLTAGE

(a)

ERROR VS TEMPERATURE

(b)

corresponds to indoor light conditions from 10 to 500 lux, i.e. from near-dark to bright. From Fig. 11, the CDC power consumption expectedly increases with the supply voltage.
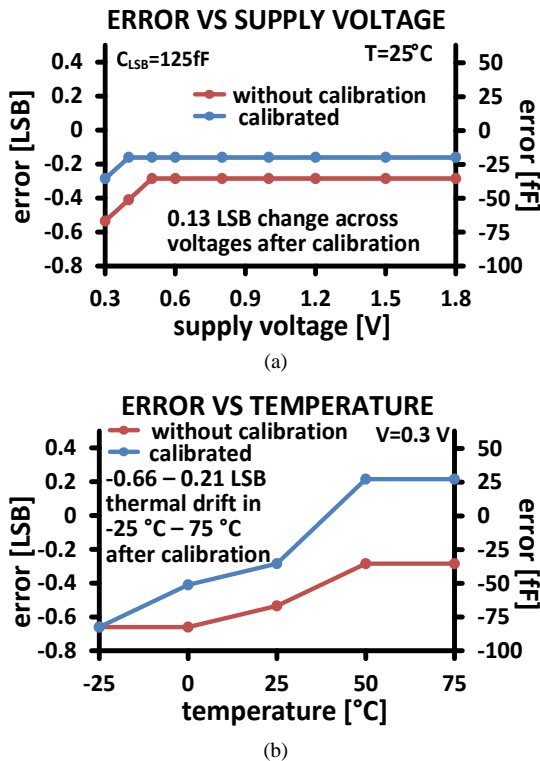
Such an increase is roughly linear, rather than the quadratic trend that would be expected from CMOS logic. This is explained by the adoption of DLS logic for oscillators, counters, and control logic in Figs. 2a-3, whose power is nearly voltage-independent [22] even if swapped biasing is adopted as in Fig. 3.

Fig. 12 confirms a nearly-linear dependence of the CDC peak power (i.e., nearly voltage-independent supply current) on the supply voltage across the entire 0.3-0.18 V voltage range that it can operate at. Such graceful near-linear CDC power dependence on its supply voltage assures sustainable operation across environmental conditions. As an example, Fig. 12 shows the available harvested power versus its voltage over a wide range of light intensities, and the resulting peak power consumed by the CDC using the above solar cell as sole energy source and supply. From this figure, the power available from the harvester grows much faster and is hence higher than the CDC power when the harvested voltage grows, and hence at higher light intensity. In particular, the harvested power is well above the CDC peak power at any practical lighting condition, starting from very dark (10 lux) and up to sunlight.

At any practical indoor light intensity (i.e., 10-500 lux), from Fig. 13 the harvested voltage varies from 0.3 V to 0.6 V, and the CDC power varies increases from 1.37 nW to 6 nW. Within the same environmental conditions, the CDC operates with consistent ENOB between 6.71 and 7.18 bits, as evidence of its ability to operate under direct harvesting without any voltage regulation.

The measured conversion time in Fig. 14a is expectedly proportional to the measured capacitance C_X and the down-counter preset M. At $M=32$, the maximum conversion time for the largest considered capacitance of 30 pF is 1.04 s. Although
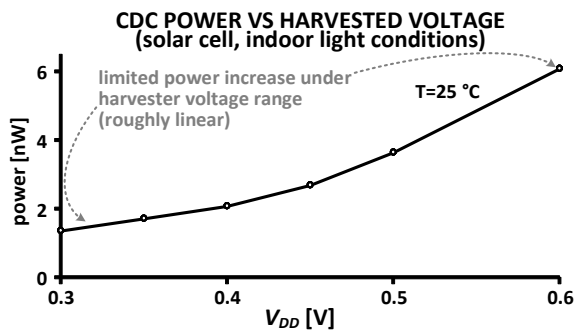

Fig. 13. Harvested voltage and resolution of CDC vs. light intensity harvested by a 1-mm^2 commercial solar cell powering the CDC directly (no intermediate DC-DC conversion).

(a)

(b)

(c)
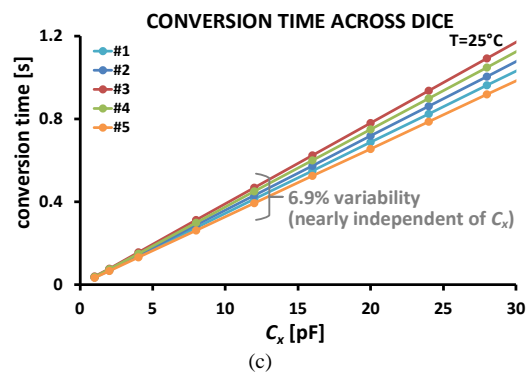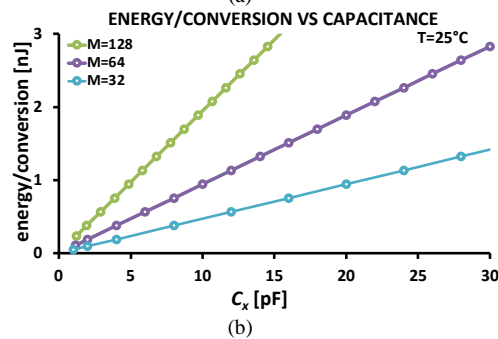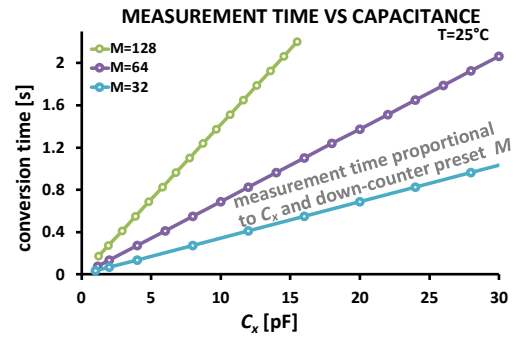
Fig. 14. (a) Conversion time vs. capacitance and (b) energy/conversion vs. capacitance ($M=32, 64, 128$). (c) Conversion time vs capacitance across dice.

Fig. 11. CDC power vs. supply voltage coming directly from a 1-mm^2 solar cell.

Fig. 12. Measured CDC power vs. V_{DD} derived from a 1-mm^2 solar cell.
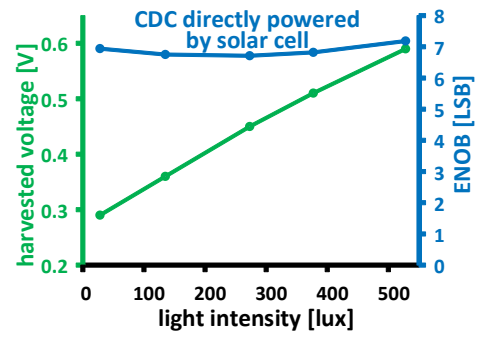
the 1.37-nW power is the correct metric to evaluate the consumption in purely-harvested systems, for completeness the resulting maximum energy per conversion is 1.42 nJ as shown in Fig. 14b, and again it linearly depends on both C_X and M.

TABLE I. COMPARISON WITH STATE-OF-THE-ART CDC (BEST PERFORMANCE IN BOLD)

	This work	JSSC'20 [12]	JSSC'20 [15]	SSC-L'20 [18]	JSSC'19 [17]	JSSC'19 [11]	JSSC'17 [13]	VLSI'17 [7]	ISSCC'15 [1919]	ESSCIRC'11 [20]
process [nm]	180	130	40	65	65	180	40	160	40	130
architecture	self-calibrating dual-swapping ring oscillators	PM	Zoom SAR + TDΔΣ	SAR	SAR	ΔΣ + SAR	SAR+VCO	SAR+ΔΣM	iterative discharge	PLL-based
area [mm²]	0.2 (a)	0.14 per channel	0.06	0.00644	0.08	0.76	0.033	0.33 (b)	**0.0017**	0.07
supply voltage [V]	**0.3-1.8(i)**	0.8	1.1/0.6(h)	0.6 / 1	0.6	1.1	1.1/0.6(h)	1.6 - 2	V_{HIGH}=1 V V_{LOW}=0.45 V	0.3
ENOB [bit]	7.0	11.7	12.34	7.7	7.76	11.8	12.1	**18.7**	7.9	6.1
cap range [pF]	0 - 30 (c)	0-20	0-5	0.458-5.886	2.97-7.67	0 -18.12	0-5	0 - 3.8	**0.7-10,000**	6.3-6.6
abs. resolution [fF]	125	2.345	0.29	6.98	6.19	1.24	1.1	**0.0025**	12.3	3.57
max conv. time [ms]	1,040	0.482	0.0125	0.01 – 1,000	0.02	0.85	**0.001**	100	0.019	1
power (d) [uW]	0.00137	8.2 (f)	6.64 (e) (f)	**0.000044 (g)**	0.0001 (f)	3.09 (e) (f)	75 (f)	3.24	1.84 (f)	0.27
energy/conv. [nJ]	1.42	0.235	0.083	**0.00094**	0.0048	2.64	0.075	324	0.035	0.27
SNDR [dB]	44.0	70.3	75.8	48.42	48.6	74.3	64.2	**114.6**	49.7	29.46
energy FoM (d) [pJ/c-s]	11.1	0.079	0.016	0.0043	0.022	0.66	0.055	0.74	0.14	3.94
testing time needed for calibration	NO (one-time self-calibration)	2-point calibration	YES	2-point calibration	3-point calibration	YES	NO	NO	NO (self-calibration)	NO
current reference needed	**NO**	YES	YES	NO	NO	YES	NO	NO	NO	NO
voltage regulation needed	**NO**	YES	YES	YES (2 supplies)	YES	YES	YES (2 supplies)	YES	YES (2 supplies)	YES
linearity digital correction needed	**NO**	NO	NO	YES	NO	NO	NO	NO	NO	NO

(a) Area assuming that the self-calibration procedure is executed by an on-chip microcontroller (otherwise custom self-calibration block would add 0.3 mm²),   (b) Whole readout, including voltage and temperature readout,   (c) Tested from 2pF onwards, due to testing setup parasitics (usual capacitive offset adding to the capacitance being digitized),
(d) In the considered applications, power (not energy FoM) is the relevant metric for consumption, since the harvester limits the instantaneous power,   (e) Power does not include current reference,   (f) Power does not include voltage regulation   (g) Power does not include linearity correction in the order of nWs (in 65nm LP process with HVT transistors, a single 8-bit adder/comparator has a leakage power of ~1nW)
(h) Analog/Digital supply, (i) Results in the table refer to nominal 0.3V supply.

More in general, the CDC energy efficiency figure of merit[4] (FOM) measured in swapped mode is 11.1pJ/c-s for the measurement time (1s) corresponding to the very worst case (i.e., largest input capacitance of 30 pF). For completeness, the conversion time across dice is shown in Fig. 14c, from which the post-calibration variability is found to be nearly independent of C_x and equal to 6.9%. Such variability is lower than the intrinsic 16% variability of the uncalibrated CDC since the proposed self-calibration in Fig. 4a adjusts the fastest oscillator and hence adds calibration capacitance to its load. In other words, the self-calibration narrows the conversion time variations by leveling up the lower oscillator time to the higher one, bringing the overall conversion time to the highest of the two native ones. This leads to a smaller variability as the maximum value of a set of equally-distributed random variables has a smaller variability than each variable itself [24].

It is worth noting that the proposed techniques trades off power and conversion time as in prior CDC architectures, as very low power and minimum supply voltage are achieved at the cost of longer conversion time. In particular, the proposed self-calibrating and mostly-digital architecture and the introduction of dual-mode logic reduce the minimum voltage and the static power below prior art (i.e., below the minimum voltage of CMOS logic, and below intrinsic transistor leakage). Compared to state-of-the-art low-power CDCs in Table I, the proposed CDC is uniquely able to operate across the voltage range from 0.3 V to 1.8 V without any voltage regulation. This range is wider than the widest [7] by 3.75×, whereas all other CDCs require a precise supply voltage considering both Table

I [11]-[13], [15], [17]-[20], and the broader prior art [9], [27]-[37] in Fig. 15 (i.e., no supply voltage fluctuations are considered or allowed). This unique property of the proposed CDC allows to suppress any voltage regulation within the above wide range and eliminates its additional power (not accounted for in all prior art), as evidenced by the above CDC characterization under direct harvesting with a 1-mm² solar cell from very dim light (10 lux) to sun light. At the same time, the minimum supply voltage of 0.3 V is as low as the lowest [20] (although it consumes a power that is 197× higher than the proposed CDC), 2-5.3× lower than [9], [11]-[13], [15], [17]-[19], and the lowest reported to date [27]-[37], as summarized in Fig. 15.

As summarized in Fig. 15, the proposed CDC has the lowest peak power of 1.37 nW after the two sub-nW average power in [17] and [18], being lower than all others in Table I by 1,343-54,740× [7], [9], [11]-[13], [15], and by 80-10.8E6× compared to broader prior art [27]-[37]. As opposed to CDCs in Fig. 15 and in Table I, the proposed CDC is the only one that does not require any support circuitry such as voltage regulation (see above), current reference circuitry, and digital output linearization, preserving true total nW power at the system level (extra power contributions are generally not reported in prior art). At the same time, from Table I the proposed CDC requires no testing time for trimming, thanks to the any-time self-calibration scheme in Section IV (again, without any extra reference).

From Table I, the maximum conversion time up to 1 s is in line with CDCs with power at the lower end of the range in Fig. 15 [18], or higher (e.g., [12]). The resolution is also in line with

[4] The energy efficiency FOM for CDCs is commonly defined as the energy per

conversion divided by 2^{ENOB}.

prior CDCs [9], [17], [18], and higher than other ultra-low power CDCs [34], [20]. In terms of other common CDC metrics, the energy FOM is significantly higher than other CDCs. However, this does not represent a disadvantage for the harvested systems targeted in this work, as their availability is purely determined by peak power rather than energy [1], and hence the above considerations on true-nW power apply.

VII. CONCLUSIONS

In this work, a relaxation oscillator-based CDC suitable for direct harvesting from mm-sized energy harvesters has been presented. Operation at nW power with unregulated supply down to 0.3 V is achieved through double-swappable oscillators in dual-mode logic with swapped biasing. An any-time load-agnostic self-calibration scheme has been introduced to suppress oscillator mismatch without requiring any testing-time trimming, any specific or accurate extra reference (either capacitance, current or frequency), and without having to disconnect the capacitance.

As opposed to prior art, the proposed CDC suppresses the need for any voltage regulation, current reference or digital post-processing, thus achieving true nW-power self-contained operation. The CDC under direct harvesting and nearly-constant resolution has been demonstrated with a 1-mm^2 light harvester under the wide light intensity ranging down to 10 lux.
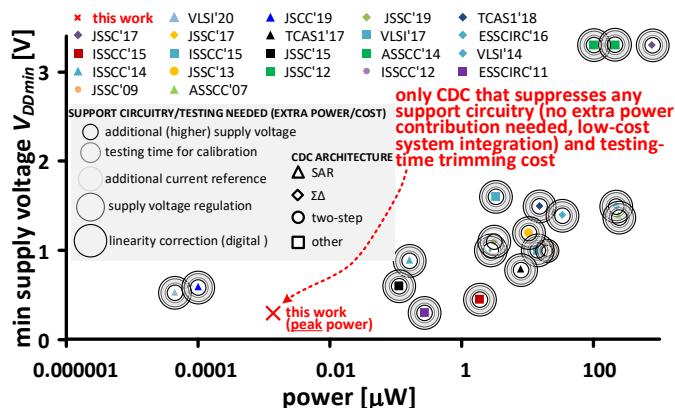
ACKNOWLEDGEMENT

Fig. 15. Minimum supply voltage vs. power in prior CDCs, and classification based on architecture type and necessary support circuitry (extra power).

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