Compact GaN-based Stacked Cells for 5G Applications at 26 GHz

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A. Piacibello, C. Ramella, V. Camarchia, M. Pirola
Dept. Electronics and Telecommunications, Politecnico di Torino, Torino, Italy
and Microwave Engineering Center for Space Applications (MECSA), Roma, Italy
e-mail: {anna.piacibello, chiara.ramella, vittorio.camarchia, marco.pirola}@polito.it

***Abstract*—This work presents the development of two 2-FET stacked cells at 26 GHz in the WIN Semiconductors 150 nm power GaN/SiC technology. Two different compact layouts, based on the same circuit scheme, are designed targeting similar performance in the FR2 5G frequency band. One version favoring distance between components, to relieve electromagnetic cross-talk, and the other favoring instead symmetry. The cells have been conceived as basic building blocks for the development of high-power 5G amplifiers, rather than as stand-alone amplifiers, hence including only input matching and stabilization networks. Based on large-signal simulations on the optimum load, the cells are expected to deliver around 34 dBm with an efficiency higher than 35% at 26 GHz, and a linear gain of 10 dB. The output power performance is maintained from 24.5 GHz to 27.5 GHz, where the saturated efficiency is above 30% for both cells. The small-signal experimental characterization results are in very good agreement with the simulations, proving the effectiveness of the electromagnetic simulation setup adopted for all the passive structures, despite the challenges posed by the compact layouts.**

***Index Terms*—5G, GaN, MMIC, power amplifier, stacked.**

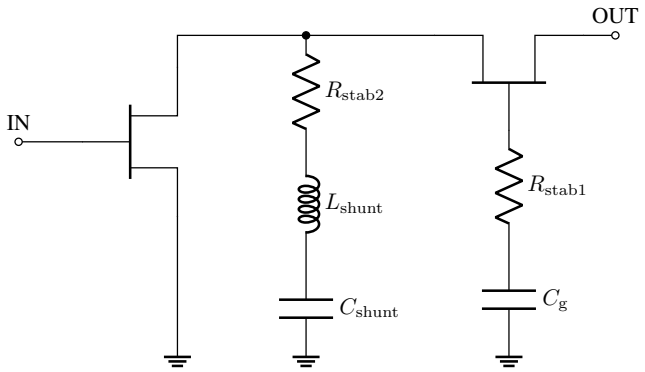
I. Introduction

The present trend toward a highly connected world, with smart devices integrated everywhere and interacting with each other, will result in billions of connections, pushing the communication networks toward unpaved frontiers in terms of capacity, latency, and coverage [1]. This trend is deeply impacting on terrestrial infrastructures, leading to higher mobile cell density, higher carrier frequency, at K-band and above, wider operating bandwidths, together with a wider use of Massive Multi-Input Multi-Output (MIMO) and envelope modulated signals.

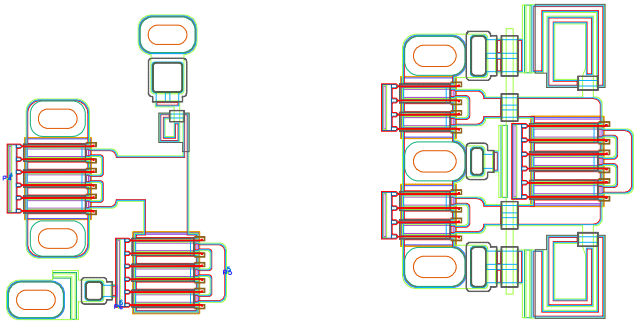
The power amplifier (PA) is known to be a key element in the transceiver, whose design is critical to meet the infrastructure requirements. Reaching the necessary gain and output power levels at millimeter-wave frequencies, with increasingly scaled transistors, is not trivial, especially if the chip area has to be limited. The stacked PA, initially adopted in Silicon technologies [2], [3], is becoming a feasible alternative to the common power combination strategies also for compound technologies, especially Gallium Arsenide (GaAs) [4], [5] but also scaled Gallium Nitride (GaN) [6], [7] processes.

In this paper, we present the design and preliminary experimental characterization of two 2-FET stacked cells designed for 5G applications in the FR2 band. The adopted technology is a commercial 0.15 μm GaN/SiC HEMT process. Two different layouts are adopted, one more compact and symmetric and one with more distance between the various circuit elements and hence affected by a lower degree of crosstalk. The cells are expected to deliver around 34 dBm and efficiency higher than 35% at 26 GHz at 5 dB compression, with a linear gain around 10 dB. Both cells have been validated by small-signal measurements, which are in remarkably good agreement with the electromagnetic (EM) simulations.

This research has been developed within the framework of the "mmWave Multi-Project Runs for Selected Universities" agreement between MECSA and WIN Semiconductors.



(a) Schematic: R_{stab2} is used only in cell V2.



(b) Cell V1. (c) Cell V2.

Fig. 1: RF schematic (a) and layouts (b,c) of the designed stacked cells.

II. Design

The circuit schematic of the designed cells is shown in Fig. 1. A stacked power amplifying cell is composed of a com-

mon source HEMT connected in series (both AC and DC) with one or more pseudo-common gate stages, featuring a finite gate capacitance that allows for impedance matching between stages [8], [9]. At high frequencies, where device parasitic reactances start playing a non-negligible role, additional inter-stage matching elements, AC-coupled shunt inductances in the present case, are also required to achieve proper waveform alignment and power combination [10].

The 0.15 μm power GaN/SiC HEMT process NP15-00 from WIN Semiconductors features a power density around 2.5 W/mm at 20 V drain bias voltage. The process cut-off frequency is around 35 GHz, which is relatively low compared to the target operating frequency of 26 GHz. Since the gain of the common gate stages of a stacked power amplifier is limited by the device's current gain [11], only 2 devices can be effectively stacked at this frequency [12]. As best trade-off between output power, gain, chip area occupation and other layout considerations, a total periphery of 1.2 mm has been determined.

Two different versions of the cell have been developed, as shown in Fig. 1. The first cell (V1) is a more classical solution as it adopts two identical 6x100 μm devices. To enhance layout compactness, they are connected in a L-shape manner as in [13]. Since a possible drawback of this solution may be represented by asymmetry, the second cell (V2) is fully symmetrical. Moreover, instead of one 6x100 μm device, it adopts two 4x75 μm devices for the common source stage, as in [6]. This should allow gain enhancement thanks to the higher gain of the smaller devices, decoupled by the shared via in between. The ultra-compact layout proposed in [5] has been instead avoided since in GaN technology the power levels to be sustained by the inter-stage lines may be incompatible with their implementation with air bridges.

The cells have been both designed considering class-AB bias, with quiescent current set to roughly 10% of the maximum current, that corresponds to around 40 mA for the 6x100 μm device. The total drain bias of the cell was set to 40 V (2$\times$20 V). Device analysis in common source configuration at 26 GHz indicates an output power at 2 dB gain compression around 32 dBm with associated gain around 7 dB and drain efficiency around 50% for the 6x100 μm device with optimum intrinsic load around 65 Ω. The optimum intrinsic load for the 4x75 μm device is instead around 105 Ω and gives 29.5 dBm of output power with about 8.5 dB associated gain, while drain efficiency is also in this case around 50%. The effect of the interconnection lines between the 2 stages has been taken into account for the design of the inter-stage matching network in the 24.5 GHz-27.5 GHz range. Among other solutions, the shunt inductance matching solution [5] proved to be the most effective for both cells. In the symmetric cell version (V2), it is split into two parallel square inductors.

Due to the intrinsic feedback capacitance C_{gd}, the insertion of the gate capacitance impacts on the output reflection. In particular, the optimum value of gate capacitance would yield, for both cells, to a simulated S_{22} higher than 0 dB in the 35 GHz-40 GHz range, where the S_{12} is around -25 dB. To avoid possible stability issues, small (few ohms) stabilization resistances are inserted as reported in Fig 1: in V1 there is only one additional resistance (R_{stab1}) in series to the gate capacitance, while in V2 there is also a second resistance (R_{stab2}) in series to the shunt inductance not to increase too much R_{stab1} as required by parallelization. The resistance values have been selected as best trade-off between stability and gain penalty, which was roughly 1.2 dB for both cells.

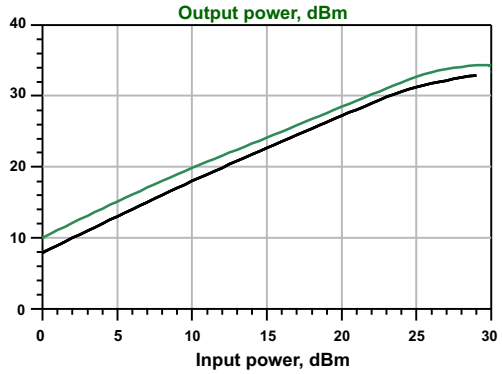
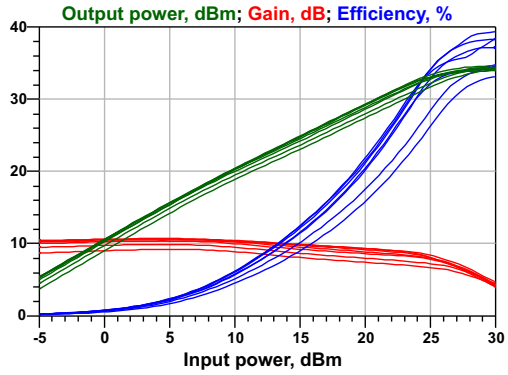


Fig. 2: Output power of cell V1 (green) compared to the output power obtained with a single 6x100 μm device on its optimum load (black) at the center frequency of 26 GHz .

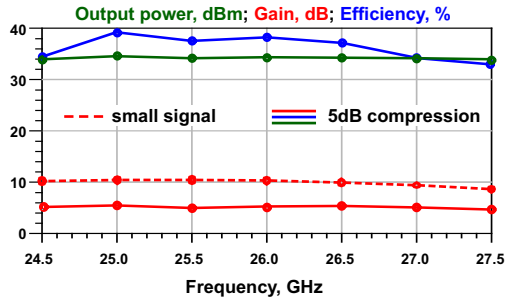
Despite this penalty, proper power combination is obtained by stacking, as shown for example in Fig. 2 for cell V1: with respect to the single common-source stage 2 dB more power is obtained, which is comparable with what can be achieved with parallel combination accounting for combining losses at such high frequency. This verification is not straightforward for cell V2, since the common-source stage is made up by two separate transistor cells with individual non-linear models.

The layouts of the two cells are shown in Fig. 1: their size is below 0.4$\times$0.5 mm^2. All the passive structures have been EM simulated in Keysight ADS Momentum. As can be noted, cell V2 features a more dense structure, which may give rise to coupling issues at high frequency [14]. In fact, cell compactness which, together with layout symmetry, is a key feature of this version, may be strongly compromised by the size of inter-stage matching networks. In this case, in order to provide the necessary AC-coupling without compromising cell size, it was mandatory to adopt a small DC-decoupling capacitor (not a short circuit at the operating frequencies as instead is the case of cell V1) and to share the via-hole of this shunt connection with the via-hole of the common source transistor. Thus, the passive structures have been EM-optimized in two steps: first considering isolated sub-blocks and then refining the results considering the whole network. On the contrary, the sharing of the via-hole in cell V1, which could have been possible leading to an even more compact cell, has been deliberately avoided to ensure weaker EM coupling among the various elements.

Finally, both cells have been provided with an input matching network including stabilization and gate bias lines for both transistors, in order to test the effectiveness of the stabilization

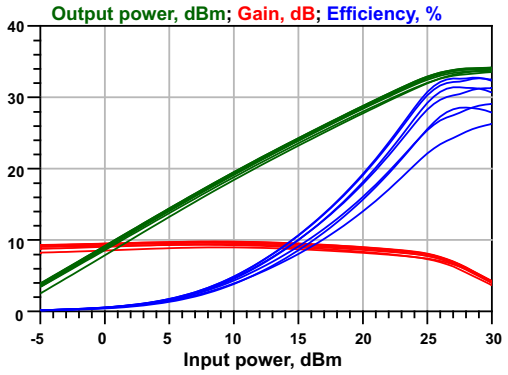


(a) Performance *vs.* input power.

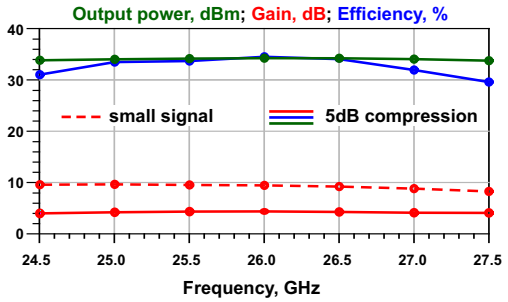


(b) Performance *vs.* frequency.

Fig. 3: Large-signal CW simulation results of cell V1 from 24.5 GHz to 27.5 GHz in 500 MHz steps.



(a) Performance *vs.* input power.



(b) Performance *vs.* frequency.

Fig. 4: Large-signal CW simulation results of cell V2 from 24.5 GHz to 27.5 GHz in 500 MHz steps.

network, knowing that stability of stacked cells may be critical. Cell V2 adopts two separate RC networks for the individual stabilization of the two 4x75 μm devices. Gate bias is supplied from a single side, while RF symmetry is maintained thanks to symmetrical RF shorts at both sides. Although a self-bias approach [15] could simplify bias routing when using the cell within complex architectures, independent bias lines allow for bias tuning and optimization. Based on the characterization results of the cell alone, the most appropriate self-bias network can be then designed if needed.

The cells' outputs are directly (AC and DC) connected to the output pads, since the design of a matching network is out of the scope of cell-level testing. This also allows for possible load-pull characterization, even if the optimum loads required by both cells are in the order of (20+j30) Ω, thus quite challenging to be synthesized at 26 GHz. In fact, synthesizing load impedances corresponding to reflection coefficient magnitudes of the order of the present one ($|\Gamma_{\mathrm{L}}| \approx 0.56$, referring to a 50 Ω system) would require the losses of the overall characterization system, including RF probes, cables and tuner to be extremely low (passive tuners) or a proper active load-pull system able to compensate it.

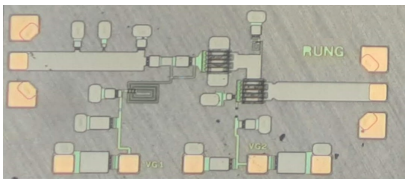
The CW simulation results in the whole design bandwidth, under the assumption of ideal optimum termination at the output, are shown in Fig. 3 and Fig. 4: both cells achieve 34 dBm of output power at 5 dB gain compression and a small-signal gain around 10 dB. The drain efficiency of cell V1 is better (roughly 5 points), but in both cases it is above 35% at center frequency and above 30% in the whole 24.5–27.5 GHz range.

III. Characterization Results

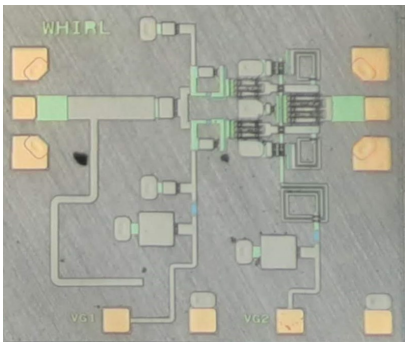
The two designed cells have been manufactured and their microscope picture is reported in Fig. 5.

The cells have been characterized in small-signal with the Keysight E8363C PNA, calibrated adopting on-wafer 2-port Short-Open-Load-Thru (SOLT) calibration. Different bias points, from class-C to the nominal class-AB bias have been tested. For both cells the agreement between simulations and measurements is excellent at all bias conditions, and for a wide dynamic range (remarkably good agreement also for S_{12}), confirming the accuracy of the adopted EM simulation set-up. Fig. 6 and Fig. 7 show the measurement results compared to simulations at two selected bias points, namely the nominal bias $I_{\mathrm{D1}} = 40$ mA and a deeper class-AB bias $I_{\mathrm{D2}} = 5$mA, which correspond to less than 2% of the maximum current.

For both cells the input matching on 50 Ω load results below -10 dB on the whole bandwidth, although the matching network was designed with the optimum power termination. The cells' gain on 50 Ω is clearly lower than that expected on their optimum loads (10 dB for both cells), being around 7.4 dB and 5 dB for cell V1 and V2, respectively.

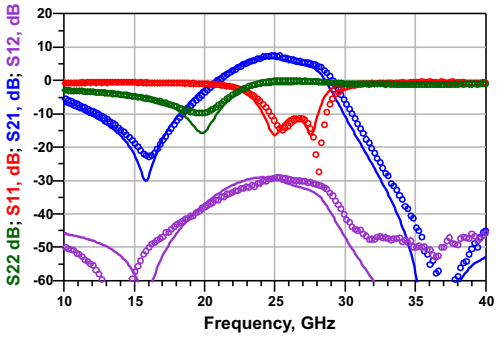


(a) Cell V1.

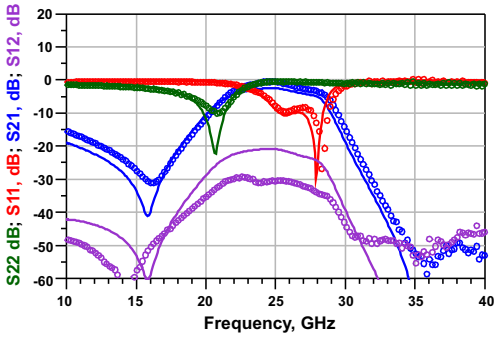


(b) Cell V2.

Fig. 5: Microscope pictures of the manufactured cells.



(a) Nominal bias, $I_{D1} = 40$ mA.

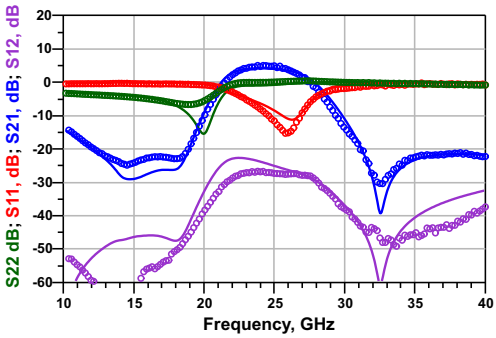


(b) Deep-AB bias, $I_{D2} = 5$ mA.

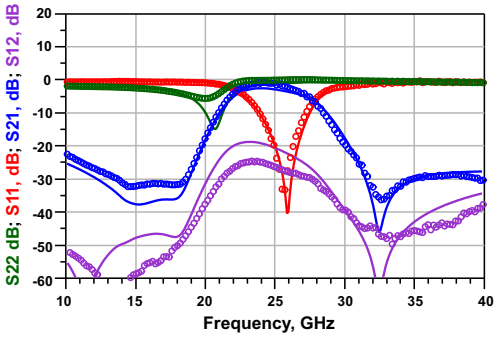
Fig. 6: Measured scattering parameters of cell V1 from 10 GHz to 40 GHz (circles) compared to simulations (solid lines).

IV. Conclusion

This work has presented the design, simulation, and preliminary experimental characterization of two 2-FET stacked cells, with different layouts, targeting 34 dBm output power in the 5G FR2 band. Both cells occupy similar area, which is smaller than $0.4 \times 0.5\,\text{mm}^2$, and exhibit similar measured



(a) Nominal bias, $I_{D1} = 40$ mA.



(b) Deep-AB bias, $I_{D2} = 5$ mA.

Fig. 7: Measured scattering parameters of cell V2 from 10 GHz to 40 GH (circles) compared to simulations (solid lines).

small-signal performance, which turn out to be in very good agreement with the prediction of EM simulations despite the challenging compact layouts. The small-signal gain is around 10 dB over the whole frequency range in both cases. Large-signal simulations on their optimum loads predict that both cells are suitable to provide the targeted output power from 24.5 GHz to 27.5 GHz, while maintaining an associated efficiency higher than 30% at around 5 dB gain compression. These cells are designed to be adopted within more complex PA architectures, such as corporate or Doherty PAs, that will target watt-level operation for 5G applications.

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