Regenerative approaches for V/UHTS feeder links: system analysis and on-board complexity reduction

REGENERATIVE APPROACHES FOR V/UHTS FEEDER LINKS: SYSTEM ANALYSIS AND ON-BOARD COMPLEXITY REDUCTION

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Abstract

The dramatically increasing demand for high data rates necessitates the proper dimensioning of the feeder links of very or ultra high throughput satellite (V/UHTS) systems. However, because most of the current solutions rely on transparent payloads, the deployment of a very large number of spatially separated ground stations is necessary to support the total system bandwidth by enabling a full reuse of the scarce available uplink bandwidth. This approach has a significant impact on the complexity and the costs of the ground segment infrastructure. Regenerative payloads could be considered to avoid this design bottleneck. By allowing demodulation and decoding on-board the satellite, the favourable link budget conditions of feeder links compared to the user links can be exploited. Using a spectral efficient transmission technique, the number of ground stations required to support a target sum throughput can be notably reduced. Meanwhile, regenerative solutions have until now barely been used in V/UHTS payloads due to their high on-board power consumption. As a consequence, candidate solutions are proposed in this work to overcome this limitation. A non-coherent modulation technique, known as Differential Amplitude Phase Shift Keying (DAPSK), is introduced to avoid on-board carrier synchronization. Moreover, polar codes are considered to minimize the power consumption of the channel decoder. A preliminary analysis of the expected on-board power consumption compared to that of a standard DVB-S2 approach is conducted using available results in the open literature. Link performance is also evaluated via numerical simulations.

1 Introduction

The growing demand for high-speed broadband satellite services drives the development of geostationary very/ultra-high throughput satellite (V/UHTS) systems. VIASAT 3, to be launched in 2022/23, and Eutelsat Konnect VHTS, started in September 2022, will, for example, reach aggregated capacities of 1 Tbit/s and 500 Gbit/s, respectively. With the deployment of hundreds of geographically separated Ka-band user beams, where frequency bands are reused, and the introduction of advanced signal processing techniques, capacities exceeding several Tbit/s in the forward link are even deemed feasible in a mid-term perspective [1]. However, this immense traffic load will raise significant challenges for the ground segment design if conventional approaches with a transparent payload are used. Since the available uplink bandwidth is limited (e.g., 5 GHz maximum in the Q/V-band), several tens of spatially separated links with a full reuse of the uplink frequency resources would be necessary to support the aggregated user link bandwidth. A solution to cope with this bottleneck is to transition from transparent to fully regenerative payloads. Benefiting from the favourable link budget in feeder links, this approach would indeed permit to significantly increase the uplink spectral efficiency and, hence, reduce the number of ground stations required to support the data traffic. Meanwhile, the demodulation and the decoding of data streams on-board multi-terabit/s satellites raises immense design challenges.

Regenerative processors have already been developed in the past for satellite missions. A typical illustration of this trend is the REDSAT payload from the Hispasat 36W-1 small geostationary Earth orbit (GEO) mission launched in 2017 [2]. However, attempts to benefit from a regenerative solution remained until now limited to relatively small systems. For example, the REDSAT processor only support 4 × 36 MHz channels using the DVB-S2 standard. The power consumption of this latter processor can easily be covered by the Hispasat 36W-1 platform which delivers around 3 kW to the payload equipment. On the other hand, to cope with the requirements of future VHTS and UHTS missions, tens of wideband carriers (500 MHz or even 1 GHz) will have to be demodulated and decoded in parallel on-board the satellite. The power requirements of such large-scale systems will not be viable if conventional communication standards (e.g., DVB-S2) are used. It is expected that a DVB-S2 regenerative payload would require as much as 5W/Gbps pushing the total power demand for demodulation and decoding in a multi-terabit/s system to more than 10 kW. Research efforts must hence be invested in the development of low-complexity solutions.

In this work, we investigate the potential of the regenerative approach for V/UHTS systems and discuss ways in which the

best trade-off between the on-board power requirements and the achieved spectral efficiency can be found. First, an example of feeder link dimensioning for a UHTS mission is presented in Section 2. Innovative approaches for the on-board digital receiver and the decoder design are introduced in Section 3 and Section 4 to limit the power consumption of V/UHTS regenerative payloads. The performance of the proposed schemes is evaluated and compared to a standard DVB-S2 solution in Section 5. Finally, conclusions are drawn in Section 6.

2 Feeder Link Dimensioning

An ambitious UHTS mission that could represent the type of systems to be developed and deployed in a 5-10 years time horizon is considered. The mission targets a sum throughput of 3 Tbit/s in the forward link which can be achieved via the user link dimensioning shown in Table 1. The assumed bandwidth per beam can be reached if the Ka-band frequencies available for Space-to-Earth connections (17.3 GHz to 20.2 GHz) are entirely allocated to user links whereas feeder links are shifted to higher frequency bands (e.g., Q/V/W-bands). Interference between user links can be mitigated using for example a 2 color scheme with orthogonal polarizations as well as advanced signal pre-processing techniques. However, the detailed design of the user links is not in the focus of this work. The considered scenario is simply an illustrative example used in the following to analyse the feeder link dimensioning. UHTS systems with similar sum throughput requirements can be obtained by tuning the system configuration (e.g., less bandwidth/beam but higher number of beams, use of beam-hopping, ...). However, such changes have no noticeable impact on the main conclusions for the feeder link dimensioning given a target sum rate.

Table 1: User links parameters

Number of active user spot beams	415
Bandwidth/beam	2.9 GHz
User link spectral efficiency	2.5 bit/s/Hz

In the following, the number of gateway stations required to support the defined UHTS mission is now evaluated both under the assumption of a transparent and of a regenerative satellite payload. To this end, the bandwidth allocated to the feeder links must first be fixed. Based on the radio regulations from the International Telecommunication Union (ITU), Earth-to-Space links can be operated in parts of the Ka-band, the Q/V-band and/or the W-band [3]. The dedicated spectrum ranges are summarized in Table 2.

Table 2: Available uplink frequency bands

Ka	27.5–29.5 GHz	Shared / In future, exploited for user links
	29.5–30 GHz	Shared / In future, exploited for user links
Q/V	42.5–43.5 GHz	Contiguous to frequencies for the return link
	47.2–50.2 GHz	Shared
	50.4–51.4 GHz	Shared
	51.4–52.4 GHz	Shared / Allocated after World Radio Conf. 19
W	81–86 GHz	Shared

In view of the current trend, it is assumed that the UHTS mission will allocate the Ka-band resources for the return links between user terminals and the satellite. On the other hand, feeder links will use the Q/V/W-bands for which hardware equipment will be mature enough. However, due to its contiguity with downlink frequencies, the use of the frequency range 42.5 – 43.5 GHz is not considered. As a consequence, a total of 10 GHz is allocated to the feeder links. With two polarizations, a single gateway-to-satellite link will hence offer 20 GHz of bandwidth. In the case of a transparent satellite, whose feeder links have to support the same aggregated bandwidth than in the user links, the number of required gateway stations is then equal to $\lceil 415 \times 2.9\ \text{GHz} / 20\ \text{GHz} \rceil = 61$. This represents a tremendous challenge for the ground segment design especially due to the large number of widely separated gateway deployment sites and the costs of the backbone network infrastructure [4]. Transitioning from transparent to regenerative payloads could help address this issue by enabling a significant increase of the spectral efficiency in the feeder links and, hence, a reduction of the required number of ground stations. The advantage of the regenerative approach relies on the fact that link budgets in the feeder links are much more favourable than in user links due to the use of ground stations with powerful amplifiers and very large reflector antennas. Example link budgets for feeder links in the Q/V- and the W-bands have been computed based on parameters obtained from the specifications of commercial of the shelf products and/or recent research and development projects [5][6][7]. The result of the link budget estimation in clear-sky conditions is provided in Table 3.

Table 3: Link budgets

	@50GHz	**@85GHz**
Bandwidth/carrier	1 GHz	
Amplifier saturation power/carrier	50 W	40 W
Output back-off (OBO)	5 dB	6 dB
Tx antenna diameter	6 m	5 m
Tx antenna efficiency	60 %	
EIRP/carrier	79.7 dBW	80.8 dBW
Miscellaneous losses (depointing,...)	4 dB	
Rx antenna diameter	2 m	1.5 m
Rx antenna efficiency	60 %	
Noise temperature	700 K	
Clear-sky CNR	26.6 dB	25.1 dB
Overall CIR (Intermodulation distortion, inter-beam interference)	25 dB	
Clear-sky CINR	22.7 dB	22 dB

Assuming a clear-sky carrier-to-interference-plus-noise ratio (CINR) of at least 20 dB for the feeder links of future UHTS systems is reasonable. According to the Shannon-Hartley theorem, a regenerative solution with a capacity achieving receiver would then allow to reach a spectral efficiency superior to 6.6 bit/s/Hz. However, a lower average spectral efficiency will be achieved in practice for the two following reasons:

- The frequency bands used for the feeder links are subject to strong rain attenuation effects. Attenuation values well exceeding 10 dB can be encountered. This impairment has to be taken into account in the system design via the

introduction of link margins and smart diversity mechanisms [8].

- Since power consumption on-board the satellite should be kept as low as possible, a compromise between the maximum achievable spectral efficiency and the receiver complexity must be found. A practical system will not be able to get the full benefit of the high CINR achieved on the link. Nevertheless, despite this unavoidable loss, opting for a regenerative approach can bring a non-negligible spectral efficiency gain compared to a transparent solution as illustrated in the following.

The number of gateways required to support a given target sum throughput T as a function of the uplink spectral efficiency S_u is determined as:

$$\boldsymbol{N = \left\lceil \frac{T}{W_u \times S_u \times P} \right\rceil}, \quad (1)$$

with W_u the available uplink bandwidth and $P = 2$ the number of polarizations per link. The result for the considered UHTS system with a sum throughput of 3 Tbit/s is shown in Fig. 1.

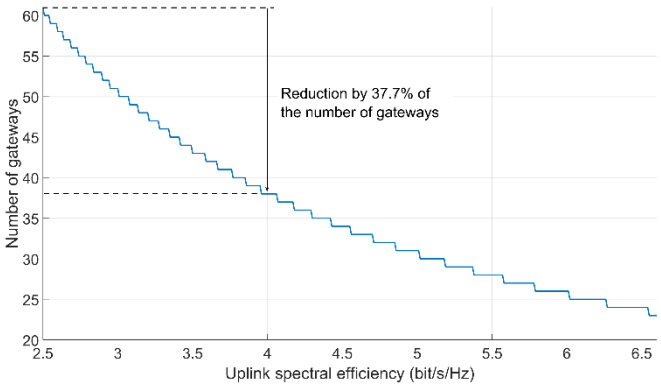

Fig. 1: Number of gateways as a function of the uplink spectral efficiency

In the considered scenario, an uplink spectral efficiency of 2.5 bit/s/Hz corresponds to the performance of a state-of-the-art transparent solution where the spectral efficiency in the feeder link is identical to the spectral efficiency in the user links. Increasing the uplink spectral efficiency from 2.5 bit/s/Hz to 4 bit/s/Hz can already reduce the number of gateways from 61 to 38. This would in this case enable a satellite operator to reduce its expenses for the procurement and the deployment of ground stations by approximately 38%. With the DVB-S2 standard, a spectral efficiency of 4 bit/s/Hz can be guaranteed if the CINR exceeds 14 dB [9] which is well below the clear-sky CINR values obtained in Table 3. However, as discussed shortly in the introduction, implementing conventional DVB-S2 receivers in V/UHTS payloads may entail a tremendous power consumption and alternative solutions must be found for on-board demodulation and decoding. In order to identify what are the most power demanding DVB-S2 receiver blocks, a rough estimation of their contribution to the overall receiver consumption is summarized in Table 4[1].

Table 4: Share of power consumption in wideband DVB-S2 receiver

Frame synchronization	~ 15 %
Phase/Frequency synchronization	~ 20 %
Decoding	~ 40 %
Other	~ 25%

In the following section, approaches are proposed to drastically reduce the complexity of the on-board receiver. Due to the relatively moderate number of links per system, proprietary solutions which are not compliant with the DVB-S2 standard can be envisioned for feeder links. In Section 3, a modulation approach avoiding the need for phase/frequency synchronization at the receiver is considered. Section 4 then presents a solution to reduce the complexity of channel decoding which is the most power-demanding block.

As a final remark, Table 4 shows that frame synchronization is also a non-negligible contributor to the overall power consumption. This is the result of using correlation at the receiver for start of frame detection. The complexity of frame synchronization could be significantly reduced at least partly by a closed-loop synchronization allowing for frame alignment between the gateway station and the receiver. This would shift part of the synchronization complexity at the transmitter side. However, potential approaches aiming at a reduction of the complexity of frame synchronization is not further discussed in this paper.

3 Low-Complexity Digital Receiver

The objective of the following section is the design of a new waveform to reduce the complexity of the synchronization mechanisms for the regenerative payload. We propose non-coherent detection methods to avoid carrier recovery at the on-board digital receiver. Differential amplitude phase shift keying (DAPSK) is introduced for this purpose. The modulation procedure and its performance are thoroughly analysed.

In Fig. 2, the transmission chain for the 64-DAPSK modulation is illustrated. In this case, 6 bits are mapped into a symbol $(b_5, b_4, b_3, b_2, b_1, b_0)$. These bits are split into two paths. 4 of them are mapped into the phase information (b_3, b_2, b_1, b_0), while the other 2 bits are used to map the amplitude information (b_5, b_4). However, unlike non-differential methods, the bits are not mapped directly into the absolute value of the amplitude and phase of the symbol, but rather in the phase rotation $(\Delta\varphi_k)$ and amplitude ratio (ρ_k)

[1] The evaluation is based on the results from [10]. However, only a receiver with a limited bandwidth (1.6MHz) was considered in this latter work whereas synchronization tasks have a higher complexity in wideband receivers. This fact has been considered when extrapolating the values in Table 4.

between two consecutive symbols. The constellation diagram of the 64-DAPSK is illustrated in Fig. 3.

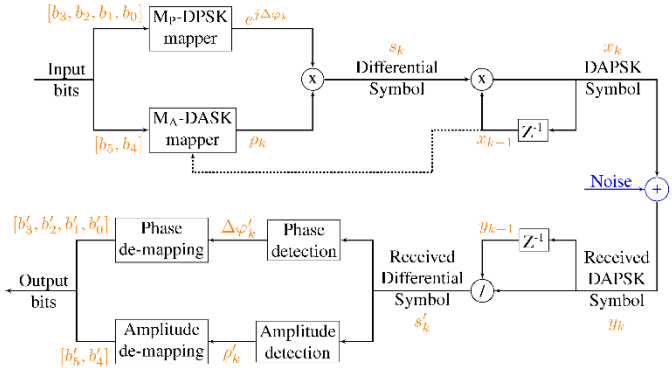

Fig. 2: DAPSK transmission chain

The parameter α denotes the amplitude ratio between the amplitudes of two consecutive constellation circles. α needs to be chosen accordingly, depending on the modulation order and the number of circles. It has been proven in [11] that an amplitude ratio of 1.4 minimizes the uncoded BER of 64-DAPSK. This value is used for the numerical simulations in the following sections.

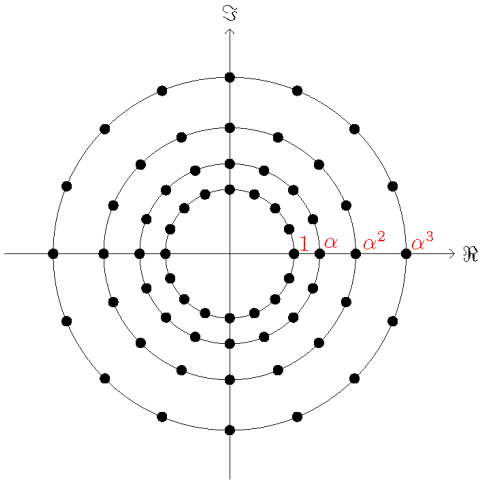

Fig. 3: DAPSK constellation diagram

For the phase, the mapping of the 4 bits follows a DPSK modulation of the order $M_P = 16$. The mapping of the other 2 bits follows a DASK modulation of the order $M_A = 4$. The resulting amplitude ratio is selected based on the previously transmitted symbol (x_{k-1}) and the values of the 2 bits to be transmitted. The mapping rules are illustrated in Table 5 and Table 6 correspondingly. When combined, the phase rotation and amplitude ratio form the differential symbol:

$$s_{k-1} = \rho_{k-1} \cdot e^{j\Delta\varphi_{k-1}}, \quad (2)$$

Afterwards, the DAPSK symbol for transmission is formed by multiplying the differential symbol with the previously transmitted symbol:

$$x_k = s_{k-1} \cdot y_{k-1}, \quad (3)$$

The DAPSK symbol to be transmitted can also be expressed in terms of its absolute amplitude and phase as:

$$x_k = \gamma_k \cdot e^{j\varphi_k}, \quad (4)$$

where, γ_k is the amplitude of the symbol and φ_k is the phase. Combining it with (3), one can rewrite (4) as:

$$x_k = \rho_{k-1} \cdot \gamma_{k-1} \cdot e^{j(\Delta\varphi_{k-1}+\varphi_{k-1})}, \quad (5)$$

Table 5: Phase rotation mapping

$\Delta\varphi_{k-1}$	b_3, b_2, b_1, b_0	$\Delta\varphi_{k-1}$	b_3, b_2, b_1, b_0
0	0 0 0 0	π	1 1 0 0
π/8	0 0 0 1	9π/8	1 1 0 1
π/4	0 0 1 1	5π/4	1 1 1 1
3π/8	0 0 1 0	11π/8	1 1 1 0
π/2	0 1 1 0	3π/2	1 0 1 0
5π/8	0 1 1 1	13π/8	1 0 1 1
3π/4	0 1 0 1	7π/4	1 0 0 1
7π/8	0 1 0 0	15π/8	1 0 0 0

Table 6: Amplitude ratio mapping

ρ_{k-1}		b_5, b_4			
		0 0	0 1	1 1	1 0
$\lvert x_{k-1}\rvert$	1	1	α	α^2	α^3
	α	1	α	α^2	$1/\alpha$
	α^2	1	α	$1/\alpha^2$	$1/\alpha$
	α^3	1	$1/\alpha^3$	$1/\alpha^2$	$1/\alpha$

After transmission over the noisy feeder link channel, the received symbol y_k at time instant k is compared with the previously received symbol y_{k-1}. This results in the received differential symbol s'_k which contains the received amplitude ratio factor ρ'_k and the phase rotation $\Delta\varphi'_k$. For the sake of simplicity, they are detected in two separate paths (however, joint detection is also possible) and, in the end, de-mapping generates 4 bits from the phase information (b'_3, b'_2, b'_1, b'_0) and 2 bits from the amplitude information (b'_5, b'_4), which are then combined together.

Since it is a non-coherent modulation technique, DAPSK avoids the need for carrier recovery at the receiver. As a result, the blocks responsible for frequency and phase correction are unnecessary. Thus, the complexity of the synchronization procedure for the receiver is greatly reduced compared to coherent demodulation as in a DVB-S2 receiver. Non-coherent modulation is not DVB-S2 compliant but, as stated in the previous section, this does not represent a critical issue since gateway-to-satellite links do not have to follow imperatively an existing standard and proprietary solutions can be considered.

The performance of the non-coherent DAPSK is degraded compared to a coherent solution. To evaluate the loss, the

performance of DAPSK has been compared with that of its non-differential counterpart, APSK. For this, the mutual information of 64-DAPSK and 128-DAPSK has been determined according to the joint amplitude phase detection (JAPD) method, as explained in [12], and compared to the mutual information of 64-APSK and 128-APSK, respectively. The results are shown in Fig. 4. According to the plot, there is an about 3 dB degradation of 64-DAPSK when compared to 64-APSK for SNR values up to 25 dB. The same degradation is seen for 128-DAPSK when compared to 128-APSK for SNR values up to 30 dB. Accepting this degradation from DAPSK compared to APSK is part of the unavoidable compromise that must be found between the maximization of the spectral efficiency and the on-board power requirements. Even though DAPSK does not have the same performance as APSK for a similar link budget, the spectral efficiency gain brought by a regenerative link with DAPSK can be sufficient to justify the switch from a transparent to a regenerative solution for the feeder links.

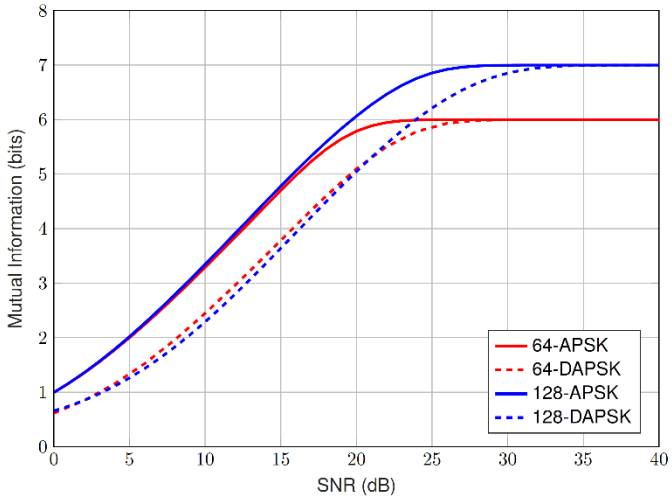

Fig. 4: Mutual Information given SNR for different modulation schemes

4 FEC Complexity Reduction

Here, we compare four state-of-the-art Forward Error Correction (FEC) coding techniques used in digital communications: Polar codes, Low-Density Parity-Check (LDPC) codes, Turbo codes, and convolutional codes. Our comparison is focused on the parameters which are relevant to the satellite application considered.

4.1. General remarks

The implementation complexity and the efficiency of channel decoding have been widely discussed in the literature. While for software implementations the complexity can easily be evaluated in terms of Giga Operations Per Second (GOPS) and amount of data memory used by the application, hardware implementation cannot be assessed as easily. For implementations targeting a Field Programmable Gate Array (FPGA) device, the complexity can be given in terms of occupied resources. However, a typical FPGA device includes several types of internal resources, such as for example Look-Up Table (LUT) units for mapping combinational logic, Flip-Flops to generate sequential circuits, block Random Access Memory (RAM) units to support storage needs, dedicated multipliers, or Multiply and Accumulate (MAC) units. Therefore, the evaluated complexity cannot be associated to a single figure of merit. Moreover, FPGA devices offered by different vendors or belonging to different families do not usually include the same types of internal resources. For silicon implementations, typical complexity metrics are the occupied area and the required number of equivalent gates. The latter depends on the technology size, but it cannot incorporate the contribution of medium to large memories, which must be evaluated separately. On the other hand, the area measure is a simple and comprehensive figure of merit, which captures the complexity of the implementation. However, it depends on the selected technology process and requires scaling factors to compare implementations provided from different processes. The measure of efficiency is even more complex because different types of efficiency can be defined. Two of them are normally of interest:

1. Area efficiency, defined as the ratio between throughput and occupied area (number of decoded information bits per second/area unit).
2. Energy efficiency, defined as the ratio between throughput and dissipated power (number of decoded information bits per seconds/power, or equivalently bits per Joule).

Area and energy efficiency can change dramatically among different implementations of the same decoding algorithm, as can be seen by looking at the works available in the open literature.

Literature comparison campaign

Focusing on the dissipated power of the decoder, we considered many literature results (approximately fifty references in the literature) reporting different implementations of decoders for our four code classes considered. These results are rather scattered and unharmonized so that we had to resort to equivalence relationships in order to compare them. We extracted from the literature results the following data (i represents the literature record):

- μ_i: technology size (nm)
- V_i: supply voltage (V)
- R_i: achievable information bit rate (Gb/s)
- P_i: total dissipated power (W)

Our goal is deriving the relationship between the dissipated power and the achievable information bit rate (or throughput) of the implementation. Thus, we set the following target parameters: $\mu_0 = 45$ nm, $V_0 = 1$ V. We also kept in mind that the throughput of interest for this satellite application is in the order of a few Gbit/s. The dissipated power corresponding to the i-th literature record is obtained by applying the following formula:

$$P_i' = P_i \times \frac{\mu_0}{\mu_i} \times \left(\frac{V_0}{V_i}\right)^2, \quad (6)$$

Fig. 5 reports the data collected in our campaign and contains second-order regression curves in log-log scale of the record data to extrapolate the expected behavior and smoothen the variability of the different implementations. From the analysis of the regression curves we extracted the following considerations.

- Turbo codes dissipate more power than the other code classes, also because they require longer codeword size, so that they seem to be a poor choice when the goal is reducing the dissipated power. From a different point of view, it must be highlighted that Turbo codes offer better flexibility in terms of code rate than other codes.
- LDPC codes tend to increase the dissipated power versus the throughput. Therefore, they exhibit a super-linear behavior which is not desirable if the goal is aggregating several FEC decoders into a single unit.
- Convolutional and polar codes exhibit a similar behavior as far as dissipated power is concerned. However, the error performance of the former is worse, at the same level of complexity, than the latter. This is why polar codes seem to have the best characteristics for this implementation scenario.

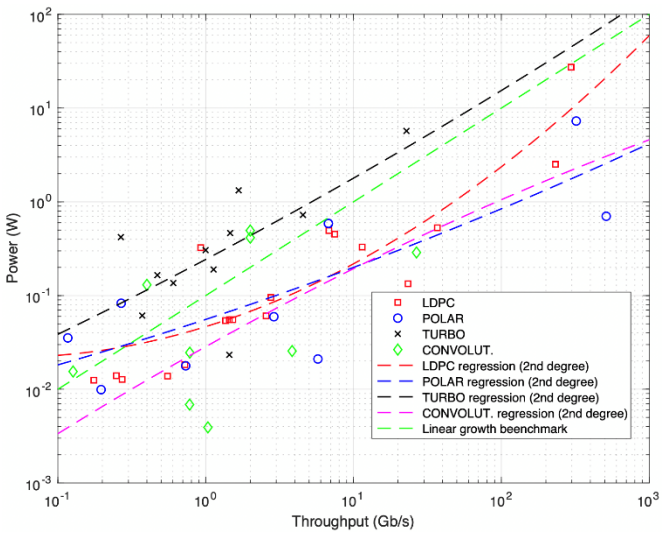

Fig. 5: Dissipated power versus throughput.

The results from this survey are addressed in more detail in the following section, which provides evidence for the optimal choice of the decoder class for our application.

4.2. Comments on the optimal implementations

In this section, we consider three selected implementations for LDPC, turbo, and polar codes, whose details are reported in Table 7.

Table 7: Comparison among the three fastest implementations of LDPC, turbo and polar codes.

		[LI 2021]	[WEITHOFFER 2020]		[KESTEL 2020]	
code		LDPC	TURBO		POLAR	
length		1027	512		1024	
rate		5/6			1/2	
algorithm		layered	max-Log-MAP		SCL (L=2)	
quantization		5	6		6	
iterations		4	2.5			
early stop		yes	yes			
performance		3 dB			4 dB	
application		>5G	>5G		>5G	
architecture		multi-core with pipelining and frame interleaving	fully pipelined iteration unrolled		fully pipelined	
technology		16 nm FinFET	28 nm FD-SOI	16 nm	28 nm FD-SOI	16 nm
implementation		layout	layout		layout	
clock frequency	MHz	1000	800		503	
supply voltage	V	0.8			1	
area	mm2	2.24	30	9.77	7.52	2.46
throughput	Gb/s	833	409.6		516	
latency	ns	38			292	
power	W	6.22			4.53	
area efficiency	Gb/s/mm2	371.9	13.65	41.77	69	211.31
energy efficiency	pJ/bit	7.47			8.79	

Table 7 provides the most important parameters for three high-throughput implementations that have been recently proposed for LDPC [13], turbo [14], and polar [15] decoders. The first part of the table reports communication and algorithm parameters, while the second part gives parameters relateing to the technology and to the implementation. The most important figures of merit are the area, the throughput, the latency, the dissipated power, the area efficiency and the energy efficiency. For the implementations from [14] and [15], the area and the area efficiency have been reported also for the case of a 16 nm technology, by correcting the value available for 28 nm with the scaling factor S, defined as the square of the ratio between the two feature sizes. A similar estimation was not extended to the throughput and power dissipation, as it would not have been accurate. As is clear from the first part of the Table, the comparison is not completely fair, because different codes have been considered and the design choices adopted in the three cases do not lead to the same level of communication performance. However, some comments on these results are in order.

1. First, we notice that, although the implementation reported in [14] was developed for a much shorter code than those presented in [13] and [15], it requires a larger area (30 mm^2 vs 2.24 mm^2 and 2.46 mm^2, respectively, for [13] and [15]), a lower throughput (102.4 Gb/s vs 833 Gb/s and 516 Gb/s) and a worse area efficiency. These results are in fair agreement with a key difference between the decoding algorithms used for turbo and LDPC codes, with the decoding of LDPC codes offering large potential parallelism, easier exploited than for turbo codes. However, as reported in [16], the direct comparison between decoder implementations heavily optimized for a specific code does not take into account the important issue of flexibility. In the case of LDPC and Polar codes, flexibility in terms of code rate is expensive, meaning that a relevant area and energy overhead must be paid to support multiple codes with different code rates. On the

contrary, we can rely on puncturing to provide a Turbo code decoder with large flexibility in terms of code rate and the hardware implementation of puncturing affects the overall complexity only in a marginal way. Therefore, we can conclude that a Turbo code decoder is not the best option if we intend to maximize the decoding throughput for a single code rate. However, if multiple code rates are required, the choice of Turbo codes could be competitive with both LDPC and Polar codes.

2. For the comparison of LDPC and Polar codes, we notice from the table that [15] exhibits a lower area efficiency than [13] (211 against 371 Gb/s/mm^2, which means a 43% difference), but better performance in terms of dissipated power (27%) and energy efficiency (+18%), although the implementation in [15] uses an older technology than [13]. This element suggests that Polar code decoders can be the best choice for energy critical implementations. However, we must observe here that the two codes are similar in terms of length, but rather different from each other in terms of code rates. The dissipated energy is definitely affected by the code rate and even more importantly the communication performance (i.e. the achievable Bit Error Rate (BER) or Frame Error Rate (FER)) strongly depends on the code rate. Therefore, no direct conclusions can be drawn from this comparison and more investigations are necessary to compare high speed implementations in a fair way.

5 Complexity and Performance Assessment

5.1 Performance analysis

To evaluate the error performance of the proposed Polar Codes, simulation modules supporting the 64-APSK and the 64-DAPSK modulations were developed. Concerning the 64-APSK modulation, which is standardized in the DVB-S2 standard, the ring ratio was optimized for the code rate 5/6 and a soft-output demapper generating log-likelihood ratios was used. For the 64-DAPSK modulation, the constellation parameters presented in Section 3 have been considered and the calculation of the log-likelihood ratios (LLR) in the demapper was based on the JAPD method, as explained in [12]. In Fig. 6, the results of the error performance for the 64-APSK are illustrated. Additionally, Fig. 7 shows the error performance results for the 64-DAPSK modulation.

It is important to note that, when compared to the mutual information results in Fig. 4, Fig. 7 suggests a higher performance loss when switching from 64-APSK to 64-DAPSK, 4.5 dB instead of 3 dB. It is believed that this is partly the result of the bit mapping procedure (explained in Section 3), which for the scenario at hand has not been optimized. In a future study, the further optimization of the DAPSK modulation (amplitude ratios and bit mapping) would help to reduce this gap.

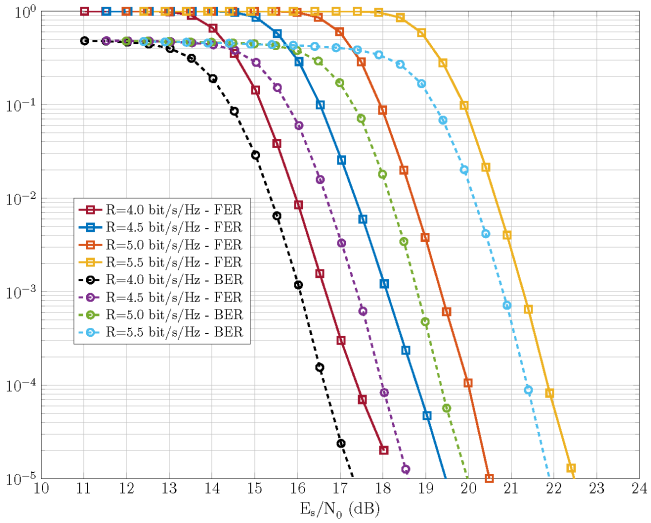

Fig. 6: Error performance of DVB-S2X compliant 64-APSK modulation with Polar encoding over the AWGN channel.

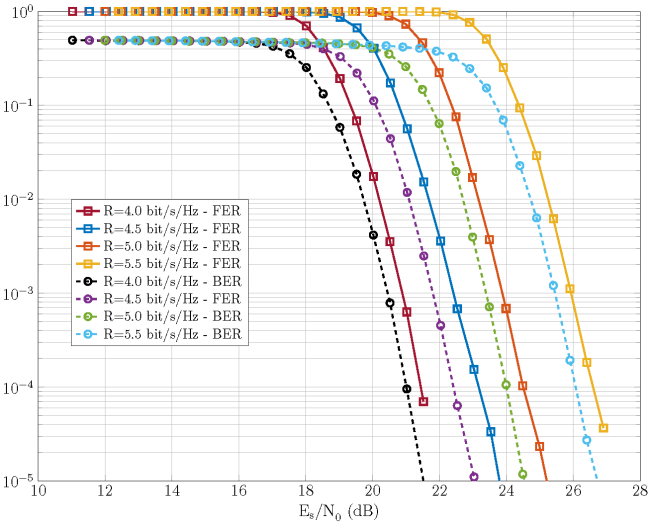

Fig. 7: Error performance of the 64-DAPSK modulation with Polar encoding over the AWGN channel.

5.2 Complexity reduction

This section reports a preliminary analysis of the expected reduction of the power consumption on-board the satellite if the proposed polar code and the non-coherent DAPSK are used to limit decoding complexity and avoid on-board carrier recovery, respectively. The comparison is done with respect to the estimated share of power consumption in a wideband DVB-S2 receiver presented in Section 2.

First, replacing the DVB-S2 LDPC code by a polar code in the communication chain can bring an up to 80 % power consumption reduction of the channel decoder block. This estimation has been obtained via the extrapolation of claimed power consumption values found in the open literature discussed in Section 4. We recall that channel decoding

accounts for around 40 % of the total power consumption of a wideband DVB-S2 receiver.

Concerning the synchronization procedure, the carrier recovery blocks (frequency and phase correction), which represent approximately 20 % of the power consumption in a standard wideband receiver, are completely avoided.

In total, a close to 50 % power reduction can hence be expected from the proposed regenerative solution compared to state-of-the-art DVB-S2 implementations reported in the open literature.

The result presented in this section is obviously a high-level estimation and relevant additional efforts that include the development of hardware models for the most power-hungry units are needed to understand to which extent the power reduction justifies the development of a new air interface for feeder links.

6 Conclusion

In this study, the benefit of a regenerative solution for the dimensioning of feeder links has been evaluated given certain constraints on the available uplink frequency resources and the expected link quality. By taking advantage of the favourable link budget in feeder links, regenerative payloads allow for a significant increase in the uplink spectral efficiency. However, their deployment has until now been limited by their high on-board power consumption. Novel modulation and coding strategies have hence been studied in this work to find a trade-off between the maximization of the spectral efficiency and the on-board power consumption. The promising results presented in this work should be completed in future by hardware models to obtain more precise predictions of the expected reduction of the power consumption compared to a state-of-the-art DVB-S2 receiver.

7 Acknowledgements

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