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Gallium Nitride Power Amplifiers for Ka-band Satcom Applications: Requirements, Trends, and The Way Forward

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Introduction

The current trend in satellite communications is moving towards high carrier frequencies and complex modulated signals, which have a non-constant envelope, such as Quadrature Amplitude Modulation (QAM) and Orthogonal Frequency Division Multiplexing (OFDM) [1]. This trend has a significant impact on the design of the transmitter and in particular of the Power Amplifier (PA) from both the energy consumption and linearity standpoints. Energy-efficient PAs are crucial for reducing the cost of satellite transmitters. Poor efficiency can negatively impact power budget, thermal design, and weight.

Satellite transmitters typically require power levels on the order of hundreds of Watts [2], which were once only compatible with Travelling Wave Tube Amplifiers (TWTAs). Over the last decades, the availability of reliable Gallium Nitride (GaN) technologies, which are characterized by higher power density than most other semiconductor alloys, has triggered interesting research activities,

demonstrating that solid-state technology can also become an attractive solution for space. However, nowadays a single GaN Microwave Monolithic Integrated Circuit (MMIC) High-Power Amplifier (HPA) in the Ka-band rarely exceeds 40 dBm of output power [3, 4, 5, 6] and combination techniques are mandatory to achieve the specified Effective Isotropical Radiated Power (EIRP) at satellite level. This can be accomplished by feeding an individual or a few antennas' elements with one MMIC, thus realizing an active antenna array with hundreds of elements [7], or by using spatial combining techniques to implement Solid-State PAs (SSPAs) with output power levels comparable to those of TWTAs, to feed a single or a few antennas [8]. Both solutions have pros and cons in terms of thermal management, mechanical design and assembly, weight, electrical performance, and earth coverage flexibility. Consequently, the choice between them is usually dictated by the specific requirements of the mission/services for which the satellite is conceived.

One factor that poses major design challenges is the fact that the PA must be able to operate efficiently not only at saturation, as in past satellite systems based on constant envelope signals, but also in output back-off (OBO), which is a relatively new requirement for this kind of application. Signals with a large peak-to-average power ratio (PAPR) necessitate OBO operation of the PA to avoid clipping and strong non-linear effects on transmitted signals. On top of that, linearity is crucial and the PA should maintain the required level as much as possible to minimize the need for additional linearity recovery blocks. This is essential to keep the complexity of the system to a minimum, which is of paramount importance for satellite systems. Traditionally, the two-tone Third-order Intercept Point (IP3) has been used to evaluate the linearity behaviour of the PA. However, with present wide-band complex signals, more robust figures of merit like Noise Power Ratio (NPR) [9] are assuming an increasingly prevalent role. Often, the target requirements for power, efficiency, and gain of the PA are provided by the end-user to the designer at a minimum degree of linearity (most often NPR).

While power back-off can improve linearity, it also reduces the average efficiency and Power-Added Efficiency (PAE) of the PA. This is because the PA is forced to operate with reduced voltage swing, thus increasing the portion of power dissipated by the active devices.

Furthermore, reliability is of paramount importance, which entails both the availability of consolidated MMIC technologies and particular care during the design to keep the active devices working in conservatively safe regions. The latter often involves applying de-rating [10, 11] and monitoring the junction temperature to preserve the lifetime and, consequently, the overall reliability of the system.

The combination of these contrasting requirements makes it challenging to identify a winning solution from a design standpoint. Corporate PAs with combined structures, often balanced, can provide the required power levels with good saturated efficiency and acceptable intrinsic linearity up to the Ka-band. However, popular solutions at communication frequencies (below 6-GHz), like the Doherty PA (DPA), may be possible competitors thanks to their higher average efficiency with modulated signals, even if typically with more complex features and lower intrinsic linearity.

Environment: Space vs. Earth

There is a crucial difference between Earth and space environments that needs to be carefully accounted for during the PA design phases. Indeed, the absence of an atmosphere in space makes the thermal management of the electronic components challenging, due to the lack of conduction and convection mechanisms. Heat sinking methods, such as fans and liquid cooling, which form the basis of solutions adopted in ground applications to remove excess heat, are less practical in space due to the absence of air and the challenges of managing liquids in micro-gravity. Thus, engineers need to devise innovative cooling solutions, like heat pipes or thermal radiators, to manage heat effectively.

Efficient thermal management is essential to ensure the reliability and performance of electronic components. This is especially crucial for PAs since, despite the potentially high efficiency, a large amount of power is dissipated in a small area, typically a few square millimeters (i.e., the transistor and its immediate vicinity). Hence, the thermal assessment of GaN devices is of crucial importance for developing a reliable and robust SSPA [12]. Finally, a vacuum can trigger destructive phenomena such as multipaction and corona discharges which can jeopardize the overall mission. Therefore thermal and vacuum cycles are essential experimental tests to be carried out on every space-borne piece of equipment.

GaN is the answer

In terms of attainable output power, there is no doubt that GaN is superior to other solid-state technologies such as GaAs and SiGe. Its higher energy gap (3.42 eV, versus 1.42 eV for GaAs) is also beneficial in terms of radiation hardness, which is fundamental in space-borne applications. Consequently, GaN devices can operate at higher drain voltage, up to 24 V for Ka-band applications, which significantly simplifies the implementation of the on-board dc/dc converters, while offering easier matching to 50 Ω over a wider bandwidth [13]. On the other hand, GaN HEMTs suffer from so-called low-frequency dispersion [14, 15, 16], which is related to the presence of thermal and charge-trapping phenomena that reduce the achievable performance in terms of output power and efficiency at the transistor level. At the PA level [17], these effects limit the maximum instantaneous video bandwidth where the satellite spectrum emission mask limits are met. Therefore, particular care should be devoted to the optimization of the nonlinear response of the amplifier when complex modulations are adopted.

Currently, there are two options available for GaN processes: Silicon Carbide or pure Silicon substrate. Gallium Nitride on Silicon Carbide (GaN-SiC)

has already proven to be the most effective semiconductor platform for realizing high-power and efficient PAs for microwave frequencies, thanks to SiC's superior thermal performance. However, pure Silicon (GaN-Si) can provide an interesting alternative in some cases. GaN-Si allows one to exploit some of the key features of GaN-SiC technologies while offering benefits, such as lower production costs due to larger wafer sizes [18] and, above all, the potential to be integrated with standard CMOS technology[19, 20, 21]. However, it is important to highlight two key differences between GaN-SiC and GaN-Si HEMTs. Firstly, Si has about twice the thermal resistance of SiC, which imposes a different limit on maximum dissipated power and, consequently, on the achievable RF power density for the same active periphery. Secondly, the losses of passive structures, particularly transmission lines, are higher in GaN-Si compared to those in GaN-SiC. In light of these factors, the use of GaN-Si technology can be favorable for implementing PAs at significantly higher frequencies, such as above the Ku-band, where distributed matching elements have relatively small dimensions, and provide RF power of 8-10 W at the chip level.

Unity is strength

On the other hand, regardless of the adopted GaN technology, the RF power achievable at the chip level is not enough to satisfy the needs of today's high-throughput GEO satellites, and thus combining techniques are mandatory. A simplified way of looking at this aspect has been proposed in [7], where the trade-off between the required output power per PA and the number of radiating elements in an active antenna for a Ka-band satellite downlink is graphically illustrated. From that work, reproduced here in Fig. 1, one can appreciate the inverse proportionality that exists between a PA's output power and the number of an antenna's elements for a given EIRP value. For instance, 50 dBW of EIRP can be achieved by using either an antenna array with 30 elements, each of which is fed by a PA with 38-40 dBm output power, or with an array of 6-7 elements, each of which is fed by a 50 dBm PA.

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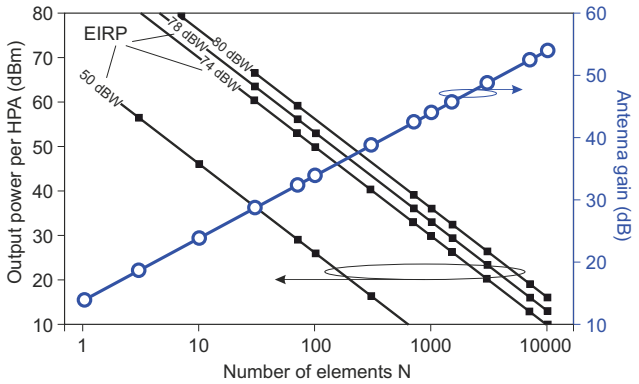

Fig. 1: Relationship between the required output power per HPA and the number of radiating elements in an active antenna for given EIRP values for a Ka-band satellite downlink. The highest EIRP levels are estimated for high-throughput satellites with capacity larger than 100 Gbps. For simplicity, the antenna gain of a single radiating element is assumed to be 14 dB (MMIC-antenna interfaces, efficiency, and element spacing trade-offs are not considered)[7].

Wide bandgap semiconductor technologies are rapidly advancing, achieving power densities of several watts per millimeter with pretty good efficiency and gain at the device level. However, a single MMIC PA is still very far from what vacuum technology can provide in terms of absolute power levels. Such a gap can be filled by collecting the output power of several MMIC HPAs using spatial combining techniques [8, 22, 23, 24] or by exploiting active integrated antennas techniques. These two alternative approaches are graphically depicted in Fig. 2. On the left, the hollow triangles represent individual MMIC PAs, with a generic architecture, each feeding a dedicated antenna. On the right, the power generated by analogous individual PAs is combined to feed a single antenna. The additional output blocks represent a coupler connected to a power detector, followed by a circulator, to detect and possibly correct for mismatch. At the input, a Gain Control Unit (GCU) and a driver complete the system architecture.

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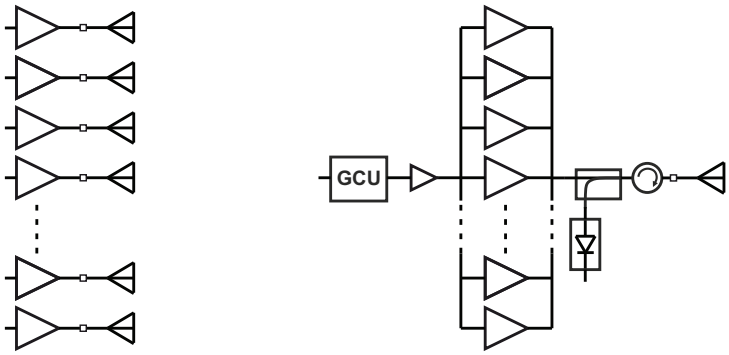

Fig. 2: Block diagram of an active integrated array (left) and an SSPA (right).

Architectures

Two architectures are primarily used to implement an individual MMIC PA, namely the more standard corporate class-AB and the recently explored DPA. The former typically relies on the adoption of N levels of 2:1 combiners to combine the power of 2^N identical transistors, all equally biased in a class-AB bias point suitable to the application. Other implementations adopt 4:1 or, in general, N:1 combiners. A generic block diagram of a corporate PA based on 2:1 combiners is shown in Fig. 3 together with its typical efficiency behavior as a function of the OBO. The amplifier is only maximally efficient at full power, and its efficiency drops with the square root of the output power.

The DPA is a popular architecture originally proposed by W.H. Doherty in 1936 [25] for vacuum tubes. It has since been adapted for solid-state technology with the introduction of complex modulated signals in various communication systems, mainly below 6-GHz. The DPA operates by modulating the load impedance presented to the active device, known as the Main or Carrier, which is typically biased in class AB. This is achieved using a second active device, the Auxiliary or Peaking, typically biased in class C.

The basic implementation of the DPA and its theoretical normalized efficiency versus OBO are illustrated in Fig. 4. At low input power levels, only the Main device is active while the Auxiliary device remains off. As the input

power increases and the Main device approaches saturation in terms of maximum voltage swing, the Auxiliary device turns on and starts modulating the load seen by the Main device. To maximize efficiency in the high-power region, an Impedance Inverting Network (IIN) is inserted between the Main device's output and the common node to modify the load seen by the Main [26]. In the basic scheme here reported, the Main and Auxiliary deliver the same maximum power and the Auxiliary turns on when the Main reaches half of its dynamics, thus leading to a highly efficient DPA over a 6-dB OBO range.

The IIN can be easily realized by a quarter-wavelength Transmission Line ($\lambda/4$ TL), although other practical implementations could be adopted. Consequently, a $\lambda/4$ TL has to be added at the input of the Auxiliary PA to properly compensate for the phase shift, (i.e., to combine the signals provided by the two devices in phase at the DPA output port). However, one of the main limitations of architectures based on $\lambda/4$ TLs, as compared to Corporate approaches, is the intrinsic bandwidth. This is further exacerbated by the need to maintain a correct load modulation over input power, which requires the synthesis of different impedances at different power levels, and the need for phase synchronization between the Main and the Auxiliary paths, to maximize the delivered power. To counteract this shortcoming, different architectural solutions have been proposed, ranging from the use of alternative combiner structures to dual-input solutions to multi-band approaches and digitally-based architectures [26]. The proposed innovations have demonstrated the possibility of obtaining a consistent back-off efficiency enhancement versus output power over rather wide bandwidths while minimizing the effect on other key aspects, such as linearity and complexity.

Both the corporate and the Doherty architectures typically need to include one or more levels of driver stages to achieve the desired gain target at Ka-band frequencies.

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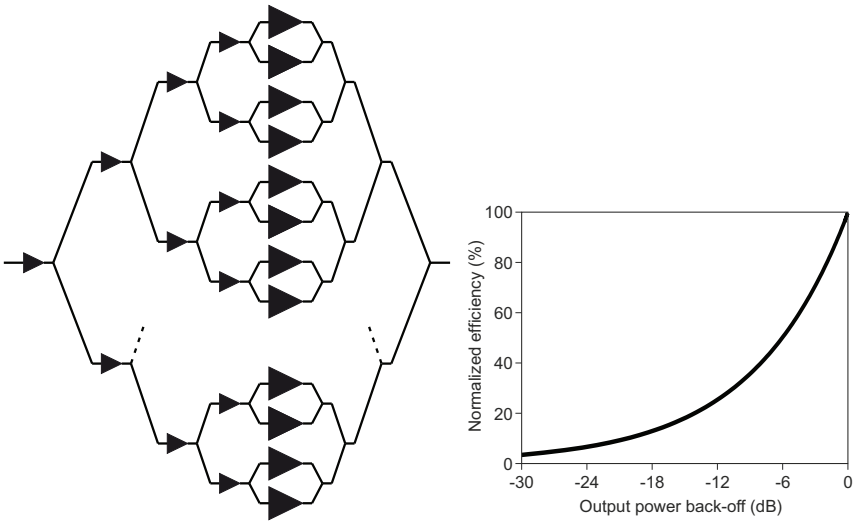

Fig. 3: Block diagram (left) and efficiency (right) of a generic corporate PA.

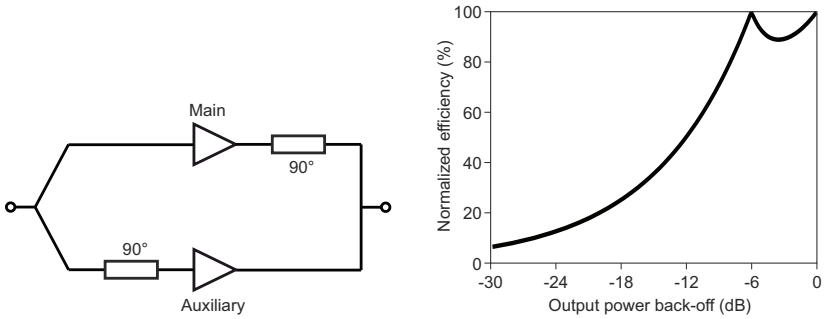

Fig. 4: Block diagram (left) and efficiency (right) of a classical Doherty amplifier.

Corporate PAs

In 2017 Northrop Grumman [3] proposed one of the first examples of K-band satellite SSPAs based on corporate GaN-SiC MMIC PAs. The MMIC PA, used as a unit cell for the assembly of the full SSPA, has 19 dB gain, more than 40 dBm output power, and a PAE of 35% at saturation in the 17.3–20.3 GHz range. It operates at 20 V and has 8 × 8f640 μm devices in the final stage and a single driver stage, see Fig. 5.

To maintain a high PAE, an aggressive 1:4 periphery ratio is used between the driver and the final stage. The SSPA module is composed of two stages, a single MMIC PA as a driver and four MMICs combined in the final stage.

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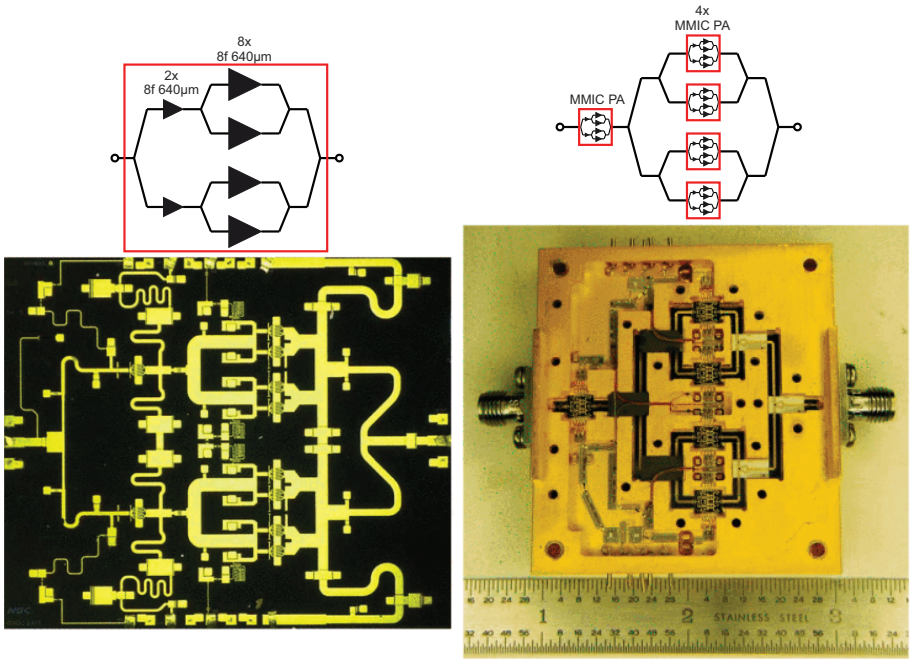

Fig. 5: Block diagram and photograph of the MMIC PA (left) and of the SSPA (right) of [3] ©2017 IEEE.

The saturated power of the modules is approximately 4 dB higher than that of the individual MMIC, which means that the output combiner introduces roughly 2 dB of losses. In fact, with four MMICs combined in parallel, the saturated power of the module should ideally be 6 dB higher than that of the single MMIC. This clearly highlights the crucial role played by the planar power combiner, which negatively affects the PAE (which went down to 20%). To meet the linearity requirement of 15 dB NPR, the output power has to be backed off by 1–1.5 dB.

Another corporate MMIC PA with similar performance was presented in 2019 by United Monolithic Semiconductors [4]. The design, shown in Fig. 6, is developed on the proprietary 0.15 μm gate length GaN-SiC process. The MMIC is then integrated into a hermetic package featuring an output waveguide transition for low-loss spatial power combination in an SSPA module. The packaged PA demonstrates in CW conditions 10 W of saturated output power, with an associated 35% of PAE and 10° AM-PM conversion in the 17.3-20.2 GHz

frequency band.

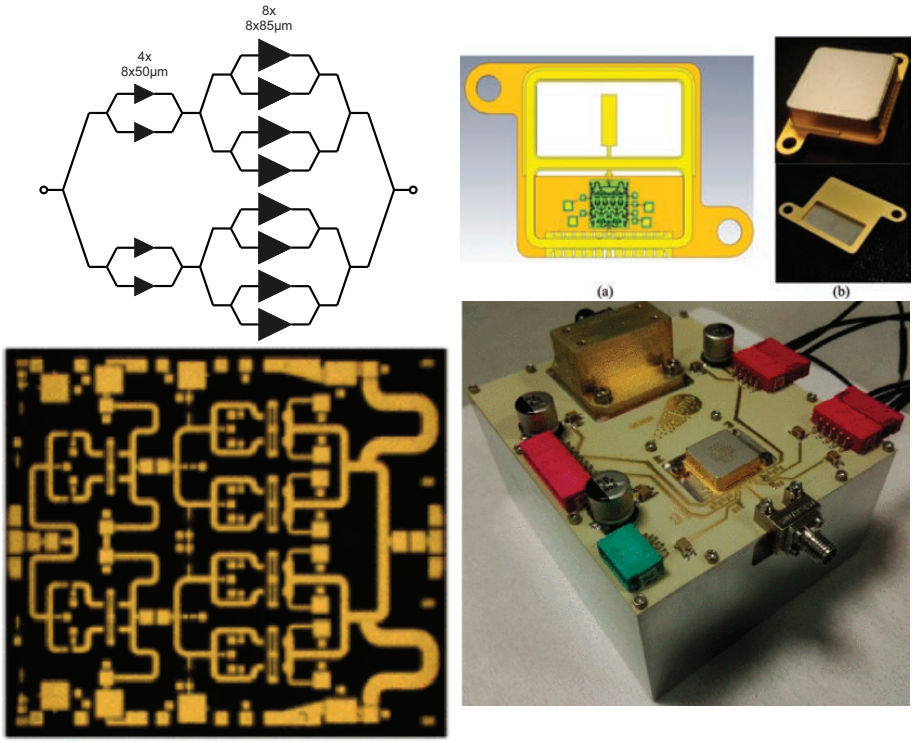

Fig. 6: Block diagram and chip photograph (left) of the MMIC in [4] (4×3.4 mm^2) and corresponding package and assembly (right) ©2019 IEEE.

To reach similar power values at the MMIC level in GaN-Si processes, the final stage requires a larger periphery. In [27], a recent example of a GaN-Si corporate MMIC PA developed on a 100 nm process is presented. As shown in Fig. 7, the MMIC is based on a three stage architecture employing $8 \times (8 \times 80\,\mu\text{m})$ devices in the last stage and $4 \times (8 \times 50\,\mu\text{m})$ and $2 \times (8 \times 30\,\mu\text{m})$ devices in the driver and pre-driver stages, respectively. The MMIC is biased with a drain voltage of 12 V in class AB. A quite good agreement between measurements and simulations is reported, with the HPA achieving an output power in continuous wave of 40 dBm, from 17 to 20.5 GHz, with an associated gain and PAE of 22 dB and 30%, respectively.

A similar HPA architecture developed on an OMMIC D01GH/Si process (100 nm gate length GaN-Si) is presented in [28]. As shown in Fig. 8, it exploits

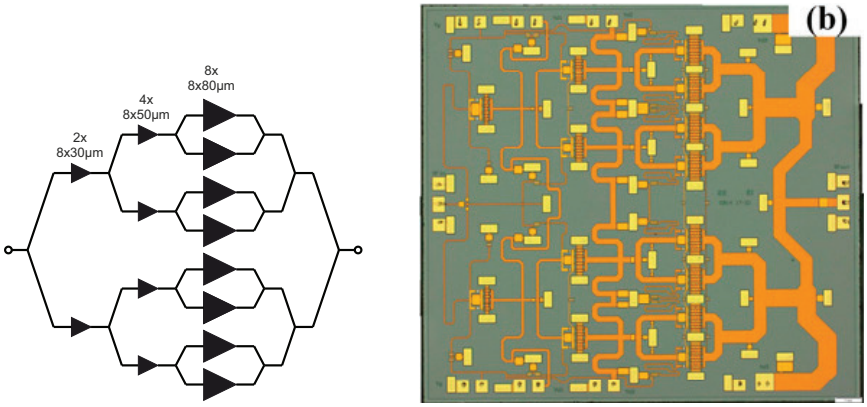

Fig. 7: Block diagram and chip photograph of the corporate MMIC PA of [27] (3.5×3.2 mm^2) ©2022 IEEE.

a slightly larger periphery in the final stage (eight devices of $8 \times 100\,\mu$m, each) than the MMIC PA in [27], whereas the same number of stages is selected to meet the gain target of around 22 dB. The larger periphery is probably needed in order to compensate for the lower drain bias voltage adopted (11.25 V instead of 12 V) to fulfill space de-rating rules. At any rate, the PAE results are on the order of 30% (peak >40%) with an output power better than 40 dBm from 17.3 to 20.2 GHz. Using the same process, a balanced PA configuration is proposed in [29]. In this case the last (i.e., the outermost) level of power combination is provided by a 90° hybrid rather than by a non-isolated fork structure (Fig. 9). To maintain the appropriate phase relation, a 90° hybrid also implements the outermost level of power splitting at the input.

The gain is 24 dB, and the PAE results are higher than 24% on the whole 17.3-20.2 GHz band.

To achieve the typical output power of more than 100 W required at the SSPA level, the MMICs of [28] and [29] were combined, adopting two strategies, as described in [22]. The proposed approaches rely on a cavity-based radial combiner (Fig. 10) and a single-waveguide longitudinal probe spatial combiner (Fig. 11). In fact, the high losses in the K-band of planar distributed structures, such as branchline or Wilkinson couplers, hamper their exploitation for the combination of several MMICs. In particular, the combination of sixteen 40 dBm

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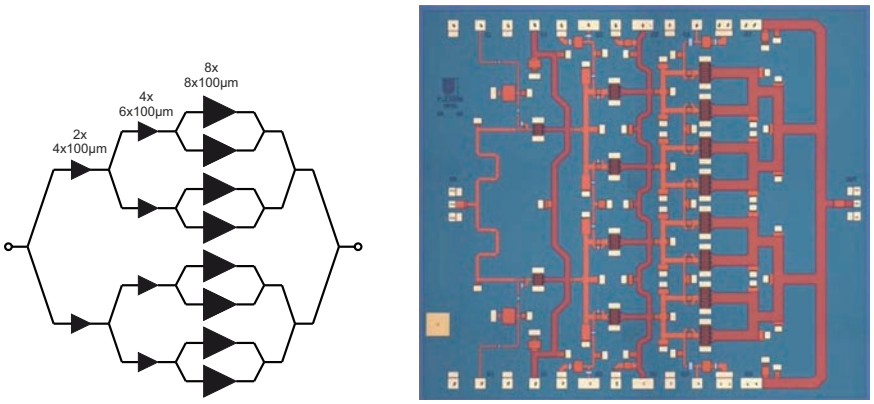

Fig. 8: Block diagram and chip photograph of the corporate PA of [28] (5×4.5 mm^2). Reproduced with permission.

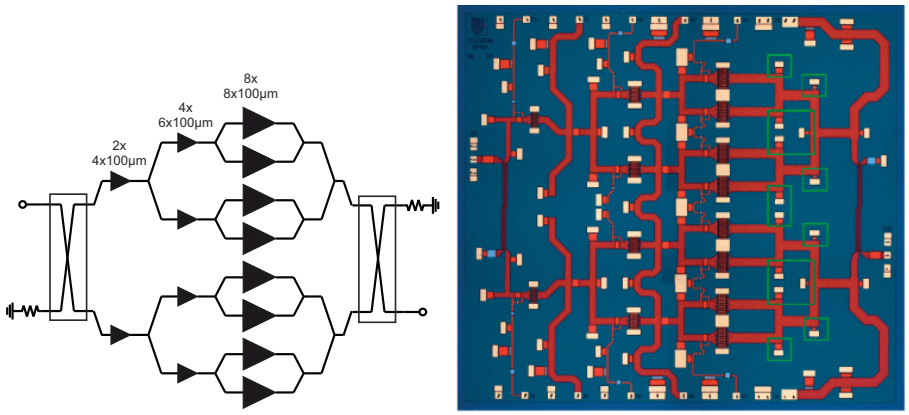

Fig. 9: Schematic and chip photograph of the balanced PA of [29] (5×4.5 mm^2) ©2021 IEEE.

MMICs leads to the realization of an SSPA with more than 50 dBm of saturated output power, with combiner losses that remain lower than 0.5 dB for the radial combiner and 1.37 dB for the spatial one. The higher losses of the latter, influenced by the presence of a Wilkinson structure, reduce the combining efficiency to 73%, while for the radial combiner, it remains as high as 89%. Conversely, the gradual degradation of the spatial combiner due to possible MMIC failure is less pronounced than in the radial combiner (0.5 dB instead of 3 dB losses, with 4 MMICs off) thanks to the presence of isolated splitting/combining structures. Finally, the spatial combiner is lighter and more compact than the radial one.

A very recent example of a three-stage HPA moving the threshold of maxi-

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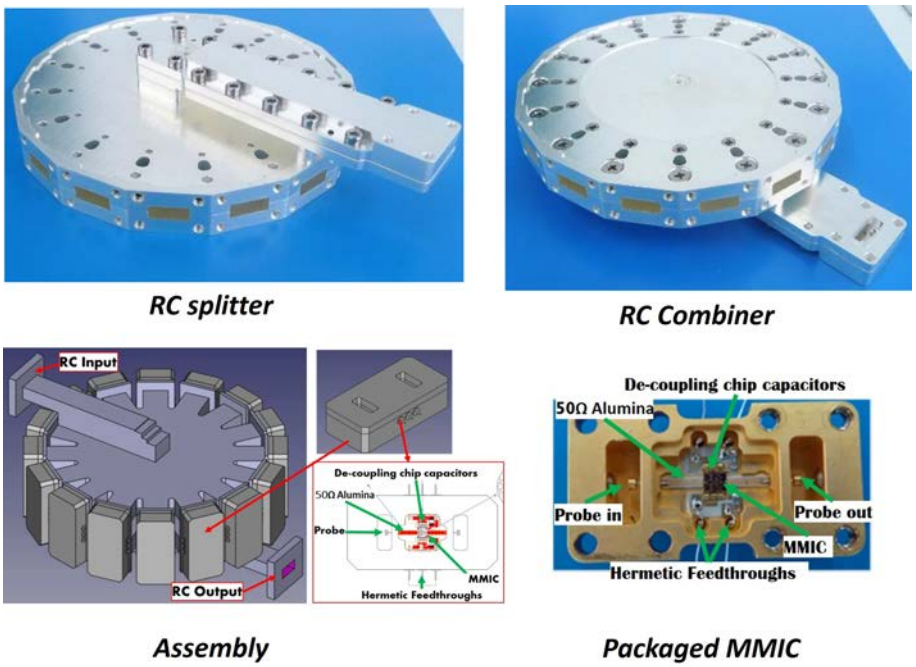

Fig. 10: Radial combiner from [22] ©2020 IEEE.

mum power attainable from a single MMIC is presented in [30]. The reported chip, in pulsed conditions, achieves more than 45 dBm in the 17.5 GHz-20.5 GHz band with an associated gain in excess of 26 dB and a PAE higher than 23 % in the full band. Fig. 12 shows the block diagram and a picture of the MMIC.

Doherty PAs

The adoption of DPAs in Ka-band satellite applications, fostered by the adoption of non-constant envelope modulation schemes similar to those adopted for ground applications, although less complex, is relatively recent. Among the most relevant reasons for this include the complexity of the power combination, the achievable bandwidth, and the intrinsic linearity. The amount of power that can be achieved at the MMIC level is sharply limited by the power density of the adopted technology since a limited number of on-chip power combinations is achievable. The linearity of DPAs is typically worse than that of class-AB non-load-modulated PAs, which may limit their adoption in scenarios such as

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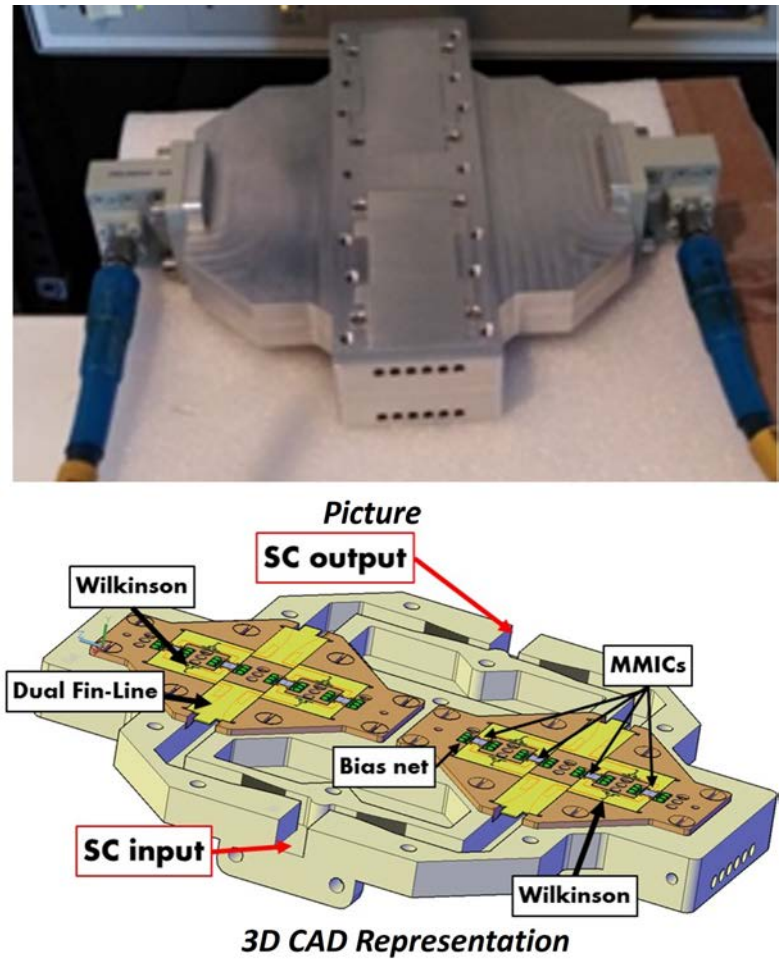


Fig. 11: Spatial combiner from [22] ©2020 IEEE.

satellites, where external linearizers are not always feasible. Finally, covering the full satellite Ka-band is really challenging, especially considering that on-chip drivers need to be adopted and most often embedded into the DPA architecture to ensure good efficiency performance.

The adoption of GaN-SiC can allow the achievement of significant power targets with a relatively simple structure, (e.g., with a single power transistor in the Main and Auxiliary branches), thus implementing the simplest PA architecture. One of the first prototypes was internally developed by the European Space Agency (ESA) in 2018 [31]. The MMIC DPA, whose block diagram and

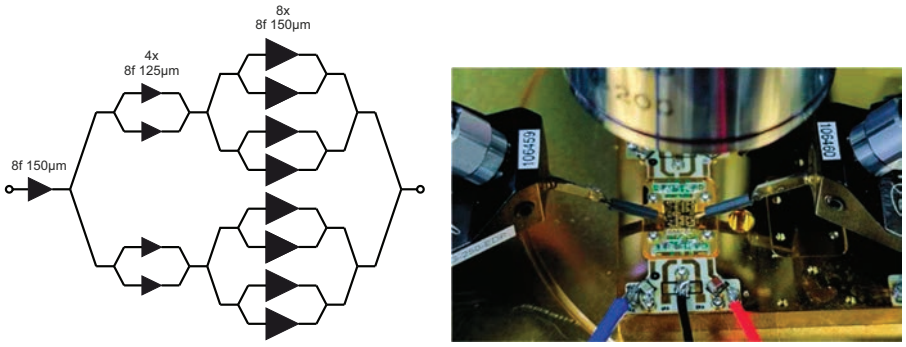


Fig. 12: Block diagram and chip photograph from [30] (4.55×2.2 mm^2) ©2022 IEEE.

chip photograph are shown in Fig. 13, was developed on a 100 nm AlGaN/GaN on SiC process. It adopts a dual-driver Doherty architecture with an additional driver at the input. It is able to achieve 25 dB linear gain and 34 dBm saturated output power with a saturated PAE of 37%. The final stage periphery is $2 \times (8 \times 100\,\mu\text{m})$. The back-off efficiency is traded off with the linearity, allowing it to achieve 27% PAE and 15 dB NPR at 2 dB output back-off. This prototype shows the potential of DPAs for this application, despite operating in 20–21 GHz, (i.e., only partially covering the targeted band).

A more recent GaN-SiC DPA was developed by Thales France on space-evaluated GH15-10 UMS technology and presented in 2022 in [5]. The architecture is 3-stage, similar to the previous architecture except for the fact that two stages of dedicated drivers are embedded into the Doherty, rather than adopting a single driver at the input. The block diagram and chip photograph are shown in Fig. 14. The pulsed measurements demonstrate that, depending on the drain supply voltage, which can range from 14 V to 20 V, the MMIC can achieve output powers on the order of 40–44 dBm with a PAE around 30–40% at saturation. However, the space de-rating requires the drain voltage to be limited to 15 V. The three-stage architecture attains a 30 dB linear gain over the target band. The DPA is also characterized under modulated signal excitation with 1 GHz instantaneous bandwidth. It operates with 26–27% average efficiency at 15 dB and 20 dB NPR when a DVB-32 APSK and a SC-FDMA signal are used,

respectively.

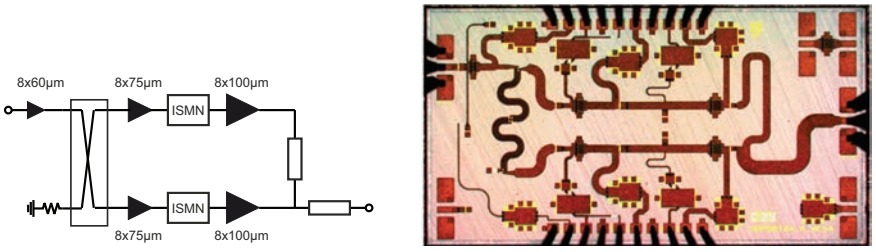


Fig. 13: Block diagram and chip photograph of the MMIC in [31] ($2.1 \times 4\text{mm}^2$) ©2018 IEEE.

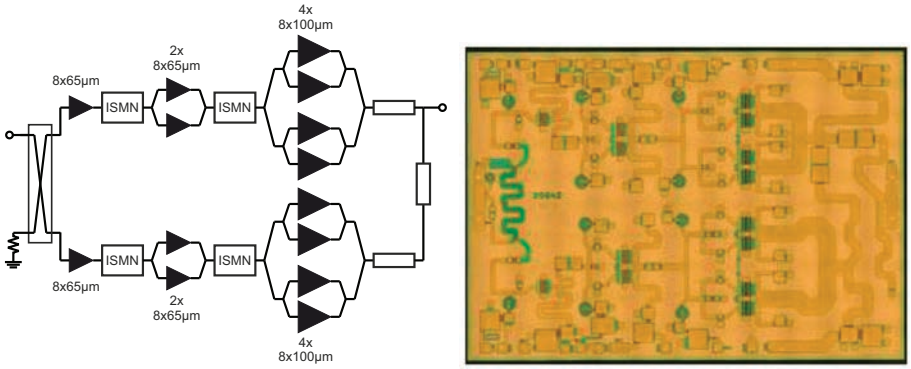


Fig. 14: Block diagram and chip photograph of the MMIC in [5] ($5.1 \times 3.6\ \text{mm}^2$) ©2022 IEEE.

To achieve comparable power levels in GaN-Si, it is necessary to resort to an on-chip power combination strategy, since the lower power density makes single-transistor DPA architectures infeasible (considering that the maximum individual transistor periphery is comparable to GaN/SiC). In [32], different on-chip power combination strategies are presented and discussed. The target is to realize DPA MMICs with 5-W saturated output power in the 100 nm GaN-Si technology of OMMIC (D01GH). The adopted transistor periphery is 8×100 µm which is the largest for which the non-linear model provided by the foundry is validated. Dedicated source- and load-pull characterization has shown that it can provide around 33 dBm of saturated output power with an associated PAE of close to 55%. This is compatible with the estimated power density of 2 W/mm, after applying suitable space de-rating to the drain supply voltage (from 15 V

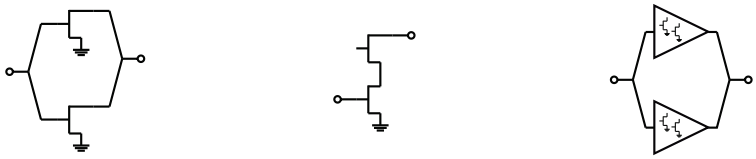
to 11.25 V) [33].

Therefore, to reach the required power levels with a reasonable margin, two transistors need to be combined in each of the DPA branches. Fig. 15 summarizes the power combination strategies explored. They can be subdivided into two categories, namely at the transistor level and at the PA level. Power combination at the transistor level offers two possibilities, namely combining two of the individual power transistor cells in parallel (a) or in series (i.e., stacking them) (b). Alternatively, it is possible to design a DPA cell that adopts a single transistor in the Main and Auxiliary stages and then combines the DPA cells in parallel (c).

At the transistor level, the parallel combination potentially offers an easier design flow, although at the price of lower optimum load impedances and thus an increased transformation ratio to reach 50 Ω, thus narrowing the achievable bandwidth. Moreover, the loading conditions of the two transistors could result in an asymmetry due to possible electromagnetic coupling effects among adjacent passive structures. On the other hand, the stacking of transistors entails a quite complex design flow and layout planning. The significant matching and stability challenges, especially when the technology is adopted rather close to its cut-off frequency, are however compensated by the increased gain and optimum load impedance. A DPA based on two-transistor stacked cells in the final stage, as detailed in Fig. 16, is presented in [34]. Thanks to the adoption of the transistor stacking strategy, a two-stage architecture (i.e., with a single level of driver amplifiers inserted in the Doherty branches) is sufficient to achieve a linear gain on the order of 25 dB.

Based on the large signal characterization at 17.3 GHz and 20 GHz, the DPA delivers saturated output power around 38 dBm with an associated PAE of 35%, while maintaining a PAE of 20–25% at 6 dB OBO.

The combination at the PA level allows for better control of the loading conditions since a single individual transistor composes the Main and Auxiliary power stages, but it generally implies a larger chip area and a more complex



(a) (b) (c)

Fig. 15: Power combination strategies: (a) transistors in parallel, (b) stacked transistors, (c) amplifiers in parallel.

layout, due to the difficulty of routing the DC bias lines to the internal active devices which, unlike in a corporate PA, typically require different voltages than the external ones. Similar to what was discussed previously for class-AB PAs, two possibilities are available to split and combine the power between the DPA cells, adopting either isolating structures (such as 90° hybrids) or non-isolating ones (such as simple forks). Non-isolating power splitters and combiners may lead to higher efficiency, since they minimize losses, especially at the output, but they are less robust in terms of stability and input/output return loss.

In the case of the combined DPAs, it is possible to design and test the single DPA cell first. For instance, the DPA cell proposed in [33] has been manufactured and tested on-wafer, and used as a building block for the full combined MMIC presented in [6]. Fig. 17 shows the block diagram of the combined DPA, the chip photographs of the MMICs alone, and when it is mounted in its test fixture. The complex routing of the DC lines is clearly visible in the MMICs. The DPA cell is matched to 100 Ω at the output, thus allowing a direct power combination with a non-isolating fork structure without additional impedance transformation. It has thus been characterized in an active load-pull setup that allows the synthesis of this optimum loading condition at each frequency. Despite the limited cooling possibilities, it demonstrates the ability to deliver 34 dBm output power and 25% efficiency (corresponding to 18–20% PAE) at saturation. At 6 dB OBO, the efficiency is 20% (15% PAE). The linear gain is 13–15 dB, thus confirming that at least one extra driver stage at the input is required for the final full MMIC DPA to achieve the target. The overall MMIC

is composed of two parallel combined DPA cells with a single pre-driver in front of the power splitter, as shown in Fig. 17.

A rather uniform large signal performance is maintained over a 4-GHz band, fully covering the targeted 17.3–20.3 GHz with a significant margin. The saturated output power ranges from 36.6 to 37.7 dBm, in line with the preliminary evaluation of the DPA cell, with an associated PAE of 23–31%. An improved efficiency performance compared to the DPA cell is achieved thanks to a twofold positive effect, the higher gain and the better heat dissipation provided by the test fixture. The PAE at 6 dB OBO is always higher than 20%. The linear gain ranges from 24 dB to 30 dB; the variability versus frequency is mainly ascribed to the effect of the input section, (i.e., the single driver and the non-isolating power splitter between the DPA cells). This choice has turned out to be somewhat sensitive to the bias point of the transistors, which have been optimized primarily to achieve the best efficiency performance. The NPR characterization on the full DPA MMIC was performed adopting an arbitrary white Gaussian noise signal with a 100-MHz bandwidth, showing compliance with the 15 dB requirement over the entire power dynamic range.

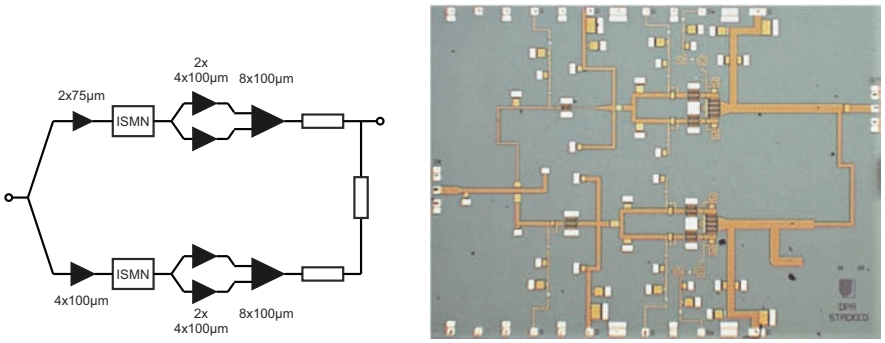


Fig. 16: Block diagram and chip photograph of the stacked DPA of [34] (5×3.7 mm^2) ©2022 IEEE.

The performance of the analyzed DPAs is summarized in Table 1, where they are also compared to the corporate PAs previously described.

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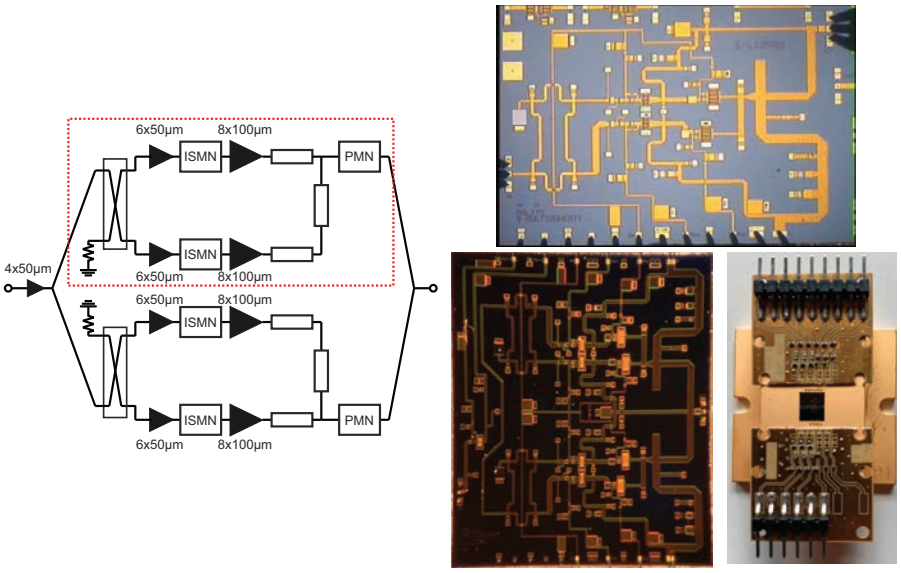

Fig. 17: Block diagram (left) and photographs (right) of the DPA cell in [33] (4×3 mm^2), and of the full combined MMIC in [6] (5×6 mm^2) and its test fixture ©2022 IEEE.

Conclusion

This contribution provides an overview of the current state-of-the-art for GaN-based Power Amplifiers in Ka-band satellite communication applications. At present, it is challenging to determine a clear winner in this field. The landscape is rapidly evolving, and the potential future developments are not yet fully defined. TWTAs-based modules still dominate the market, but solid-state power amplifiers are gaining momentum due to the availability of reliable and high power density processes based on GaN technology.

Whether the solid-state PAs will completely replace the current reference solution in the near future will largely depend on specific trade-offs and considerations, particularly in terms of cost. Further research efforts are still needed to address critical aspects related to the design and integration of space-borne PAs, the outcomes of which will lead to the evolution of the market.

Table 1: Performance of state-of-the-art GaN PAs for Ka-band satellite applications.

Substr.	**Arch.**	**Freq. (GHz)**	$\mathbf{P_{out,sat}}$ **(dBm)**	$\mathbf{PAE_{sat}}$ **(%)**	$\mathbf{PAE^{\#}_{OBO}}$ **(%)**	$\mathbf{G_{sat}}$ **(dB)**	**Ref.**
SiC	corp.	17.2-20.2	41	35	-	19	[3]
SiC	SSPA	17.3-20.3	45	20	-	30	[3]
SiC	corp.	17-21	40.4–40.8	36–40	-	22	[4]
SiC	corp.	17.5–20.5	45–46.1	23–34	-	26	[30]
Si	balanc.	17.3-20.2	39.5	28	-	24	[29]
Si	corp.	17.3-20.2	40	25–35**	-	25***	[35]
SiC	DPA	20-21	34	37	18*	17*	[31]
SiC	DPA	17.3-20.3	41.5	37	32	30	[5]
Si	DPA comb.	16.3–20.3	36.6–37.7	23–21	19–21	18–22	[6]
Si	DPA	17.3-20.3	34	25**	20**	8–10	[33]
Si	DPA	17.3-20	36.3–38	24–37	18–28	20–23	[34]
Si	corp.	17–20.5	40.4	33	-	23	[27]

PAE at 6 dB OBO

* Value extrapolated from graphs

** DE

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