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Doctoral Dissertation
Doctoral Program in Electronics Engineering (36^{th}cycle)

High-resolution Digital Pulse width Modulation Techniques for Digitally Controlled Power Supplies

By

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Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

Ahmed Abdullah
2024

Abstract

Recent advances in large bandgap semiconductor devices, such as silicon carbide (SiC), gallium arsenide (GaAs), and gallium nitride (GaN), have created new possibilities for high-frequency power conversion. This has led to the development of digital control in power electronics.

In modern Switch-mode Power Supplies (SMPS), digital controllers are becoming more popular due to their inherent flexibility, reliability, cost-effectiveness, and reduced susceptibility to aging compared to their analog counterparts. However, digitally controlled SMPS face challenges, such as the emergence of low-frequency steady-state Limit-cycle Oscillations (LCOs) due to quantization effects from the Analog-to-Digital Converter (ADC) and the Digital Pulse Width Modulator (DPWM). While high-resolution ADCs and DPWMs can mitigate these issues, they also increase the complexity and cost of the system, especially for SMPS operating at high switching frequencies that utilize emerging GaN and SiC power transistors.

In order to overcome these challenges, several high-resolution DPWM techniques have been proposed to enhance DPWM resolution. This motivates further research into high-resolution DPWM in digitally controlled SMPS, as well as the design of DPWM-based Digital-to-Analog Converters (DACs).

This thesis extensively investigates Dyadic Digital Pulse Width Modulation (DDPWM) as a systematic approach to achieving accurate, LCO-free operation in digitally controlled power converters. It proposes a digitally controlled Boost converter implementation based on DDPWM, which is justified through a comparison of Buck and Boost converters. The analysis highlights the challenge of meeting the DPWM resolution requirement over a wide range of duty-cycles in Boost converters compared to Buck converters due to non-linearities in output voltage quantizations. The effectiveness of DDPWM in suppressing LCOs, improving DC accuracy, and reducing output ripple is verified through Simulink/Modelsim co-simulations and

experimental testing on a voltage-mode Boost converter. Significant improvements are observed in DC accuracy and output ripple compared to plain DPWM and Digital Thermometric Dithering Pulse Width Modulation (DTDPWM).

As a second contribution, this thesis presents a theoretical assessment of Dyadic Digital Pulse Modulation (DDPM) and its spectral properties. It includes a comparison among software (SW) implementation of existing hardware (HW) DDPM modulator architectures and proposes a novel optimized DDPM modulator architecture tailored for software (SW) implementation. The proposed SW DDPM modulator is evaluated through the implementation of a software-defined 8-bit DDPM DAC on a Texas Instruments c2000 microcontroller platform. Results demonstrate superior performance compared to iterative SW implementations in terms of sample rate, INL error, DNL, and dynamic characterization parameters (SNDR, SFDR, ENOB).

I would like to dedicate this thesis to my loving parents

Thank you for your unwavering love and support throughout my academic journey. Your guidance and encouragement have been my source of strength and inspiration. I am forever grateful for all the sacrifices you have made to provide me with the best education possible. This achievement is as much yours as it is mine. I hope I have made you proud.

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Chapter 1

Introduction

Earlier, analog devices mainly controlled power electronics devices, utilizing a controller board with various components to oversee and manage the module's functions. Analog systems presented drawbacks such as many parts, restricted computational capabilities, susceptibility to aging and temperature changes, and limited reconfigurability. This led to performance limitations and complexity with discrete components as designs became more complex. To address these challenges, digital control systems have become more appealing due to their ability to execute complex control strategies using powerful calculations and math-intensive algorithms. However, transitioning to digital control introduces challenges like quantization loss, delay, and complexity. By exploring the history and implementation of technologies, this chapter provides valuable insights into the advantages and challenges of digital control versus analog control, potential applications, and future advancements in digital control of power electronics systems.

1.1 Digital Control in Power Electronics

Efficient management and control of electric power are necessary for a wide range of applications, from on-chip power management to motor drives and utility applications that require hundreds of kilowatts or megawatts of power. To achieve high efficiency and static and dynamic control of inputs or outputs under various operating conditions, power electronics are used, which consist of switched-mode

power supplies (SMPS) made up of passive components (capacitive and inductive) and power semiconductor devices that function as switches [7].

Classical power electronics is a well-established field with developed technologies and engineering practices, particularly in discrete component-based SMPS and conventional analog control strategies. However, power electronics is constantly evolving, and promising research fields are shaping the future trajectory of the field. The need for higher SMPS conversion efficiency, propelled by environmental concerns and regulatory measures, has led to significant progress in the development of wide bandgap semiconductor devices like silicon carbide (SiC), gallium arsenide (GaAs), and gallium nitride (GaN) [8]. These advancements have the potential to enable amplification of radio signals and power conversion at ultra-high frequencies, paving the way for high-frequency (multi-MHz) and high-temperature power converter circuits. This could lead to significant progress in achievable power densities, driving innovation in power electronics. It also encourages research in other areas. The integration of magnetic and capacitive passive components into a single device opens up possibilities for implementing minimum volume, quasi-monolithic converters, thereby improving efficiency and compactness. Furthermore, addressing electromagnetic interference (EMI) becomes critical for the design of compact, high-frequency converters, requiring thorough analysis and mitigation strategies. Another critical research direction is integrating control circuits and power devices on the same semiconductor chip, known as the digital power concept [8]. This integration holds significant potential for optimizing performance and efficiency, as well as human-machine interface (HMI), heralding a new era in power electronics design. Modern power electronics, summarized in Fig. 1.1, have progressed significantly from just proof-of-concept demonstrations to the point where fully digital controller chips are now available from multiple vendors. These chips are being adopted at increasing rates in many different applications. Indeed, integrating complex control functions anticipated for the next generation of power supplies presents a challenge that realistically necessitates the advanced capabilities offered by digital control design [8].

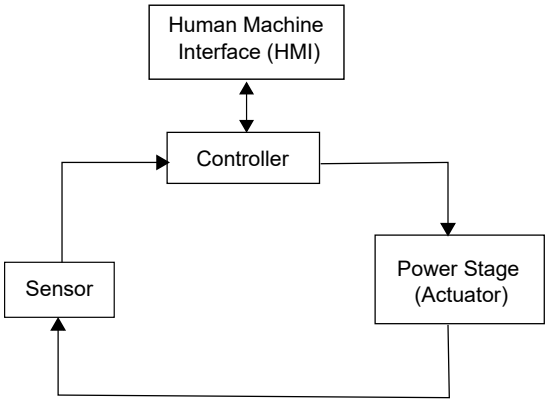

Fig. 1.1 Block diagram of a modern SMPS-based system.

1.1.1 Why Digital Control?

Digital power is the application of digital control to the power supply. This integration of digital control directly at the pins of the control IC bridges the gap between analog and digital domains within the power supply system.

It is important to note that while digital control is used, the power stage's operational principles and design aspects remain unaffected. Factors such as power supply specifications, topology selection, component choices, and required control functions still fall within the analog domain, requiring expertise in power supply design.

However, the significant difference between analog and digital control lies in the quality and quantity of information available to the controller for making operational decisions. In other words, a very complex control function is required, which is too complicated to design in the analog domain, whereas digital control has the capability to implement complex control laws, allows precise parameter values to be captured, stored, and utilized for decision-making processes. Digital controllers offer inherent flexibility, allowing designers to easily modify or reprogram control strategies without requiring significant hardware changes.

Digital controllers use advanced semiconductor technologies, often incorporating microcontrollers (μC) or digital signal processors (DSPs) as their core components. This integration provides greater flexibility in implementing various control algorithms than traditional analog controllers. Unlike analog systems, which have predetermined responses, digital controllers offer user-programmable reactions to

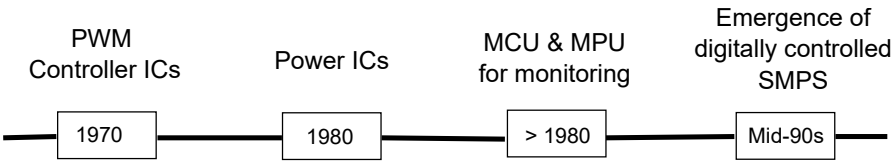

Fig. 1.2 Events leading to the emergence of digitally controlled SMPS.

changing operating conditions. Designers can customize responses to current limit thresholds, allowing for adaptive behavior, such as temporary operation within the limit during transient conditions before resorting to shutdown, thereby enhancing overall system resilience and performance.

Below is a summary of the factors that led to the rise of the concept of "digital power" in power electronics applications.

- The cost of digital integrated-circuit processes has been declining due to ongoing advancements, while processing capabilities continue to increase [7].
- The need for improved system integration and more complex power management and monitoring tasks has led to the need for digital interfaces and programmability in applications related to switched-mode power conversion [9].
- Innovative methods for achieving high-performance digital control have been demonstrated, along with practical approaches that provide new capabilities or performance gains that would be challenging or impractical to attain using traditional analog techniques [10].

1.1.2 Historical Context

The introduction of the first PWM controller IC, the SG1524, by Bob Mammano in 1976 marked the beginning of the digital power era. Subsequent advancements in PWM controllers, summarized in Fig. 1.2, offered more features and capabilities as the requirements for SMPS design became more stringent [11]. The mid-1980s saw an expansion in the diversity of power ICs beyond PWM control to address tasks such as supervisory and fault management. The introduction of microprocessor unit (MPU) and microcontroller unit (MCU) chips in the mid-1970s, followed by DSPs

in 1983, facilitated the proliferation of digital control. The deepest penetration of digital technology in SMPSs occurred with the introduction of DSP-based controllers (DSCs) and their firmware by the 1990s, enabling complete digital control of power conversion tasks [1].

In conclusion, while experimental systems with complete digital control were proposed in scientific literature earlier, widespread adoption of SMPS with digital control occurred in the late 1990s, thanks to the availability of low-cost microcontrollers and DSCs. This trend is expected to continue, further driving the integration of digital control into power electronics.

1.1.3 Trends and Perspective

It is clear from the above discussion that digital control in power electronics is becoming more widespread, and it is unlikely to stop. The advantages of digital control circuits are so compelling that it is probable that all current analog integrated control solutions will be substituted by new ones that include some form of digital signal processing core. The usefulness of digital control features in current and future power converters is indisputable [8]. The question that remains is how long the transition will take.

Applications like electrical drives, test power supplies, uninterruptible power supplies, and renewable energy source interfaces are expected to remain unchanged in the near future. The use of μC units or DSPs is expected to continue dominating this field with an increasing trend towards integrating higher-level functions. Some of these functions may include communication protocols for local area networks or field buses, man-to-machine interfaces, and remote diagnostic capabilities. These capabilities require separate signal processing units in combination with low-level control functions [7, 8].

There is currently no established market for digital controllers in low-power applications. However, research on digital control in this field is being conducted extensively. We can anticipate the arrival of advanced control solutions that can substitute traditional analog controllers with digital ones. This substitution will be carried out in such a way that it will be hardly noticeable to the end-user. This transition to digital control solutions is expected to take place in the near future.

Consequently, the complete integration of power and control circuitry is likely to have a transformative impact on how low-power converters are designed [7, 8].

Academia and industry have recently shown significant interest in digital control for power management. Numerous publications at major conferences have discussed the theoretical and practical aspects of digital control implementations. APEC 2003 organized the first Rap Session on digital power, which brought together participants from end users, power supply manufacturers, and IC companies. In early 2003, iSupply released the first Market Report on digital power.

1.2 Digital Control Architecture and Challenges

The specialized programmable Analog-to-Digital Converter (ADC), Digital Pulse Width Modulator (DPWM), and compensator blocks are utilized by the digital control architecture shown in Fig. 1.3 to attain high-performance closed-loop dynamic responses. Besides, a microcontroller core manages programmability, power management, and system interface functions. The controllers illustrated in Fig. 1.3 can be created using a standard digital VLSI design flow that begins with defining logic functions in a hardware language such as VHDL or Verilog.

There are two major differences between digital control and analog control: time quantization and amplitude quantization.

- **Time quantization**
  Time quantization is correlated with the discrete-time nature of the controller, which processes analog signals in sampled versions to produce a control output that is also discrete-time. This process introduces built-in time delays because of the ADC sampling, which can substantially impact the system's stability and response time. To create high-performance control loops, designers must thoroughly understand and consider the resulting delays and aliasing effects caused by the ADC sampling and also by the control processing. Although continuous-time averaged modeling provides an approximation for the sampling effects and control delays, a more accurate approach requires discrete-time modeling to directly design compensator transfer functions. Power electronics engineers may prefer traditional analog techniques for controller design, although var-

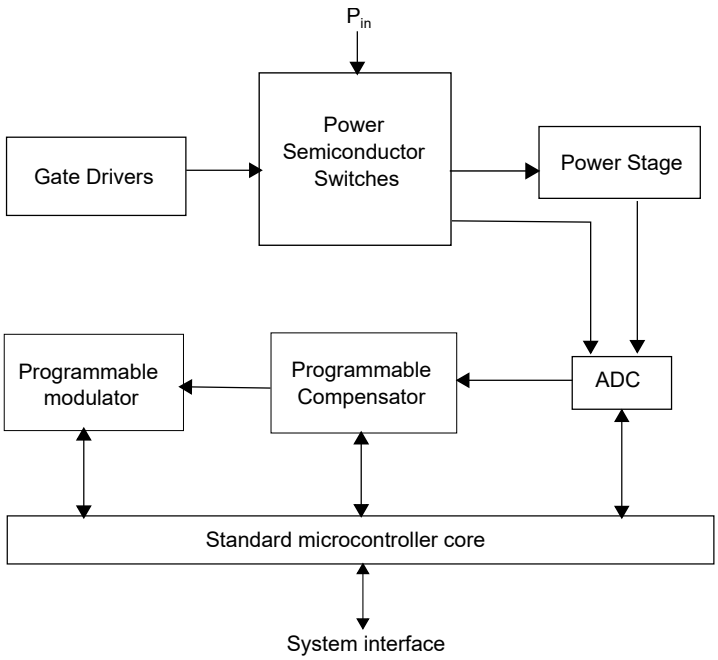

Fig. 1.3 Digital controller architecture of typical switched-mode power supplies.

ious digital design techniques have been suggested to combine the intuitive nature of analog design with digital control principles [7, 12].

Redesigning compensators from an analog to a digital format is a widely used technique due to its low design requirements in the discrete z-domain. However, this approach is vulnerable to discretization effects such as frequency warping, which can occur when using the bilinear method, as well as disregarding acquisition, computation, and zero-order-hold (ZOH) delays. A transfer function in the z-domain is obtained as a result of utilizing either the redesign or direct digital design methods. This transfer function can be later transformed into a difference equation that can be used for implementation purposes. The use of digital multipliers for coefficient multiplication may increase computational delays or system clock frequency, which can pose issues for high-frequency switching converters. Using lookup tables (LUTs) of specific sizes is recommended to reduce delays. [13, 14].

- **Amplitude quantization**

  The precision and accuracy of regulation in digitally controlled converters depend on the resolution of ADC and DPWM blocks. Improved signal res-

olution is achieved through higher bit counts in ADC and DPWM, but this still introduces amplitude quantization effects due to the discrete finite values involved. Limit cycling, which is a steady-state disturbance, can result from these nonlinear effects and will be discussed in detail in subsequent chapters [7, 15].

Other than that, digital interfaces follow algorithms that can be interrupted by higher-priority instructions, potentially causing feedback correction delays. In fault conditions, prompt reactions are necessary, making it critical for DSPs to have faster sampling rates and instruction cycles. The switching frequency of DC-DC conversion further complicates digital design as power supply designers aim to reduce core size, which is inversely proportional to the converter's switching frequency. Increases in switching frequency necessitate corresponding enhancements in the sampling speed of error correction controllers to maintain effective feedback loop resolution during each power conversion cycle [16, 17].

The complexity of digital control algorithms, which often involve intricate mathematical models and algorithms, requires significant computational resources. Real-time implementation of these algorithms can be challenging, especially in high-power applications where fast and precise control is essential. The computational demands may strain the resources of μCs or DSPs, necessitating algorithm optimization or more powerful processors [18, 19].

Integrating digital control into power electronic systems increases system complexity due to additional hardware and software components. This complexity poses challenges for system design, parameter tuning, and fault diagnosis. Integrating digital control systems with existing power electronic devices or legacy systems becomes a formidable task, requiring meticulous consideration of compatibility and communication protocol [18].

Another critical consideration in digital implementations is recognizing that μCs or DSPs operate on significantly lower voltages due to advanced semiconductor technologies. However, unlike their analog counterparts, they lack direct interfacing capabilities with power components. The power supply requires low-voltage supplies, high-current gate drivers, and compatible input thresholds for proper functioning. This creates a clear partition between the analog and digital segments of the power supply.

The digital controller's output needs to be converted into a signal that can drive the power switches in the converter. Furthermore, the voltage levels must be adjusted to match the input voltage range of the analog inputs. This range is usually determined by the reference voltage of the onboard ADC that is present within the digital controller.

1.3 Advantages of Digital Control

Applying digital control techniques to SMPS has garnered significant interest due to several compelling advantages over analog counterparts, which are listed below [12, 18, 20, 21].

- **Precise Control and Adaptability**
  One of the most notable advantages is the capability to implement sophisticated control laws, effectively managing nonlinearities, parameter variations, and construction tolerances. This is achieved through self-analysis and autotuning strategies, which are challenging or impractical with analog methods.

- **Flexibility and Ease of Modification**
  Digital controllers offer inherent flexibility, allowing designers to easily modify or reprogram control strategies without requiring significant hardware changes. Moreover, signal noise has less impact on digital control systems, and they are not affected by aging effects or thermal drifts.

- **Integration with Modern Devices**
  Embedded microprocessors have become indispensable due to the prevalence of electronic devices requiring man-to-machine interfaces (MMIs). Digital controllers leverage computational power for lower-level control tasks, making them almost unavoidable in modern electronics.

- **Proliferation Across Industries**
  The adoption of digital controllers has been steadily increasing, particularly in industrial power supply production areas. Adjustable speed drives (ASDs) and uninterruptible power supplies (UPSs) are examples of equipment that are now mainly controlled digitally.

Table 1.1 Comparison between analog and digital controller (+better;-worst) [5]

Control Properties	Analog	Digital
Clock frequency (CPU limitations)	+	-
Precision (tolerances, aging, temperature effects, drift, offset, etc.)	-	+
Resolution (numerical problems, quantization, rounding, etc.)	+	-
Bandwidth (sampling loop, ADC ñ DAC speed)	+	-
Compatibility	+	-
Communication, data management	-	+
Advanced control algorithm (non-linear control, improved transient)	-	+
Multiple loops	-	+
Cost of a platform (flexibility, time to market)	-	+
Component count (comparable functionality, integration)	-	+

- **Cost-Effectiveness and Performance**
  The widespread use of digital controllers in a range of applications, including cost-sensitive markets like portable equipment, battery chargers, and electronic welders, has been made possible by the availability of inexpensive but high-performing μCs and DSPs.

The qualitative comparison between analog and digital control regarding the advantages is summarized in Table 3.1.

In addition to the advantages mentioned above, some key advancements in digital control are explained in what follows.

1.3.1 Efficiency Optimization

Power conversion efficiency is a crucial metric across applications, and digital controllers offer unique advantages in the realm of efficiency enhancements. These advantages include precise adjustment of switching frequency and timing parameters of switch control waveforms, real-time power stage reconfiguration, and control of current distribution in multiphase setups. Digital controllers also enable algorithmic approaches for on-the-fly efficiency optimization [18, 19].

The adoption of digital control in high-frequency power electronics is reshaping conventional design practices and finding utility in diverse applications. Power systems, from mobile devices to data centers and communication networks, are increasingly featuring programmability, monitoring capabilities, digital interfaces,

and system-level power management. Digital control enhances dynamic responses, reduces passive filter sizes, and opens doors to efficiency optimizations at converter and system levels [22, 23].

Given the escalating energy costs and environmental issues, energy efficiency efforts are increasingly focused on power conversion efficiency and power quality in data centers and computer power supplies. Future energy efficiency programs are expected to set more stringent requirements for efficiency, power factor, and harmonic distortion in offline power supplies across broader load variations. Additionally, digital control algorithms offer significant benefits in renewable energy applications like photovoltaic power systems and electric vehicles, enhancing functions such as maximum power point tracking, fault detection, and efficiency optimization [7].

1.3.2 Improved Dynamic Responses

Linear small-signal models and frequency domain analysis-based compensator designs are relied upon in analog and digital converter controller designs. However, recent studies suggest that focusing on the switching behavior of the power stage and utilizing large-signal instantaneous variables for control actions can enhance dynamic responses. Switching surface control is a time-domain approach that has demonstrated potential in both analog and digital domains, with digital implementation being particularly suitable for investigating techniques aimed at improving dynamic responses [7].

Achieving time-optimal responses to external disturbances such as step load transients is of particular interest. These transients involve a precisely timed sequence of switching actions. Various digital control methods have been suggested to implement time-optimal control, exhibiting improved step load transient responses near the limits of passive LC filter components [24, 25].

Multisampling techniques, asynchronous sampling, mixed-signal control methods, and nonlinear techniques in DC-DC applications are among the other methods for enhancing dynamic responses. Explorations into improving dynamic responses in multiphase architectures and utilizing more complex controllers coupled with power stage modifications are also being investigated to push the boundaries of dynamic response enhancements even further [7].

1.3.3 Integration of Frequency-Response Measurements

Experimental verification using network analyzers to measure small-signal frequency responses is a crucial step in conventional controller designs. Recent research has investigated the incorporation of nonparametric frequency-domain system identification (system-ID) capability into digital controllers. This method involves using a pseudo-random binary sequence (PRBS) to perturb the duty cycle command, cross-correlating the perturbation with measured output responses to derive the system impulse response, and employing the fast Fourier transform (FFT) to obtain frequency responses. To enhance this process, techniques such as the fast Walsh–Hadamard transform (FWHT), signal filters, and noise reduction methods are employed [7, 26].

Examples of various converters have been applied successfully to this methodology, proving its efficacy in accurately identifying frequency responses. The frequency response identified can be utilized for diagnostic, design, or tuning purposes. The triumph of these applications relies on the accuracy of frequency response identification, the degree of automation, related costs in terms of complexity and time, and the impact on the output voltage. Research shows that it is possible to integrate automated frequency response measurement capabilities into digital PWM controllers at a reasonable additional cost and time duration. The identification process can typically be finished within a few hundred milliseconds while maintaining the output voltage within a narrow range throughout [7, 27, 28].

1.3.4 Communication and System-Level Integration

Integrating multiple power converters into modern digital systems is becoming more common due to various components like CPU, GPU, RAM, and audio processing units on a typical motherboard, each of which requires specific power specifications. This leads to individual power converters for each component, which necessitates power management communication between them to ensure seamless operation [7].

The popularity of digital control systems has risen as a result of this need for system integration. Many companies, including Texas Instruments Incorporated, Zilker Laboratories, Maxim IC, and Linear Technology, have developed digital controllers capable of communicating via the PMBus power management protocol [19].

The communication protocol enables central system controllers to control up to 127 DC-DC digital converters through serial communication. This system defines a language for over a hundred power-management-specific commands and offers several advantages, including power-up/power-down sequencing, fault detection, reaction mechanisms, and the ability to reconfigure power converters in the field. The growing complexity of digital systems has prompted the power electronics industry to develop digital controllers that incorporate the communication interface [29–32].

1.3.5 Digital Autotuning

Autotuning is a process that utilizes the programmability of digital controllers and aims to automatically adjust controller parameters based on system dynamics. The main objective of an autotuning digital controller is to fine-tune controller settings to meet predefined performance objectives by analyzing the characteristics of the power converter and the load. This approach is a significant departure from traditional design methodologies [33, 34].

There has been significant progress in practical autotuning digital control algorithms and implementation methods, with continuous research and development efforts dedicated to this area [7, 19].

1.4 Implementation Technologies for Digital Controllers

There are several technologies available that allow for real-time digital control, each with its own unique advantages and capabilities. These technologies include Microcontrollers (μC), Digital Signal Processor-Based Controllers (DSC), Digital Signal Processors (DSPs), Field-Programmable-Gate-Arrays (FPGAs), or Complex Programmable Logic Devices (CPLD), Real-time (RT) Rapid Prototyping Systems, Programmable Logic Controllers (PLCs), and Industrial Computers that use industrial buses [1].

1.4.1 Microcontroller and Digital Signal Controller

Microcontrollers are versatile solutions that combine analog and digital I/O capabilities, CPU, and memory on a single chip. They frequently come equipped with specialized DSP cores for control tasks. They integrate high-performance cores (16 or 32-bit), sufficient RAM, and FLASH memory, along with various peripherals such as ADCs, PWM units, pulse counters, and different communication interfaces like Serial Peripheral Interface (SPI), Controlled Area Network (CAN) bus, Universal Serial Bus (USB), Ethernet, and wireless connectivity options such as Zig-Bee and Wi-Fi integration [35–37].

Digital Signal Controllers are similar to microcontrollers in their computational capabilities but are tailored for System-on-Chip (SoC) development and may feature distinct memory configurations. Both μCs and DSCs are capable of exceeding 100 MIPS and 300 MFLOPS in "motion control" applications. They employ cores such as ARM Cortex, Infineon 167, Renesas SH2 for μCs, and Texas Instruments C2000 series and DSPIC series for DSCs in power electronics [38].

1.5 Digital Signal Processors

DSPs come equipped with a specialized "multiply and accumulate" (MAC) unit that enables them to perform better than standard cores. These chips were one of the earliest single-chip solutions used in power electronics. The TMS320C14 was one of the earliest components to feature a multichannel ADC, PWM outputs, and a 10 MIPS, 16-bit processor, which was explicitly designed for direct digital control [39]. In 1988, the TMS320C30 was introduced, a 32-bit wide floating-point DSP used in many high-end systems [1]. Many high-performance processors employ a dual-bus Harvard architecture, where one bus handles data flow, and the other manages program instructions and MAC units. This architecture increases efficiency as both buses operate independently and concurrently.

- **Communication Channels**
  Microcontrollers nowadays require advanced communication capabilities, leading to the integration of high-speed serial channels and specialized interfaces such as the SPI. These channels serve multiple functions, including interprocessor communication and facilitating high-speed interactions with peripherals

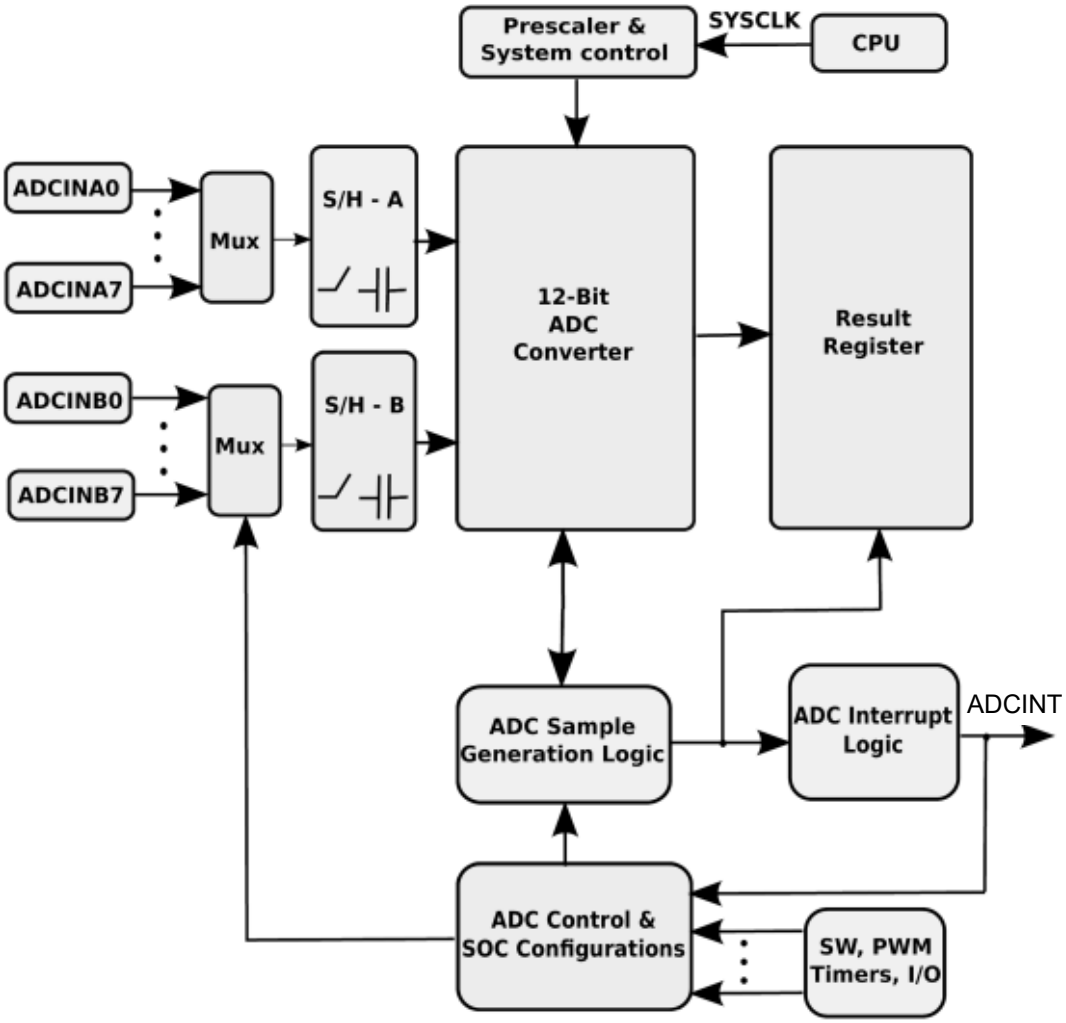

Fig. 1.4 Typical analog to digital conversion in microcontrollers [1].

like ADCs, DACs, and FLASH memory [40]. The CAN bus is widely used in industrial and automotive applications due to its robustness and versatility. Moreover, interprocessor communications benefit from USB and Ethernet interfaces, which enhance system connectivity and flexibility [1].

- **Analog to Digital Conversion**
  Power converters require precise feedback of current and voltage. This requirement has led to the integration of ADC capabilities in microcontrollers. Fig. 1.5 shows the typical ADC equipped with microcontrollers. These ADCs are mostly 12-bit or 14-bit, which have sampling times of just a few hundred nanoseconds. Some microcontrollers come with multiple ADCs featuring

Sample and Hold (S/H) input buffers to ensure phase correctness among three-phase quantities. This configuration allows simultaneous sampling of multiple input channels, eliminating phase shifts and delays. Finally, the management of multiple channels is made possible through multiplexers [1].

- **Timers and Counters**
  Microcontrollers commonly include timer/counter units for measuring and generating time intervals. These peripherals enable various functionalities, including event counting and signal generation based on the comparison between the timer's hardware counts and reference signals generated by the control algorithm [41].

- **Pulse Width Modulation (PWM) Peripherals**
  PWM peripherals are among the most crucial parts of microcontrollers. They are responsible for generating signals that control power devices such as MOSFETs and IGBTs through driver circuits. The microprocessor's output voltage/current is amplified, and buffers provide galvanic insulation between processing circuits and power stages. To create complex pulse-width waveforms with minimal CPU overhead, PWM units must be highly programmable and flexible. Furthermore, their operation should be user-friendly and intuitive to simplify system development and deployment. Modern μCs and DSCs are typically equipped with a 6-output, 16-bit comprehensive PWM module that facilitates interfacing with three-phase inverters/rectifiers. They may also incorporate additional units for driving DC-DC converters, Power Factor Correctors (PFC), or other electronic power converters. Advanced DSPs come equipped with high-resolution pulse width modulators (HRPWM) that operate at the nanosecond-level resolution, enabling precise control over power conversion processes [1].

1.5.1 Field Programmable Gate Arrays

FPGAs have become an essential part of digital control systems as they provide versatility and flexibility in applications such as PWM inverters, PFCs, DC-DC converters, multilevel converters, and more. These components, consisting of flip-flops and logic block arrays, permit users to generate customized hardware for specific applications through programming. As shown in Fig. 1.5, FPGA-based

controllers prioritize optimizing hardware architecture for algorithms to reduce slices, LUTs, and registers within particular processing times. They can function as coprocessors or complete SoC solutions, combined with DSPs or integrated with host processors. Their rising density allows for single-chip solutions with RISC processors like ARM Cortex-M3 or Microblade, enabling efficient motion control [1], [42], [43], [44].

The conventional process of designing FPGAs typically involves using Verilog and VHDL. However, HDL code generators like Simulink HDL Coder or LabVIEW add-in modules can be utilized for speedy prototyping. Nevertheless, manual HDL coding may be required for superior control performance, which can be a challenging task during hardware architecture design, as it demands significant effort [45].

1.5.2 Programmable Logic Controllers

PLCs are control systems that are based on microprocessors and can work independently. They use both analog and digital signals as input and execute actions according to pre-written programs. PLCs are highly modular, they can resist electrical disturbances and support various input/output (I/O) arrangements. PLCs are widely used in different industries and power systems and can communicate through interfaces such as Ethernet, RS-232, RS-485, or RS-422. They also support industrial buses like PROFIBUS and PROFINET [46, 47].

Different software tools like SIMATIC STEP 7 by Siemens or RSLogix 5000 from Rockwell Automation are commonly used for writing control logic into PLCs. However, PLCs from different manufacturers have their own exclusive memory organization, I/O addressing, and instruction sets, which reduces program interchangeability [48].

1.5.3 Real-Time Bus System Architectures

General-purpose industry-standard buses have gone through a three-decade evolution, initially preferring Rack-and-Stack instruments. General Purpose Interface Bus (GPIB) was introduced by Hewlett-Packard in the 1980s, which standardized communication but had limited performance [49]. Versa Module Eurocard (VME) performed well but had challenges due to its asynchronous nature. VME bus eX-

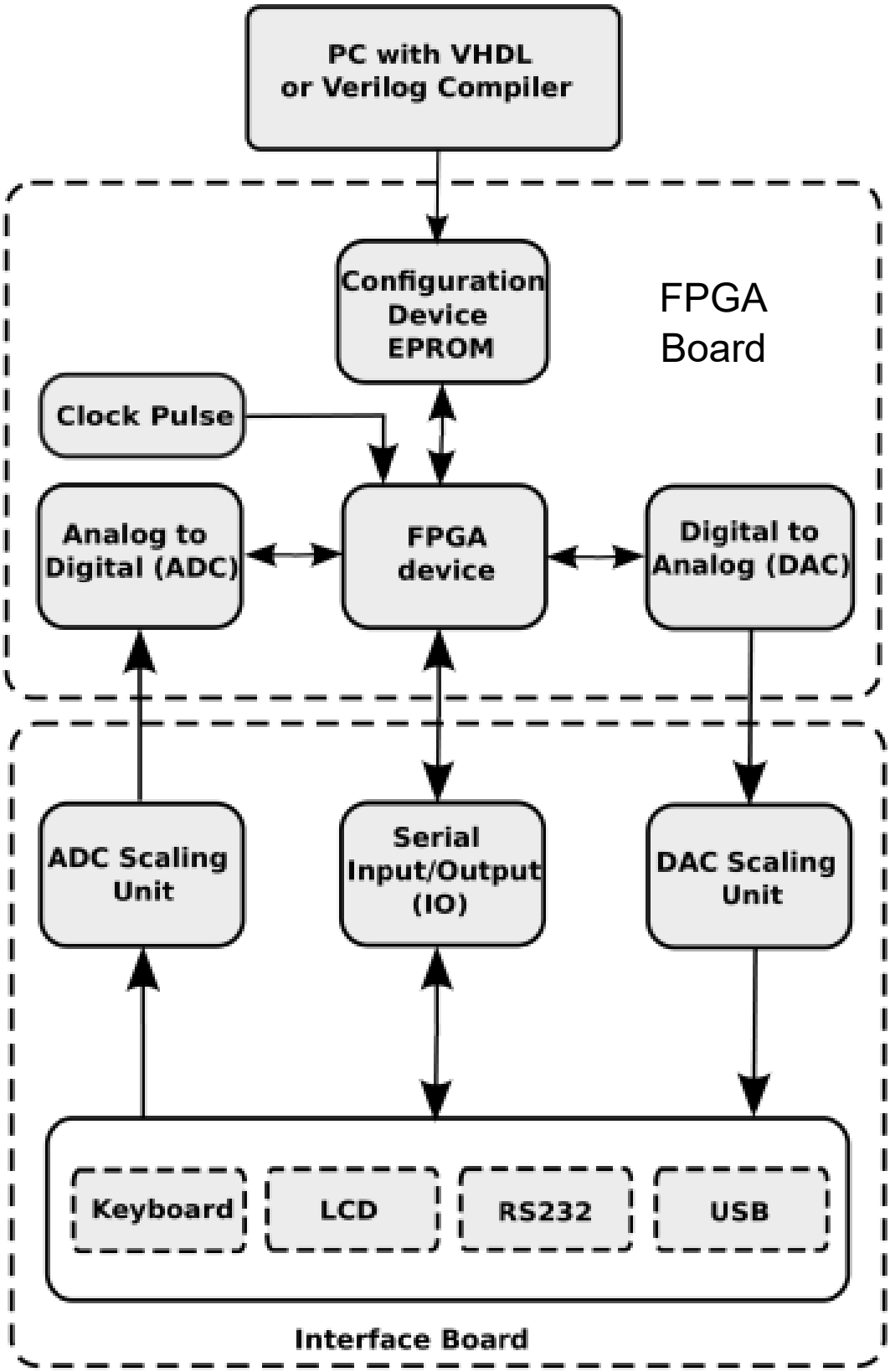

Fig. 1.5 Block diagram of FPGA-based digital platform [1].

tension for Instrumentation (VXI) improved VME by transitioning to a modular card-based system, which dominated digital subsystem architectures by the late 1990s [50]. PC1 extensions for Instruments (PXI), which was introduced in 1997, utilized Compact PCI and accommodated high-density analog electronics [51]. LAN extensions for Instruments (LXI) modules offer flexibility in test systems, using LAN for external triggers and IEEE-1588 for tight synchronization [52]. Power Management Bus (PMBus) standardizes power management protocols, simplifying communication and monitoring of power system devices [53].

Hybrid architectures combine components from various hardware platforms, such as VME, VXI, PXI, GPIB, USB, and Ethernet, providing flexibility for upgrades without a complete redesign. When selecting interfaces, integrators should consider I/O port availability and performance implications [54–56].

1.6 Applications of Digital Control in Power Electronics

Digital control has become widely adopted across diverse power electronic applications. In the following section, we will examine several notable applications where digital control plays a pivotal role in power electronics.

1.6.1 High Power Applications

1.6.1.1 Motor Drives

Motor drives are essential in various applications such as fans, electric vehicles, and industrial sectors like paper mills and steel mills. The evolution of digital control in motor drives began with the introduction of microprocessors in the 1960s. The adoption of digital systems accelerated with the development of microprocessors like the INTEL-4004 and INTEL-8080. By the 1980s, dedicated digital controllers like the PDP-11 minicomputer were widely used. DSPs and FPGAs further enhanced control capabilities, leading to ongoing advancements in motor drive technology [57–60].

1.6.1.2 High Voltage Direct Current (HVDC)

HVDC technology revolutionized long-distance power transmission, with notable systems like the Pacific Intertie and Nelson River link [61]. The transition from hardwired controls to digital systems occurred in the 1980s, with microprocessors like the INTEL-8086 becoming key components. DSPs and RT digital simulators played vital roles in HVDC control advancements, enabling robust testing and implementation [61].

1.6.1.3 Multilevel Converters (MCs)

Advanced switches and digital controllers enabled the development of innovative converter topologies like Modular Multilevel Converters (MMCs) [62]. MMCs offer advantages such as smaller footprints, minimal harmonic output, and enhanced controllability. DSPs and FPGAs are commonly used for controller implementation, supporting various PWM techniques for improved performance [62].

1.6.1.4 Renewable Energy

Renewable energy sources like solar and wind require sophisticated digital control systems for efficient integration [63]. Digital controllers enable precise control of power conversion processes, including AC-DC and DC-AC conversion in wind turbines and photovoltaic (PV) systems. FPGA-based controllers offer flexibility and high computational power, facilitating advanced control algorithms for optimizing energy generation and storage [64–67].

1.6.2 High Frequency SMPS Applications

1.6.2.1 Point-of-Load DC-DC Converters (POL)

POL power supplies (including microprocessor and DC-DC converters for battery-powered electronics) are crucial in supplying power to microprocessors and other electronic loads [18]. Digital control ensures precise voltage regulation, high efficiency, and fast dynamic response. Multi-phase architectures with parallel-operating

converter modules are commonly used, with digital control enabling features like digitally programmable output voltage and load-dependent voltage positioning [68].

1.6.2.2 Active Power Factor Correctors

Digital control is employed in PFCs to improve power quality by mitigating harmonics and reducing reactive power [17]. Digital controllers analyze line current waveforms and inject compensating currents to cancel out disturbances, enhancing overall power system efficiency and stability.

1.6.2.3 Uninterruptible Power Supplies

Digital control is vital in ensuring reliable power backup in UPS systems [17]. It enables precise voltage regulation, fast response to load variations, and efficient battery management, ensuring uninterrupted power supply to critical loads during grid failures or fluctuations.

1.7 Thesis Organization

Chapter 2 of the thesis provides a thorough theoretical analysis of Limit-cycle Oscillations (LCOs) in digitally controlled power converters. It examines the impact of quantization effects from the Analog-to-Digital Converter (ADC) and the Digital Pulse Width Modulator (DPWM), outlines quantization characteristics, and suggests methods for determining steady-state DC solutions and conditions to prevent LCOs. Moreover, it reviews the latest DPWM implementation techniques to enhance resolution and mitigate LCO onset. Additionally, it explains Dyadic Digital Pulse Width Modulation (DDPWM) and its spectral properties. Finally, it compares existing hardware implementations of Dyadic Digital Pulse Modulators (DDPM) in terms of complexity and performance, considering their potential software translation.

Chapter 3 emphasizes the difference in DPWM resolution between the Buck and Boost converters regarding output voltage quantization. It calculates the minimum required DPWM resolution for LCO-free operation in the Boost converter. Subsequently, it introduces the first digitally controlled, voltage-mode Boost converter implementation utilizing DDPWM. The effectiveness of DDPWM in attenuating

LCOs onset, improving DC accuracy, and reducing output voltage ripple is validated through Simulink/Modelsim co-simulation and hardware implementation under various operating conditions and ADC/DPWM resolutions.

Chapter 4 proposes a novel optimized DDPM modulator architecture tailored for software (SW) implementation that is compared to existing solutions. The proposed architecture's effectiveness is demonstrated through the SW implementation of an 8-bit DDPM DAC in a general-purpose microcontroller unit, with experimental validation of its operation.

Finally, the thesis concludes with Chapter Conclusion, where some concluding remarks are drawn.

Chapter 2

Limit-Cycle Oscillations in Digitally Controlled Power Converters

This chapter delves into the complexities of nonlinear interactions between the Analog-to-Digital Converter (ADC) and the Digital Pulse Width Modulator (DPWM) in the context of digitally controlled power converters, which can lead to low-frequency steady-state oscillations known as Limit Cycle Oscillations (LCOs). This phenomenon poses significant concerns to digitally controlled regulators' regulation accuracy and performance. The chapter focuses on the origin of limit cycling in digitally controlled power converters. It explores quantization effects and their impact, summarizes quantization characteristics, discusses methods for finding steady-state DC solutions, and proposes conditions to prevent limit cycling. Additionally, it reviews the state-of-the-art DPWM implementation techniques that improve resolution and minimize the onset of LCOs.

2.1 Digital Control of Power Converters

In this section, I will explore digitally controlled synchronous Boost [illustrated in Fig. 2.1(a)] and Buck [illustrated in Fig. 2.1(b)] power converters operating in voltage mode.

These converters consist of two primary stages: the power stage and the digital controller stage. The power stage operates in Continuous Conduction Mode (CCM)

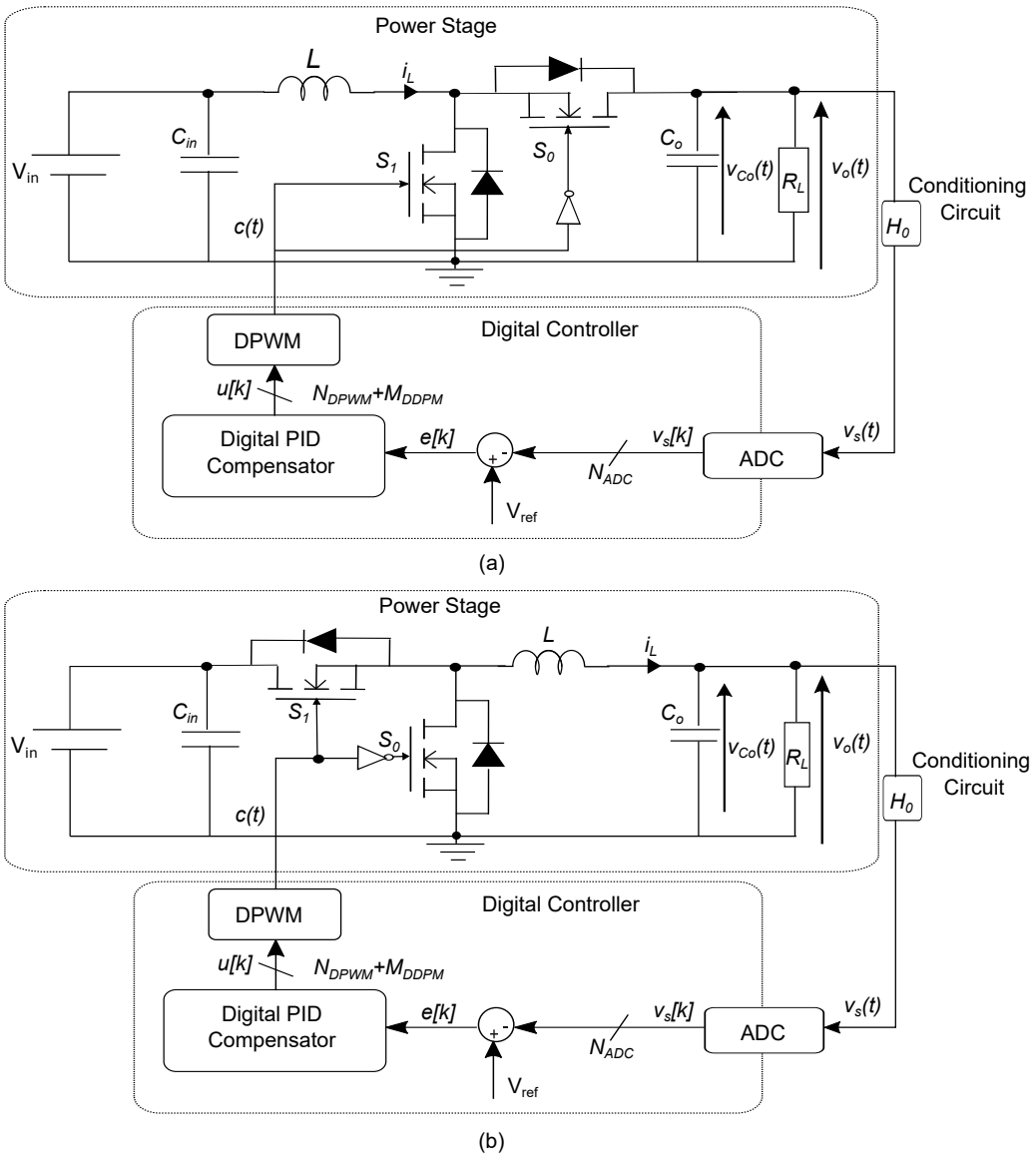

Fig. 2.1 Digitally controlled voltage-mode (a) Boost converter and (b) Buck converter.

and comprises a half-bridge with two Field-Effect Transistors (FETs) switches that alternate between two states: switch-off (S_0) and switch-on (S_1). Additionally, it includes a physical inductor (L), an input capacitor (C_{in}), an output capacitor (C_{o}), and a load resistor (R_{L}). The converter's input voltage is represented as V_{in}, and the output voltage is denoted as v_{o}. The output voltage undergoes signal conditioning in the analog domain, which is depicted by the transfer function $H_0(s)$ of the sensing path, as described in Equation 2.1.

$$v_s(t) = H_0 \cdot v_o(t) \tag{2.1}$$

The sensed output voltage $v_s(t)$ is then converted into a digital sequence $v_s[k]$ via an N_{ADC}-bit resolution ADC, with a sampling period T_{s}. Generally, the sampled version of the sensed signal is $v_s[k] = v_s(kT_{\text{s}})$, where kT_{s} represents the sampling instants.

The control error $e[k]$ is processed by a digital compensator in the digital controller stage. This error is between the internal digital reference V_{ref} and the acquired signal v_s. This digital compensator computes the digital control command $u[k]$ on a per-switching-cycle basis. Subsequently, an N_{DPWM}-bit resolution DPWM generates a modulated output $c(t)$ of duty cycle D by latching $u[k]$ every T_{sw} seconds at the onset of each modulation cycle. This output pulse $c(t)$ drives the half-bridge circuit, and its duration is proportional to $u[k]$.

In addition, the digitized versions of all controller signals are denoted with the superscript 'd' in our discussion. For instance, $v_s^{\text{d}}[k]$ represents the digital output of the ADC, $e[k]$ is the digital error, and $u^{\text{d}}[k]$ is the digital control command.

2.1.1 Discrete-Time Modeling of Power Stage

To achieve high-performance digital control loops, it's crucial to comprehend and account for resulting delays and aliasing effects. While continuous-time averaged modeling is a common practical approach for designing digital loops, it only approximates sampling effects and digital control delays. A more rigorous method involves discrete-time modeling [69], which is detailed below.

Discrete-time modeling aims to describe the dynamics of sampled converter waveforms without any averaging step involved in the process. Consider the converter

operating alternately between two topological states, S_0 and S_1, both modeled by a linear set of state-space equations

$$\begin{aligned} \frac{dx}{dt} &= A_c x(t) + B_c u(t) \\ y(t) &= C_c x(t) \end{aligned} \tag{2.2}$$

where $c \in \{0,1\}$ denotes the PWM signal, while $x(t) = \begin{bmatrix} i_L(t) \\ v_{c_o}(t) \end{bmatrix}$, $u(t) = \begin{bmatrix} V_{\text{in}} \\ \frac{v_{\text{o}}(t)}{R_{\text{L}}} \end{bmatrix}$, and $y(t) = \begin{bmatrix} i_L(t) \\ v_{c_o}(t) \end{bmatrix}$ denote the input, output vectors, and state, respectively. In the context of control-to-output dynamics, the input vector is considered constant, i.e., $u(t) = U = \begin{bmatrix} V_{\text{in}} \\ \frac{V_{\text{o}}}{R_{\text{L}}} \end{bmatrix}$.

A state-space representation in eq. (2.2) can be re-written as

$$\begin{aligned} \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{c_o}}{dt} \end{bmatrix} &= A_c \begin{bmatrix} i_L(t) \\ v_{c_o}(t) \end{bmatrix} + B_c \begin{bmatrix} V_{\text{in}} \\ \frac{V_{\text{o}}}{R_{\text{L}}} \end{bmatrix} \\ \begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} &= C_c \begin{bmatrix} i_L(t) \\ v_{c_o}(t) \end{bmatrix} \end{aligned} \tag{2.3}$$

For a Boost converter, the state space matrices are

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_{\text{L}} C_{\text{o}}} \end{bmatrix}$$

$$A_0 = \begin{bmatrix} 0 & \frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_{\text{L}} C_{\text{o}}} \end{bmatrix}$$

$$B_1 = B_0 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$C_1 = C_0 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

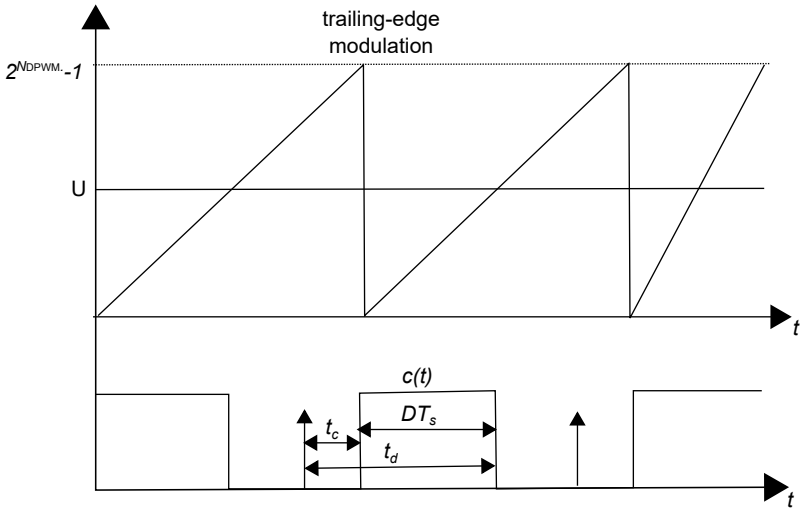

Fig. 2.2 Waveforms illustrating the total control loop delay in discrete-time modeling-trailing-edge modulation.

while for the Buck converter:

$$A_1 = A_0 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_o} & 0 \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix}$$

$$B_0 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix}$$

$$C_1 = C_0 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

Let's assume the implementation of a hardware-based controller, which includes an ADC, a digital compensator, and a trailing-edge DPWM modulator, as depicted in Fig. 2.1. It is believed that the DPWM captures the control command at the onset of each modulation cycle at a specific time known as t_c. This time interval occurs after the voltage $v_s(t)$ has been sampled, as illustrated in Fig. 2.2. Therefore, the entire loop delay is calculated as $t_d = t_c + DT_s$. While considering the converter operation

alternating between two topological states S_0 and S_1, the z-domain small-signal control-to-output transfer matrix $G_{uv}(z)$ is given by [70]:

$$G_{uv}(z) = \frac{v_o(z)}{u(z)} = \delta(zI - \Phi)^{-1}\gamma \tag{2.4}$$

where:

$$\Phi = e^{A_0(T_s - t_d)} e^{A_1 DT_s} e^{A_0(t_d - DT_s)}$$

$$\gamma = \frac{T_s}{2^{N_{DPWM}} - 1} e^{A_0(T_s - t_d)} F$$

$$\delta = C_0$$

$$F = (A_1 X + B_1 V) - (A_0 X + B_0 V)$$

$$X = (I - e^{A_1 DT_s} e^{A_0 DT_s})^{-1} \left[-e^{A_1 DT_s} A_0^{-1} (I - e^{A_0 DT_s}) B_0 - A_1^{-1} (I - e^{A_1 DT_s}) B \right] V.$$

The method used in this modeling enables the creation of compensator transfer functions through digital design. The design specifications are in the frequency domain and involve concepts that analog designers are familiar with, such as the loop-gain crossover frequency denoted as f_c and the phase margin represented by ϕ_m.

2.1.2 ADC Conversion

The term "input quantization" refers to the quantization process performed by the ADC on the analog sensed signal $v_s(t)$. It is commonly used in the field. It is assumed that the converter's effective number of bits is aligned with its hardware resolution N_{ADC} and that there are no significant offset voltage or integral and differential non-linearities present. The process of ADC conversion involves sampling the analog input, followed by amplitude quantization of the acquired sample.

To ensure that there are no sampling artifacts and that the sampling process is synchronized with the power converter's switching operation in the digital domain, it is common practice to restrict the sampling rate to be a multiple of the converter switching frequency, f_{sw}. If the sampling rate of $v_s(t)$ is higher than the converter switching rate, it can cause spectral aliasing of the switching ripple to generate a frequency image below the Nyquist rate. This effect needs to be mitigated by a filtering action performed by the digital controller. In order to avoid spectral aliasing

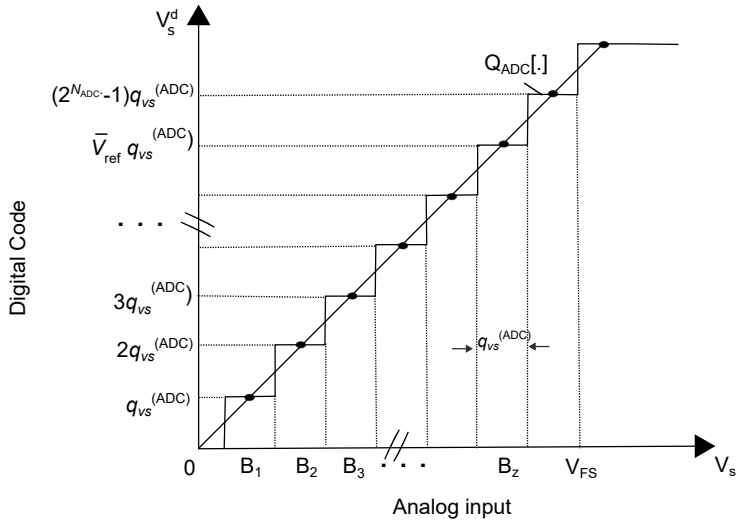

Fig. 2.3 ADC quantization characteristics.

around DC and prevent the creation of images of the original spectrum below the Nyquist rate, it is most common to sample $v_s(t)$ at $f_s = f_{\text{sw}}$. The sampling moment is guaranteed to occur at a consistent fixed position within a switching period, as mentioned in [71].

The ADC has an internal quantizer that works with an analog input range of [0, V_{FS}] and has a resolution of N_{ADC} bits. To calculate the quantization step in $v_s[k]$, one needs to use the following formula:

$$q_{v_s}^{(\text{ADC})} = \frac{V_{\text{FS}}}{2^{N_{\text{ADC}}}} \tag{2.5}$$

The quantized range is divided into $2^{N_{\text{ADC}}}$ voltage intervals B_i, $i = 0, \cdots, 2^{N_{\text{ADC}}} - 1$, commonly referred to as bins. Each bin of the ADC spans $q_{v_s}^{(\text{ADC})}$ volts. The ADC quantization characteristic ($Q_{\text{ADC}}[\cdot]$) is depicted in Fig. 2.3. The digital output $v_s^{\text{d}}[k]$ of the ADC is represented as:

$$v_s^{\text{d}}[k] = Q_{\text{ADC}}[v_s[k]].$$

The resolution N_{ADC} and full-scale range V_{FS} of the ADC are shared by the digital setpoint V_{ref} of the controller:

$$V_{\mathrm{ref}} = q_{v_s}^{(\mathrm{ADC})} \bar{V}_{\mathrm{ref}}$$

where the integer $\bar{V}_{\mathrm{ref}}$ identifies the zero-error bin, which corresponds to the quantization interval B_z to which $v_s^{\mathrm{d}}[k]$ should be regulated.

2.1.3 Digital PID Compensator

The digital circuit known as the compensator calculates the control command $u[k]$ by evaluating the regulation error $e[k]$. A difference equation describes a linear, time-invariant compensation law [71] used in this computation.

$$\begin{aligned} u[k] = &- a_1 u[k-1] - a_2 u[k-2] - \cdots - a_N u[k-N] + \\ &+ b_0 e[k] + b_1 e[k-1] + \cdots + b_M e[k-M] \end{aligned} \tag{2.6}$$

A discrete-time PID compensator is a vital instance of eq. (2.6). It represents the digital equivalent of the renowned analog PID regulators [72]. The equations for a discrete-time PID controller can be obtained by discretizing the differential equations of a continuous-time PID controller. This method is explained in detail in [71].

$$\begin{aligned} u_{\mathrm{p}}[k] &= K_{\mathrm{p}} e[k] \\ u_{\mathrm{i}}[k] &= u_{\mathrm{i}}[k-1] + K_{\mathrm{i}} T_{\mathrm{sw}} e[k] \\ u_{\mathrm{d}}[k] &= \frac{K_{\mathrm{d}}}{T_{\mathrm{sw}}} (e[k] - e[k-1]) \\ u[k] &= u_{\mathrm{p}}[k] + u_{\mathrm{i}}[k] + u_{\mathrm{d}}[k] \end{aligned} \tag{2.7}$$

The z-domain PID transfer function is expressed in eq. (2.8):

$$G_{\mathrm{PID}}(z) = K_{\mathrm{p}} + \frac{T_s K_{\mathrm{i}}}{1 - z^{-1}} + \frac{K_{\mathrm{d}}}{T_s} (1 - z^{-1}) \tag{2.8}$$

It is presented as an equivalent block diagram in Fig. 2.4.

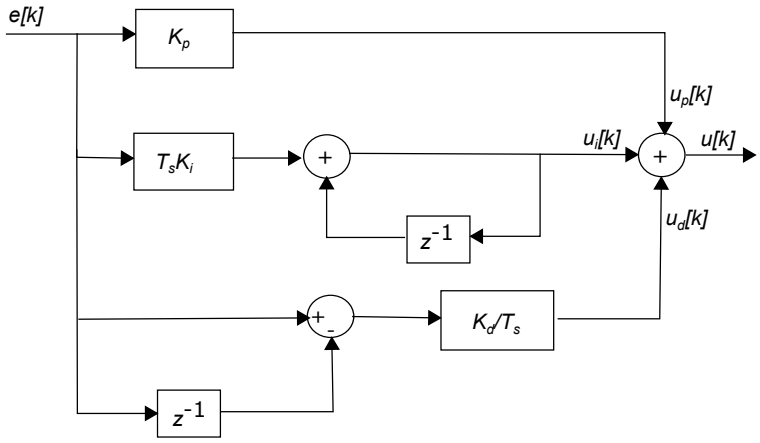

Fig. 2.4 Block Diagram of PID Compensator.

2.1.4 DPWM Modulation

The DPWM, with a precision of N_{DPWM} bits, operates at a clock frequency of $f_{\text{clk}} = 1/T_{\text{clk}}$. It retrieves the control command $u[k]$ on a sampling cycle basis, specifically at each switching period (T_{sw}), and produces a series of pulses with a quantized duty cycle $d[k]$. Consequently, the DPWM functions behaves as a quantizer $Q_{\text{DPWM}}[\cdot]$ on $u[k]$ as depicted in Fig. 2.5 [71], i.e.,

$$d[k] = Q_{\text{DPWM}}[u[k]] \tag{2.9}$$

The resolution bin of duty cycle q_{D} in a standard counter-based DPWM is given by:

$$q_{\text{D}} = \frac{1}{2^{N_{\text{DPWM}}}}. \tag{2.10}$$

From eq. (2.10), the smallest achievable resolution q_u by the DPWM on the command $u[k]$ can be expressed as:

$$q_u = q_{\text{D}} \cdot N_r = \frac{N_r}{2^{N_{\text{DPWM}}}}, \tag{2.11}$$

where $N_r = 2^{N_{\text{DPWM}}} - 1$.

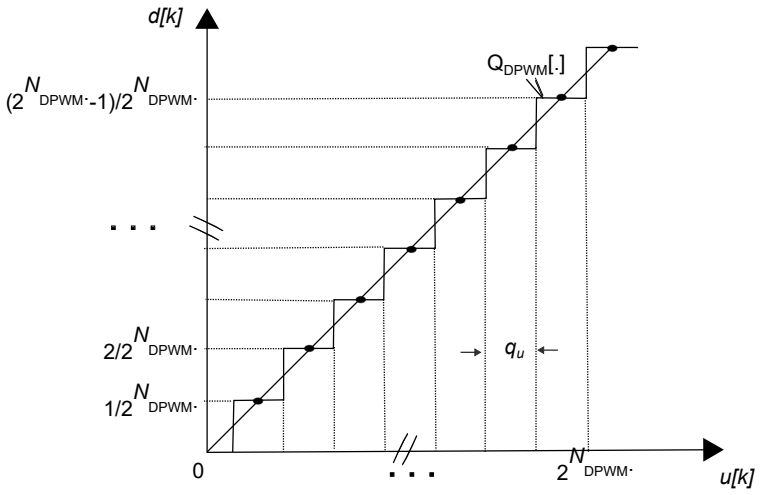

Fig. 2.5 DPWM quantization characteristics.

2.2 Onset of LCOs due to System Quantization Effects

The preceding discussion shows that the fundamental digital control loop shares conceptual similarities with the standard voltage-mode analog PWM control loop. However, it diverges from analog control in two crucial aspects: time quantization and amplitude quantization. Time quantization pertains to the discrete-time nature of the controller, which operates on sampled versions of sensed analog signals for regulation and produces discrete-time control outputs. Conversely, amplitude quantization introduces nonlinear effects that may induce steady-state disturbances, often called limit cycling [73]. These effects and associated design considerations are elaborated in what follows.

2.2.1 ADC Amplitude Quantization

As discussed earlier, the zero-error bin B_z is the specific quantization level at which the sensed signal v_s is to be regulated, as identified by the controller's digital setpoint V_{ref}. Assuming the existence of a steady-state operating point in the closed-loop system where $e^d = 0$, the quantized ADC output v_s^d equals V_{ref}, indicating that the

sampled version of the sensed analog signal lies within the zero-error bin B_z:

$$e^d = V_{\text{ref}} - v_{\text{s}}^d = 0 \rightarrow v_{\text{s}}^d = V_{\text{ref}} \tag{2.12}$$

In an ideal scenario, the controller should achieve and maintain the zero-error bin indefinitely without external disturbances. However, such an operating point is only sometimes guaranteed when quantization is involved. The stability of the steady-state operating point becomes a delicate issue when considering quantizer non-linearities [73].

As a result of quantizing the sensed signal v_s^d, the converter's output voltage v_o undergoes a similar quantization. Therefore, the equivalent output voltage quantization bin, denoted as $q_{v_o}^{(\text{ADC})}$, can be expressed as the width of this quantization.

$$q_{v_o}^{(\text{ADC})} = \frac{q_{v_o}^{(\text{ADC})}}{H_0} = \frac{V_{\text{FS}}}{2^{N_{\text{ADC}}} \cdot H_0} \tag{2.13}$$

where V_{FS}/H_0 defines the equivalent ADC range on the output voltage.

Analog output voltages within a zero-error bin of width $q_{v_o}^{(\text{ADC})}$ generate a zero digital error signal ($e^d = 0$), indicating that the $q_{v_o}^{(\text{ADC})}$ determines the precision of output voltage regulation by the digital control loop. In order to guarantee that $q_{v_o}^{(\text{ADC})}$ is below $\varepsilon\%$ of the nominal output voltage V_{ref}/H_o, a minimum resolution necessary for the ADC is:

$$N_{\text{ADC}} > \log_2\left(\frac{100}{\varepsilon}\right) + \log_2\left(\frac{V_{FS}}{V_{ref}}\right) \tag{2.14}$$

In actual designs, the effective number of bits (ENOB) of the ADC needs to be considered.

2.2.2 DPWM Quantization

In accordance with our previous discussion, the DPWM generates pulses that have a quantized duty cycle, as given in eq. (2.9) and shown in Fig. 2.5. This means that the on-time T_{on} of the switching period is limited to an integer multiple of T_{clk}, which results in a quantized duty cycle $D = T_{\text{on}}/T_{\text{sw}}$. This, in turn, leads to a corresponding quantization of the steady-state converter output voltage.

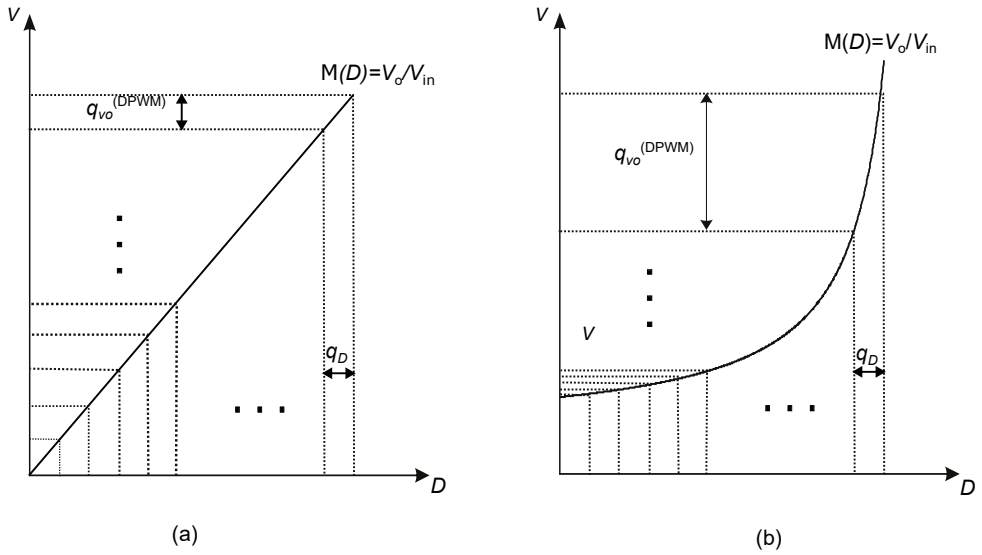

Fig. 2.6 DPWM quantization in terms of output voltage with respect to duty cycle resolution for (a) buck converter and (b) boost converter.

Determining the steady-state output voltage produced by a quantized constant duty cycle for a converter with a conversion ratio $\mathrm{M}(D) = V_\mathrm{o}/V_\mathrm{in}$ as:

$$V_\mathrm{o}(D) = \mathrm{M}(D) \cdot V_\mathrm{in} \tag{2.15}$$

However, the quantization of V_o is generally non-uniform since $\mathrm{M}(D)$ depends on D and so does the converter's operating point. The smallest variation in duty cycle (q_D) resulting in the smallest variation in output voltage, denoted as $q_{v_\mathrm{o}}^{(\mathrm{DPWM})}$ is expressed as [73]:

$$q_{v_\mathrm{o}}^{(\mathrm{DPWM})} \approx \frac{\partial M}{\partial D} \cdot q_\mathrm{D} \cdot V_\mathrm{in} \tag{2.16}$$

For a Boost converter with $\mathrm{M}(D) = \frac{1}{1-D}$ [74], the eq. (2.16) becomes

$$q_{v_\mathrm{o}}^{(\mathrm{DPWM})} \approx \frac{1}{(1-D)^2} \cdot \frac{1}{2^{N_\mathrm{DPWM}}} \cdot V_\mathrm{in} \tag{2.17}$$

which depends on D, having finer quantization steps for lower duty-cycle values and larger steps as the duty cycle increases, as shown in Fig. 2.6(b).

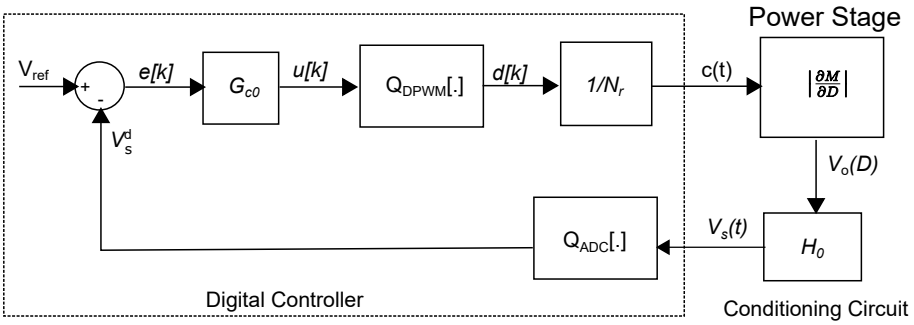

Fig. 2.7 Digitally controlled converter DC model.

Conversely, for a Buck converter, $\mathrm{M}(D) = D$ [74], the eq. (2.16) becomes

$$q_{v_\mathrm{o}}^{(\mathrm{DPWM})} \approx \frac{1}{2^{N_\mathrm{DPWM}}} \cdot V_\mathrm{in}, \tag{2.18}$$

which is independent of D, and the change in output voltage variations is directly proportional to the change in the duty cycle variations, as shown in Fig. 2.6(a).

2.2.3 Existence of LCOs

Consider a DC model of a digitally controlled power converter, as shown in Fig. 2.7, to find the steady-state solution, where the controller variables remain constant, and the converter waveforms become periodic, with a period equivalent to the switching period. The model takes into account ADC ($Q_\mathrm{DPWM}[.]$) and DPWM ($Q_\mathrm{ADC}[.]$) quantization, represents the discrete-time compensator by its DC gain G_c0, and the power stage by slope voltage conversion ratio $\left(\left|\frac{\partial M}{\partial D}\right|\right)$. Finally, H_0 denotes the conditioning circuit DC gain.

2.2.3.1 Ideal Case

Assuming first that both the ADC and DPWM resolution is very high, i.e., $q_{v_s}^{(\mathrm{ADC})} \approx 0$ and $q_u \approx 0$. The ADC quantization characteristic becomes simply:

$$V_s^\mathrm{d} = V_s \tag{2.19}$$

The V_s obtained through the block diagram of Fig. 2.7 is,

$$V_s = \left|\frac{\partial M}{\partial D}\right| \frac{H_0 V_{\text{in}} G_{\text{c0}}}{N_r}(V_{\text{ref}} - V_s^{\text{d}}) \tag{2.20}$$

For a Buck converter $\text{M}(D) = D$, the eq. (2.20) becomes

$$V_s = \frac{H_o V_{\text{in}} G_{\text{c0}}}{N_r}(V_{\text{ref}} - V_s^{\text{d}}) \tag{2.21}$$

by inserting eq (2.19) in (2.21), we can obtain the steady-state DC output voltage, V_o, as

$$V_o = \frac{V_s^{\text{d}}}{H_0} = \frac{V_{\text{ref}}}{H_0} \frac{\frac{H_0 V_{\text{in}} G_{\text{c0}}}{N_r}}{1 + \frac{H_0 V_{\text{in}} G_{\text{c0}}}{N_r}} \tag{2.22}$$

In eq. (2.21), it can be observed that a non-zero DC regulation error arises when the DC compensator gain (G_{c0}) takes on a finite value. However, this error can be eliminated by using an infinite DC compensator gain (i.e., $G_{\text{c0}} \to \infty$), which can be accomplished by incorporating integral action in the compensator (i.e., with $K_{\text{i}} > 0$). This results in a very high compensator gain [73], allowing eq. (2.22) to be expressed as follows:

$$V_o \approx \frac{V_{\text{ref}}}{H_o} \tag{2.23}$$

This equation corresponds to a zero DC error.

On the other hand, in a Boost converter with $\text{M}(D) = \frac{1}{1-D}$, the steady-state DC output voltage can be derived as

$$V_o = \frac{V_s^{\text{d}}}{H_0} = \frac{V_{\text{ref}}}{H_0} \frac{\frac{H_0 V_{\text{in}} G_{\text{c0}}}{(1-D)^2 N_r}}{1 + \frac{H_0 V_{\text{in}} G_{\text{c0}}}{(1-D)^2 N_r}} \tag{2.24}$$

2.2.3.2 Practical Case

Now, assuming the finite resolution ADC and DPWM of width $q_{v_s}^{(\text{ADC})}$ and q_u, respectively, the ADC quantization characteristic can be expressed as

$$V_s^{\text{d}} = Q_{\text{ADC}}[V_s] \tag{2.25}$$

The value of V_s obtained through the block diagram of Fig. 2.7 is given by

$$V_s = \left|\frac{\partial M}{\partial D}\right| \frac{H_0 V_{\text{in}}}{N_r} Q_{\text{DPWM}}[G_{\text{c0}}(V_{\text{ref}} - V_s^{\text{d}})] \tag{2.26}$$

Again, if the compensator DC gain, G_{c0}, is finite, it results in a non-zero DC regulation error. However, this solution may not be feasible due to vertical steps in ADC quantization characteristics. After analyzing the situation, the compensator would have a significant but limited DC gain, which means that the digitally controlled converter could not remain in a fixed equilibrium point. As a result, the controller would be responsible for oscillating the output voltage through multiple bins, including the zero-error bin, leading to limit cycling. This phenomenon is demonstrated in Fig. 2.8.

By incorporating the integral gain, the compensator gain becomes infinite [73] (i.e., $G_{c0} \to \infty$), which makes the width of the vertical quantization steps vanish to zero (i.e., $q_u/G_{\text{c0}} \to 0$). In such cases, multiple equilibrium solutions may exist within the ADC zero-error bin B_{z}.

It is worth noting that the condition for the existence of multiple equilibrium solutions is determined by the presence of an integral action in the compensator (i.e., $K_i > 0$) and the width of DPWM quantization bin being shorter than those of the ADC, i.e.,

$$\frac{H_0 V_{\text{in}} q_u}{N_r} < q_{v_s}^{(ADC)} \tag{2.27}$$

If the condition stated in eq.(2.27) is not satisfied, it is uncertain whether a stable solution exists or not. The existence of a DPWM quantized sensed output voltage V_s within the ADC zero-error bin determines the possibility of a steady-state solution. If there is no such point, the control loop causes the output voltage to oscillate back and forth between two or more bins surrounding the zero-error bin, leading to limit cycling. To achieve a state where all controller variables maintain constant values, ensuring that a DC solution exists within the zero-error bin of the ADC [2] is crucial.

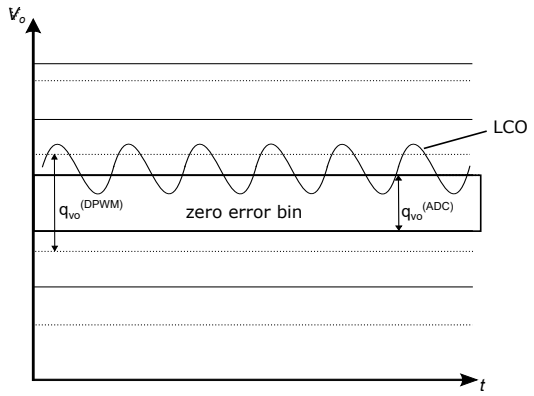

Fig. 2.8 Limit cycle oscillations at the output voltage of the converter.

2.3 LCOs free Operation Guidelines

Based on the insights gained from the analysis in Section 2.2, a steady-state solution within the zero-error bin of the ADC is essential for preventing limit cycling. In this section, the necessary conditions to prevent limit cycling will be presented, considering factors such as DPWM and ADC resolution, as well as determining the integral gain K_i.

2.3.1 DPWM versus ADC Resolution

To ensure the existence of a DC solution within the zero-error bin of the ADC, the first of these conditions is that the DPWM quantization interval in terms of output voltage $q_{\mathrm{v_o}}^{(\mathrm{DPWM})}$ should be smaller than the ADC quantization interval in terms of output voltage $q_{\mathrm{v_o}}^{(\mathrm{ADC})}$, i.e.,

$$q_{\mathrm{v_o}}^{(\mathrm{DPWM})} < q_{\mathrm{v_o}}^{(\mathrm{ADC})}. \tag{2.28}$$

If condition (2.28) is not met, then none of the $q_{\mathrm{v_o}}^{(\mathrm{DPWM})}$ levels will be inside the zero-error bin of the ADC, as depicted in Fig. 2.9(a). The output cannot be within the zero-error bin, and instead, it will vary between two or more duty-cycle levels. As a result, the output voltage will be around the zero-error bin, leading to

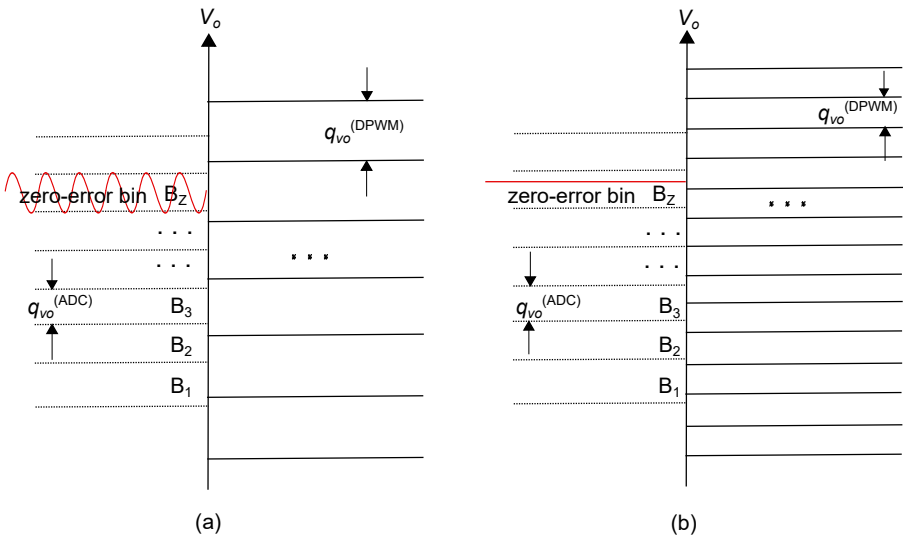

Fig. 2.9 ADC quantization bins and DPWM quantization levels.

the presence of low-frequency LCOs. In contrast, if we abide by (2.28), as shown in Fig. 2.9(b), we can eliminate the limit cycle [2, 73].

2.3.2 Integral Gain

Recalling condition (2.28) is essential, which relies on the assumption of integral action in the compensator ($K_i > 0$). However, even if (2.28) is satisfied, limit cycling can still occur due to excessively large integral gain K_i. This is because the ADC quantization, combined with the integral action in the compensator, leads to effective steady-state quantization of the duty cycle command $u[k]$.

At a steady state condition ($e[k] = 0$), imagine a digital PID compensator with only an integral term $u_i[k]$. This term accumulates all previous regulation errors, meaning that it contains the sum of all past errors. i.e.,

$$u[k] = u_i[k] = K_i \sum_{n=1}^{k} e[n] \tag{2.29}$$

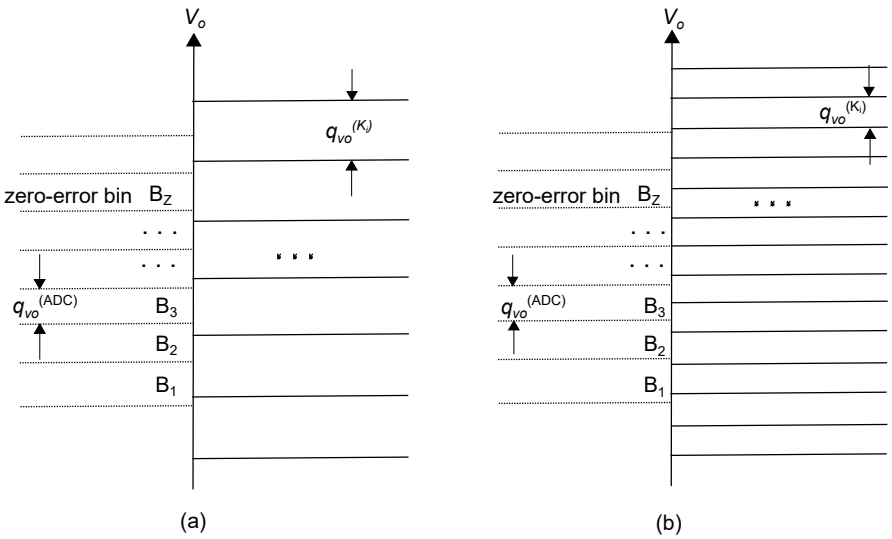

Fig. 2.10 ADC quantization bins and integral term quantization levels.

Due to the quantization of ADC, the error in regulation is also quantized as $e[n]q_{v_s}^{(\mathrm{ADC})}$. As a result, eq. (2.29) is modified as

$$u_i[k] = K_i \left(\sum_{n=1}^{k} e[n] \right) q_{v_s}^{(ADC)} \tag{2.30}$$

It means that the inherent quantization of steady state command ($u_i[k]$) is determined as,

$$q_u^{(K_i)} = K_i q_{v_s}^{(ADC)} = K_i H_0 q_{v_o}^{(ADC)} \tag{2.31}$$

which in terms of output voltage quantization can be expressed as

$$q_{v_o}^{(K_i)} = G_{vu0} K_i H_0 q_{v_o}^{(ADC)} \tag{2.32}$$

Again, to ensure the steady state solution, at least one quantization level must reside in the zero-error bin, i.e.,

$$q_{v_o}^{(K_i)} < q_{v_o}^{(ADC)} \tag{2.33}$$

Fig. 2.10(a) shows that if the constraint is not met, no DPWM level is present inside the zero-error ADC bin, resulting in limit cycling. To avoid this situation, it is possible to decrease the integral gain K_i until each ADC bin can be reached by a

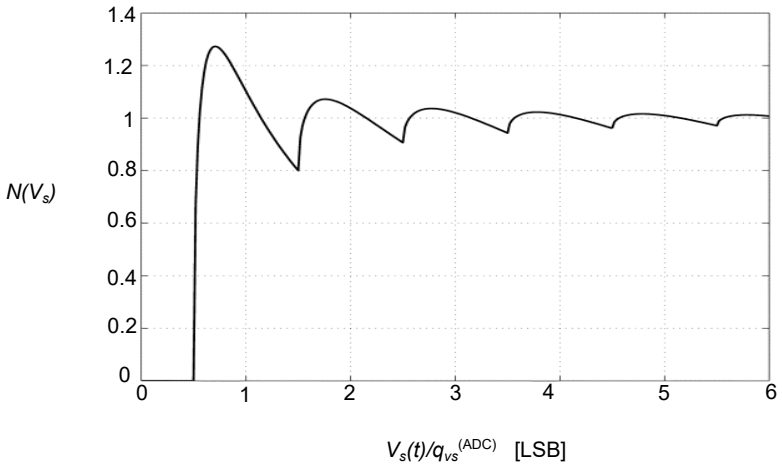

Fig. 2.11 Describing function of a round-off quantizer with zero DC bias [2].

DPWM level. This condition is demonstrated in Fig. 2.10(b). By substituting (2.32) in (2.33), it is possible to derive a no-limit-cycling condition involving the integral gain, as described in [2, 73].

$$G_{vu0}K_iH_0 < 1 \tag{2.34}$$

2.3.3 Dynamic Quantization Effects

It is worth noting that the conditions specified may not be enough to fully get rid of steady-state limit cycles, as the feedback loop's quantizers' discrete characteristics can still cause limit cycling, especially when loop gains are high. To overcome this limitation, nonlinear system analysis methods can be used to determine the maximum allowable loop gain without inducing limit cycles [73]. One of these methods involves analyzing the ADC's describing function, which represents its effective gain relative to the input signal amplitude and DC bias.

Only limit cycles with a zero DC component can be considered stable if the feedback control law includes an integral term. This is because the integrator component drives the DC component of the error signal toward the bin of zero error. To assess the stability of a system, the describing function of a round-off quantizer with zero DC bias, denoted as $N(V_s)$ and illustrated in Fig. 2.11 [2], is utilized. The maximum effective gain of the ADC corresponds to a maximum value of approximately 1.3, which is illustrated in the plot of the describing function.

In designing the control law for the system, the effective gain of the ADC must be incorporated into the loop gain calculations to prevent limit cycles, i.e.,

$$1 + N(V_s)L(j\omega) \neq 0 \tag{2.35}$$

where $L(j\omega)$ is the loop gain from output (V_s^{d}) to input (V_s) of the ADC.

While the conditions (2.34) and (2.35) are not difficult to meet by design with convenient PID coefficients, condition (2.28) demands a high resolution for both the ADC and DPWM, thus poses a greater challenge. Therefore, condition (2.28) will be considered in our discussion in what follows while assuming that the other two conditions are already satisfied.

2.4 High-resolution DPWM Techniques

As we discussed earlier, high-resolution DPWM and ADC are necessary to achieve accurate regulation and reduce limit cycling oscillations in digitally controlled converters. This section summarizes various DPWM implementation techniques specifically designed for high-frequency switched-mode power converters.

2.4.1 Standard Counter-based DPWM

The counter-based DPWM represents the most basic DPWM architecture, consisting only of an n-bit counter and an n-bit digital comparator, as illustrated in Fig. 2.12(a), and its timing waveform is illustrated in Fig. 2.12(b). In this setup, the PID compensator's digital command u is latched into the DPWM input register and held constant throughout the switching period T_{sw}. The counter, which is clocked at frequency $f_{\mathrm{clk}} = 1/T_{\mathrm{clk}}$, increments at each positive edge of the clock, and generates a PWM carrier denoted as $r[nT_{\mathrm{sw}}]$. The content of the register u_h and $r[nT_{\mathrm{sw}}]$ are directed to the inputs of the digital comparator. The comparator output remains in a high-level state until the $r[nT_{\mathrm{sw}}]$ reaches or exceeds u_h, hence generating a pulse $c(t)$ with width proportional to the u.

An N_{DPWM}-bit counter-based DPWM structure requires a clock frequency of

$$f_{\mathrm{clk}} = 2^{N_{\mathrm{DPWM}}} f_{\mathrm{sw}} \tag{2.36}$$

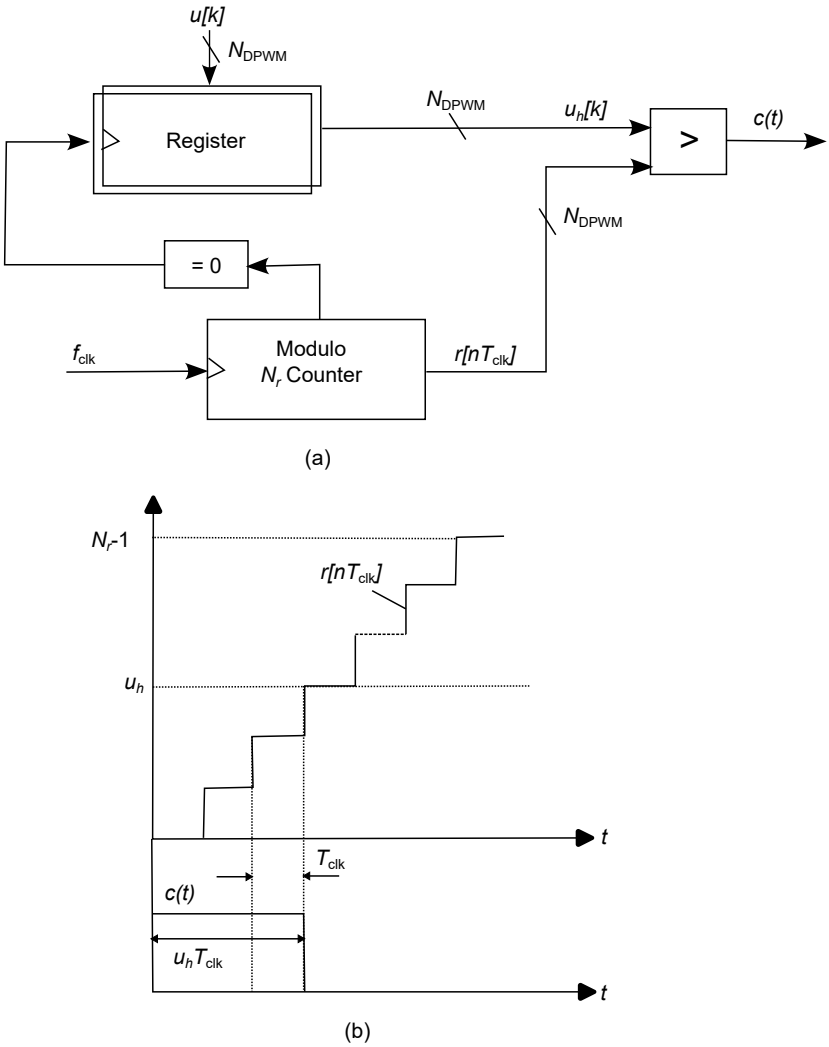

Fig. 2.12 Standard Counter-based DPWM (a) DPWM Architecture (b) timing waveforms.

which can be represented inversely as

$$N_{\text{DPWM}} = \log_2\left(\frac{f_{\text{clk}}}{f_{\text{sw}}}\right). \tag{2.37}$$

The duty cycle (D) of the counter-based DPWM is defined as:

$$D = \frac{T_{\text{on}}}{T_{\text{sw}}} = \frac{u_h}{2^{N_{\text{DPWM}}}} \tag{2.38}$$

where T_{on} represents the on-time of the PWM pulse, $c(t)$, controlled by the value of u_h ranging from 0 to $2^{N_{\text{DPWM}}} - 1$.

The resolution of the counter-based DPWM in eq. (2.37) is directly proportional to the clock frequency, making it unsuitable for high-resolution implementations due to the requirement of a higher clock frequency.

As a result, it can be said that meeting condition (2.28) to avoid LCOs requires a trade-off among f_{clk}, f_{sw}, and N_{ADC}. A lower value of N_{ADC} leads to DC voltage inaccuracies in the output. For instance, considering $f_{\text{clk}} = 100$ MHz and $f_{\text{sw}} = 3$ MHz, the required N_{DPWM} is calculated to be 5-bits. To meet (2.28), N_{ADC} should ideally be less than 5-bits, which is quite low for most practical applications. Conversely, for high DC accuracy ($N_{\text{ADC}} = 8$ bits or higher) and a switching frequency of $f_{\text{sw}} = 3$ MHz, a clock frequency of greater than $f_{\text{clk}} = 1.5$ GHz is required, which is impractically high.

Even though multiple counterclocks can be used in conjunction to improve the DPWM resolution, this approach requires high-frequency Phase-Locked Loops (PLLs), which can be difficult to implement in practical scenarios [75].

Various alternative techniques have been proposed to effectively increase the DPWM resolution without increasing the clock frequency [76]. A brief overview of the state-of-the-art techniques is presented in what follows.

2.4.2 Delay Line DPWM Architecture

Architectures that have precise timing as their main goal use a series of delay cells known as delay lines instead of relying solely on a high-frequency clock. An illustration of a basic M_{Delay}-bit delay-line DPWM architecture is shown in Fig. 2.13(a), while its timing waveform is demonstrated in Fig. 2.13(b). Towards the

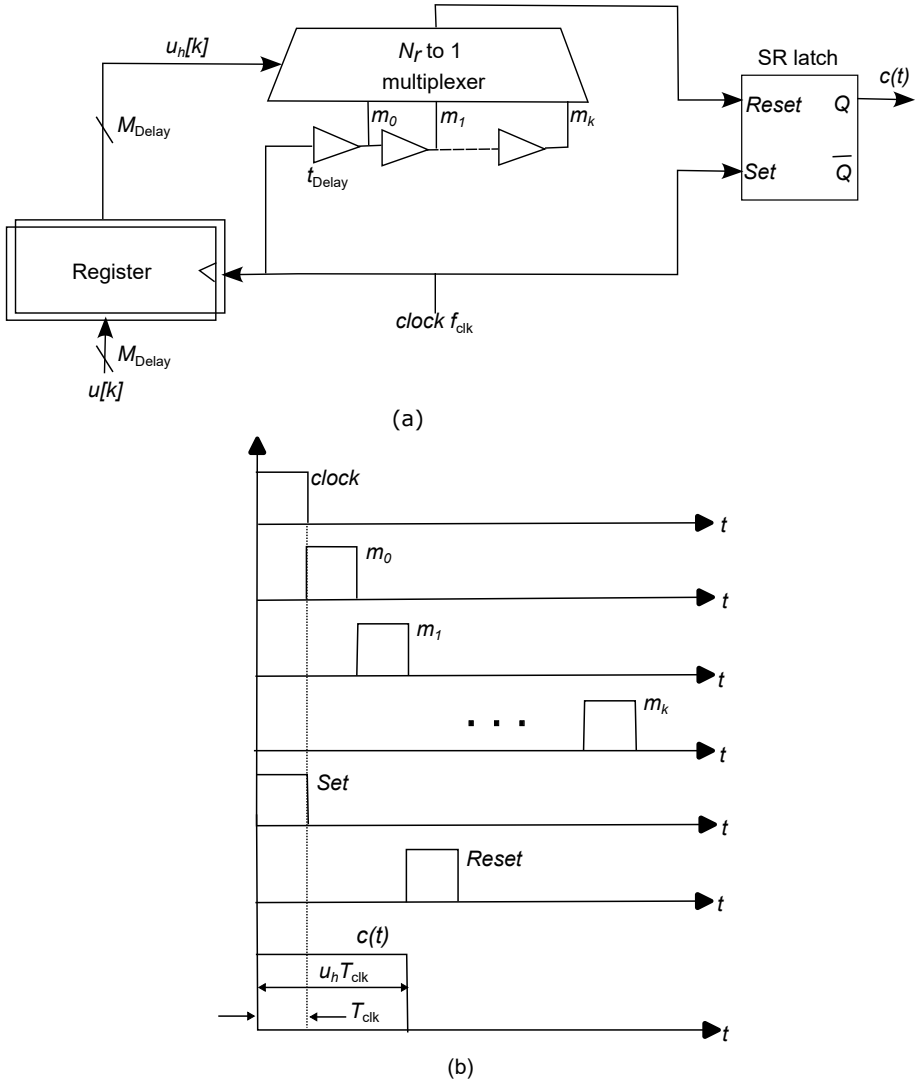

Fig. 2.13 Delay Line (a) DPWM Architecture (b) timing waveforms.

beginning of every switching period, a clock signal that matches the switching frequency ($f_{\text{clk}} = f_{\text{sw}}$) triggers an output latch. This clock signal passes through a delay line, causing a delay between consecutive taps m_k, with a cell delay of t_{Delay}. A digital control command, $u_h = u$, selects a specific tap to reset the output signal using a $2^{M_{\text{Delay}}}$ to 1 multiplexer. The delay line's delay determines the pulse width of the output signal, which offers high-resolution time quantization.

The delay line method allows for greater flexibility in timing resolution as compared to counter-based systems, which rely on clock periods. However, challenges arise in matching desired switching periods by adjusting the delay. These challenges

can be addressed by closing the delay line into a self-oscillating ring or using a Delay-Locked Loop (DLL) to modify the delay. As the number of bits increases, the delay line's length and the multiplexer's size grow exponentially, which limits its scalability [71, 76, 77].

Hybrid architectures that combine counter-based and delay-line methods are used to address this limitation. In these architectures, the control command u is split into two parts: the M_{Delay} least significant bits (LSBs), containing $u_{h,L}$, is used for the delay-line portion, while the remaining N_{DPWM} most significant bits (MSBs), containing $u_{h,M}$, are assigned to the counter-based portion, as shown in Fig. 2.14(a), while Fig. 2.14(b) shows the simplified timing waveforms. The counter increments with each clock cycle, and when it reaches zero, the latch is triggered to set to "one", initiating $c(t)$. The counter's output is compared with $u_{h,M}$ to produce a pulse $m(t)$, which is sent through the delay line. Each output of the delay cells is tapped out and directed into a multiplexer. The output pulse is extended by $u_{h,L}t_{Delay}$, and the multiplexer's output selection is determined by $u_{h,L}$. The duty cycle of the output pulse $c(t)$ is equal to

$$D = \left(u_{h,M} + \frac{u_{h,L}}{2^{M_{\text{Delay}}}}\right)\frac{T_{\text{clk}}}{T_{\text{sw}}} = \frac{u_{h,M}2^{M_{\text{Delay}}} + u_{h,L}}{2^{M_{\text{Delay}}+N_{\text{DPWM}}}} \tag{2.39}$$

There is a trade-off between delay-line and counter-based methods when balancing size and clock rate requirements. However, the implementation issues related to clock and delay-line synchronization, delay matching, and circuit layout require precise consideration and are sensitive to variations in process and temperature [71]. To synchronize its operation with an external clock, an analog PLL or DLL can be used to adjust the delay within the delay line of a DPWM [78]. These techniques work well for traditional synthesizable hardware-description language digital designs, but they are not practical to use on an FPGA. Another option is to use a DSP-based digital controller to improve DPWM precision, but this strategy requires substantial hardware resources and complicated DSP control. These facts have been reported in the literature [76, 79].

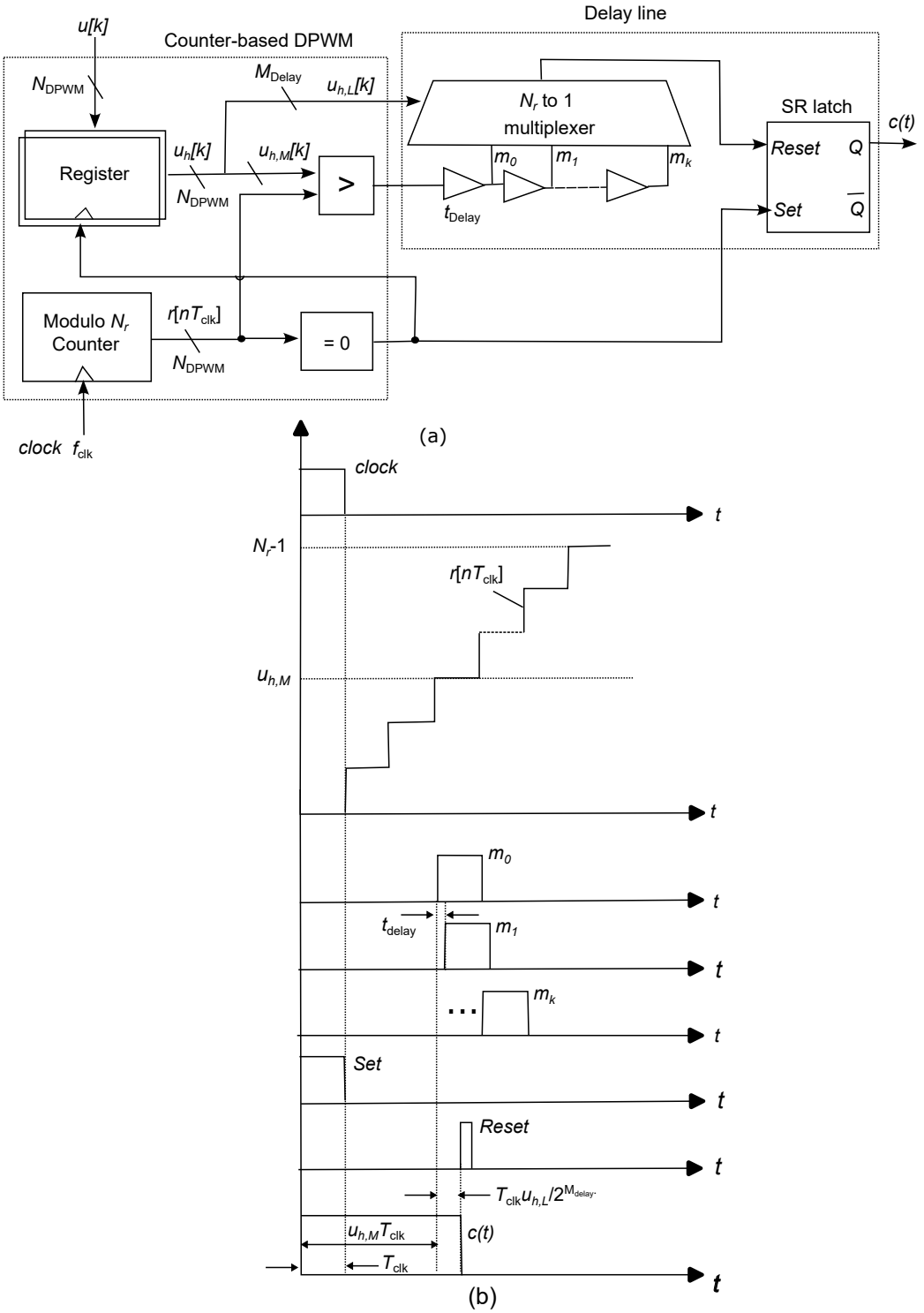

Fig. 2.14 Hybrid Delay Line (a) DPWM Architecture (b) timing waveforms.

2.4.3 Digital Dithering-based DPWM

Digital dithering is one method to enhance the effective resolution of a DPWM module. This technique involves adjusting the duty cycle by one LSB over several switching periods. As a result, it produces an average duty cycle lying between two adjacent quantized duty cycle levels [2].

To carry out dithering, we use D_1 and D_2 to denote two adjacent quantized duty cycle levels produced by the DPWM module, where $D_2 = D_1 + LSB$. By alternating the duty cycle between D_1 and D_2 every other switching period, we can achieve an average duty cycle over time of $(D_1 + D_2)/2 = D_1 + (1/2)LSB$. This way, we can obtain an intermediate (1/2) LSB level by averaging over two switching periods, thus effectively increasing the DPWM resolution by 1-bit.

2.4.3.1 Digital thermometric dithering based DPWM (DTDPWM)

The DTDPWM method is applied to improve the resolution of a N_{DPWM}-bit DPWM to $N_{\text{DPWM}} + M_{\text{DTD}}$ bits. The process is explained in Fig. 2.15(a), and its timing waveform is shown in Fig. 2.15(b) for a digital command, u, which is obtained from PID compensator, and is divided into N_{DPWM} MSBs used for representing the number $u_{h,M}$ and M_{DTD} LSBs containing $u_{h,L}$. The M_{DTD}-bit DTD modulator operates at $f_{\text{clk}}/2^{N_{\text{DPWM}}}$, and generates DTD signal based on input, $u_{h,L}$, to DTD. The DTD signal whose value is either "zero" or "one" is then added to $u_{h,M}$, and the obtained resultant signal is input to a counter-based N_{DPWM}-bit DPWM modulator operated at f_{clk}. It eventually generates the duty cycle, which is $D_1 = (u_{h,M} + 1)/2^{N_{\text{DPWM}}}$ for the first $u_{h,L}$ switching periods and $D_2 = (u_{h,M})/2^{N_{\text{DPWM}}}$ for the remaining $(2^{M_{\text{DTD}}} - u_{h,L})$ switching periods. Therefore, an average duty cycle of

$$D = \frac{u_{h,M} \cdot 2^{M_{\text{DTD}}} + u_{h,L}}{2^{N_{\text{DPWM}} + M_{\text{DTD}}}} \tag{2.40}$$

is achieved over $2^{M_{\text{DTD}}}$ switching periods, which effectively increases the resolution of DPWM from N_{DPWM} to $N_{\text{DPWM}} + M_{\text{DTD}}$. For instance, for 8-bit duty cycle $D = \frac{108}{256}$, splitted in to 4-most significant bits ($N_{\text{DPWM}} = 6$) and 4-least significant bits ($M_{\text{DTD}} = 12$), the average duty cycle ($D = \frac{7}{16} \cdot \frac{12}{16} + \frac{6}{16} \cdot \frac{4}{16} = \frac{108}{256}$) is achieved over $2^4 = 16$ switching cycles.

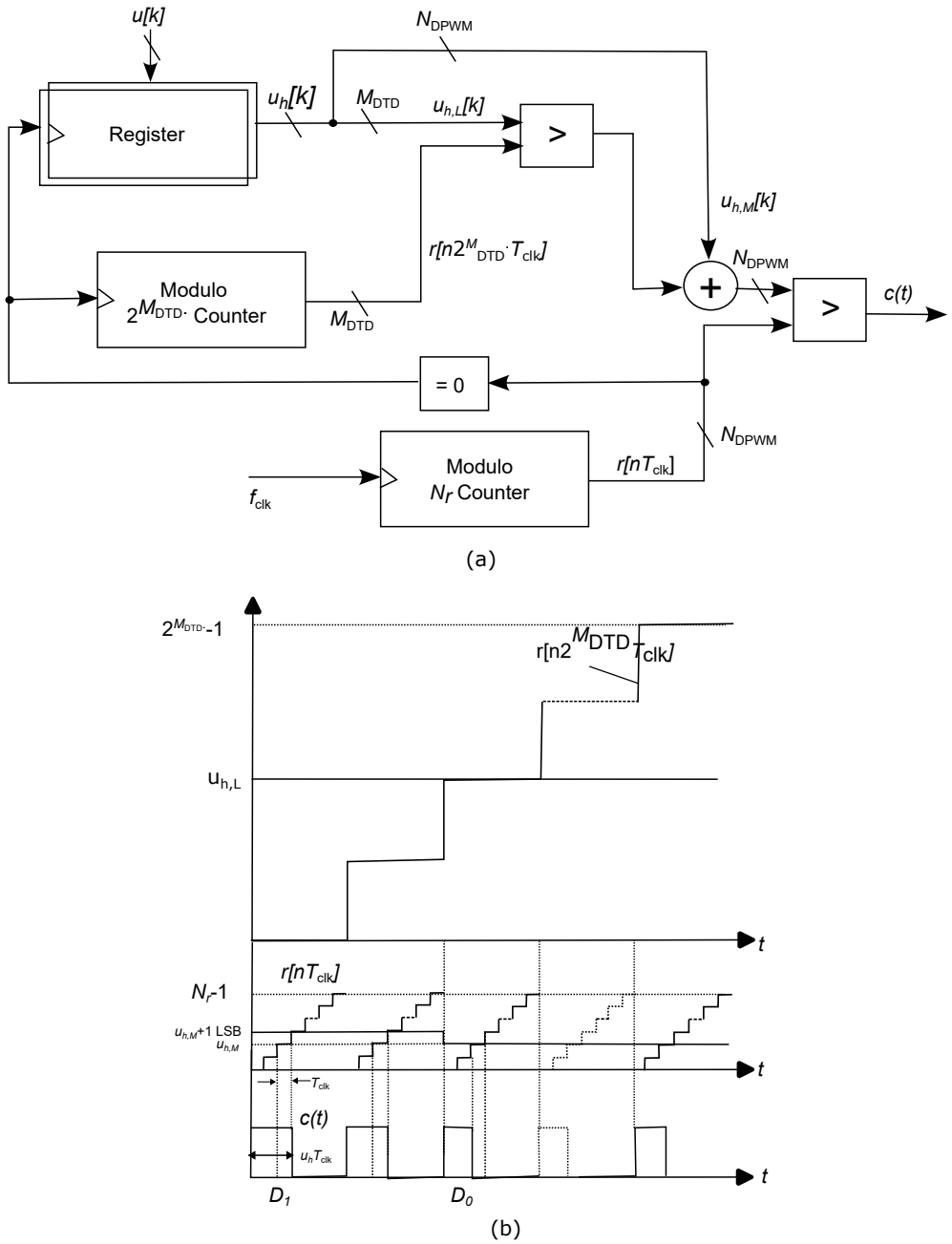

Fig. 2.15 Digital thermometric dithering (a) Architecture (b) timing waveforms.

2.4.3.2 Spectral Analysis of an $N_{\mathbf{DPWM}} + M_{\mathbf{DTD}}$ DTDPWM Signal

The frequency spectrum of an $N_{\mathrm{DPWM}} + M_{\mathrm{DTD}}$-bit DTDPWM signal, presented in [80], is briefly described in what follows.

A DTDPWM signal can be represented as:

$$x_{n,m}^{\mathrm{DTDPWM}}(t) = x_n^{\mathrm{DPWM}}(t) + x_{m,n}^{\mathrm{DTD}}(t) \tag{2.41}$$

where,

$$x_{m,n}^{\mathrm{DTD}}(t) = x_m^{\mathrm{DTD}}(t)\left[x_{n+1}^{\mathrm{DPWM}}(t) - x_n^{\mathrm{DPWM}}(t)\right] \tag{2.42}$$

where, $x_{n+1}^{\mathrm{DPWM}}(t) - x_n^{\mathrm{DPWM}}(t)$ denotes the difference between DPWM waveforms with a duty cycle of $(n-1)/2^{N_{\mathrm{DPWM}}}$ and $n/2^{N_{\mathrm{DPWM}}}$ and a period of T_{sw}, and $x_m^{DTD}(t)$ is a DTD signal with a period of $2^{M_{\mathrm{DTD}}}T_{\mathrm{sw}}$ and a duty cycle of $m/2^{M_{\mathrm{DTD}}}$.

Using eq. (2.41), the spectrum of $x_{n,m}^{\mathrm{DTDPWM}}(t)$ can be expressed as:

$$X_{n,m}^{\mathrm{DTDPWM}}(f) = X_n^{\mathrm{DPWM}}(f) + X_{m,n}^{\mathrm{DTD}}(f) \tag{2.43}$$

where $X_n^{\mathrm{DPWM}}(f)$ is the spectrum of an $N_{\mathrm{DPWM}}-$bit DPWM signal at frequency f_{sw} with a constant duty cycle $n/2^{N_{\mathrm{DPWM}}}$, given by:

$$X_n^{\mathrm{DPWM}}(f) = \frac{n}{2^{N_{\mathrm{DPWM}}}} \sum_{k=-\infty}^{+\infty} \mathrm{sinc}\left(\frac{kn}{2^{N_{\mathrm{DPWM}}}}\right) \mathrm{e}^{-\frac{j\pi kn}{2^{N_{\mathrm{DPWM}}}}} \delta\left(f - kf_{\mathrm{s}}\right) \tag{2.44}$$

and

$$X_{m,n}^{\mathrm{DTD}}(f) = \sum_{k=-\infty}^{+\infty} b_{k,n} d_{k,m} \delta\left(f - k\frac{f_{\mathrm{sw}}}{2^{M_{\mathrm{DTD}}}}\right) \tag{2.45}$$

where

$$b_{k,n} = \frac{1}{2^{N_{\mathrm{DPWM}}+M_{\mathrm{DTD}}}} \mathrm{sinc}\left(\frac{k}{2^{N_{\mathrm{DPWM}}+M_{\mathrm{DDPM}}}}\right) \mathrm{e}^{-\frac{j\pi k\left(2^{N_{\mathrm{DPWM}}}+n\right)}{2^{N_{\mathrm{DPWM}}+M_{\mathrm{DDPM}}}}} \tag{2.46}$$

and

$$d_{k,m} = \frac{m}{2^{M_{\mathrm{DTD}}}} \mathrm{sinc}\left(\frac{km}{2^{M_{\mathrm{DTD}}}}\right) \mathrm{e}^{-\frac{j\pi km}{2^{M_{\mathrm{DTD}}}}}. \tag{2.47}$$

DTD is easy to implement and highly controllable. However, it generates an additional AC ripple at the LC filter's output, which combines with the ripple produced by the converter's switching action. This combined ripple cannot be

filtered out effectively [81]. To prevent problems such as poor output regulation, EMI, and LCOs resulting from the interaction between the ripple produced by the dithering and the ADC, it is crucial to minimize the amplitude of this ripple. Therefore, choosing a suitable dithering pattern that reduces the ripple's amplitude is beneficial.

Another approach to generating a dithering pattern involves utilizing Sigma-Delta ($\Sigma-\Delta$) modulation.

2.4.4 Sigma-Delta ($\Sigma\Delta$) modulation-based DPWM

The operation of $\Sigma-\Delta$ is based on the concept of noise-shaping, a technique commonly used in analog-to-digital and digital-to-analog converters [82, 83]. It is made up of a low-resolution DPWM that can operate at high switching frequencies and a $\Sigma-\Delta$ modulator that improves the effective resolution of the counter-based DPWM from N_{DPWM}-bit to $N_{\text{DPWM}}+M_{\Sigma\Delta}$-bits. The $\Sigma-\Delta$ modulator has two adders, a truncator, and a delay block that forms two feedback loops, as demonstrated in Fig. 2.16(a). The digital filter $(1-\text{NTF}(z))$, which is present in the inner loop, is known as the noise transfer function of the i-th order $\Sigma-\Delta$ modulator. The $N_{\text{DPWM}}+M_{\Sigma\Delta}$-bit digital command, u, is truncated to N_{DPWM} MSBs containing $u_{h,M}$, which are given to the N_{DPWM}-bit counter-based DPWM modulator. On the other hand, $M_{\Sigma\Delta}$ LSBs containing $u_{h,L}$, which represent the quantization noise, are given to a digital filter that ensures the quantization noise approaches zero. The $\Sigma-\Delta$ modulator adjusts $u_{h,M}$, the low-resolution input of the counter-based DPWM, among $2^{N_{\text{DPWM}}}$ possible values to achieve a high-resolution average duty ratio value equal to the $N_{\text{DPWM}}+M_{\text{DPWM}}$-bits input u over several switching cycles. It produces a pattern in $u_{h,M}$, ensuring that the low-frequency average value of $u_{h,M}$ matches the u, while variations in $u_{h,M}$ are shifted to higher frequencies. Consequently, these variations are filtered by the power converter's low-pass action. However, these variations may make jitter noticeable in the signal $c(t)$ [71].

For lower resolutions of $u_{h,L}$, the lowest order harmonic frequency can drop below the cutoff frequency of the output filter, which can amplify low-frequency harmonics and pose challenges for controller design. One way to address this issue is to use second-order $\Sigma-\Delta$ modulators that distribute harmonics across a wider frequency range, pushing low-order harmonics into higher frequencies and leveraging

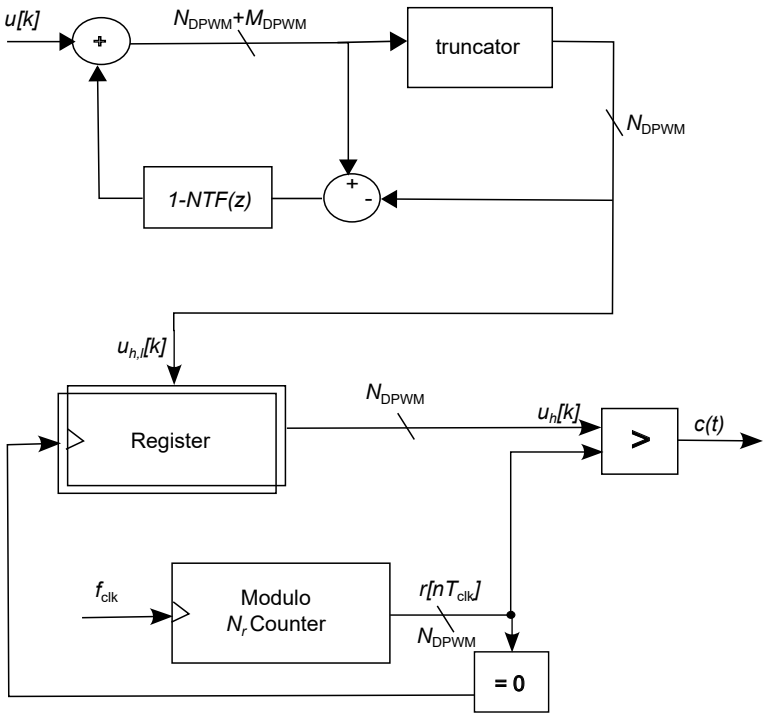

Fig. 2.16 Architecture of ΣΔ DPWM.

noise-shaping principles [82]. However, output filter design can be complicated due to the variable dither frequency and its dependency on the output, which makes predicting the harmonic spectrum difficult. Conversely, satisfactory resolutions of $u_{h,L}$ compared to $u_{h,M}$ can lead to instability issues, further degrading the output signal in specific power stage filters [84].

Dither signals can be introduced into multi-bit $\Sigma - \Delta$ modulators to mitigate idle tone effects. This dither signal is introduced before the quantizer within the modulator loop, and it can be applied to modulators of any order as an alternative to second-order modulators. The method of dithering distributes the power of noise generated by unused frequencies across a broader range of frequencies. This distribution helps to avoid spikes in the output filter's passband or at its corner frequency. This technique has been discussed in [85] and [86]. However, depending on the statistical properties of the dither band, noise quantization may worsen up to four times compared to the undithered case. It is crucial to maintain the lowest order harmonic frequency high enough to allow flexible design of the output filter cutoff frequency and control bandwidth. Although distributing dithers evenly over one period can eliminate the lowest order harmonic, complete elimination under all dither output conditions may not be possible [83].

Multi-Stage Noise Shaping (MASH) modulators are preferred over higher-order modulators because of simplified stability analysis, but they require more system resources and silicon area [87].

2.4.5 Dyadic Digital Pulse Modulation

The dyadic digital pulse modulation (DDPM), introduced in [88], is a digital modulation technique that aims to produce digital bit streams characterized by pulse density proportional to an input binary code. This modulation technique offers favorable spectral attributes, making it suitable for PWM in digitally controlled power converters and for all-digital, cost-effective, energy-efficient, and area-efficient baseband digital-to-analog conversion.

2.4.5.1 DDPM Stream Definition

The DDPM technique that associates to an integer number

$$m = \sum_{i=0}^{M_{\mathrm{DDPM}}-1} b_i 2^i \tag{2.48}$$

with a binary representation on M_{DDPM} bits

$$B_m[M_{\mathrm{DDPM}} - 1 : 0] = (b_{M_{\mathrm{DDPM}}-1}, b_{M_{\mathrm{DDPM}}-2}, \ldots, , b_1, b_0), \tag{2.49}$$

to the periodic digital stream

$$\Sigma_m(t) = \sum_{i=0}^{M_{\mathrm{DDPM}}-1} b_i S_i(t), \quad 0 < t < T_0 \tag{2.50}$$

obtained by superposition of orthogonal dyadic basis functions $S_i(t)$ ($i = 0, \ldots, M_{\mathrm{DDPM}} - 1$) defined on the fundamental period $(0, 2^{M_{\mathrm{DDPM}}} T_{\mathrm{clk}})$ as:

$$S_i(t) = \sum_{i=0}^{M_{\mathrm{DDPM}}-1} \prod \left(\frac{t}{T_{\mathrm{clk}}} - h 2^{M_{\mathrm{DDPM}}-i} - 2^{M_{\mathrm{DDPM}}-i-1} + 1 \right) \tag{2.51}$$

where T_{clk} is the clock cycle and $\Pi(x)$ is the unit pulse ($\Pi(x) = 1$ for $0 \leq x \leq 1$ and $\Pi(x) = 0$ elsewhere).

Each $S_i(t)$ is made up of M_{DDPM} non-overlapping, digital streams that are repeated periodically, and each stream consists of $2^{M_{\mathrm{DDPM}}}$ clock cycles. These streams are arranged in a way that $S_{M_{\mathrm{DDPM}}-1}$ is high every alternate clock cycle, i.e., in $2^{M_{\mathrm{DDPM}}-1}$ cycles per period, $S_{M_{\mathrm{DDPM}}-2}$ is high every other cycle in which $S_{M_{\mathrm{DDPM}}-1}$ is low, i.e., in $2^{M_{\mathrm{DDPM}}-2}$ cycles per period, $S_{M_{\mathrm{DDPM}}-3}$ is high every other cycle in which both $S_{M_{\mathrm{DDPM}}-1}$ and $S_{M_{\mathrm{DDPM}}-2}$ are low, i.e., in $2^{M_{\mathrm{DDPM}}-3}$ cycles per period, and so on, until S_0, which is high only once per period.

The S_i are high for 2^i cycles per period and are non-overlapping. As a result, the DDPM streams m (as defined in eq. (2.50)) are also high for exactly m cycles per period. The time average of these streams is $m/2^{M_{\mathrm{DDPM}}}$, as shown in Fig. 2.17. The figure illustrates the construction of a DDPM stream by the superposition of orthogonal dyadic basis functions for $m = 12$.

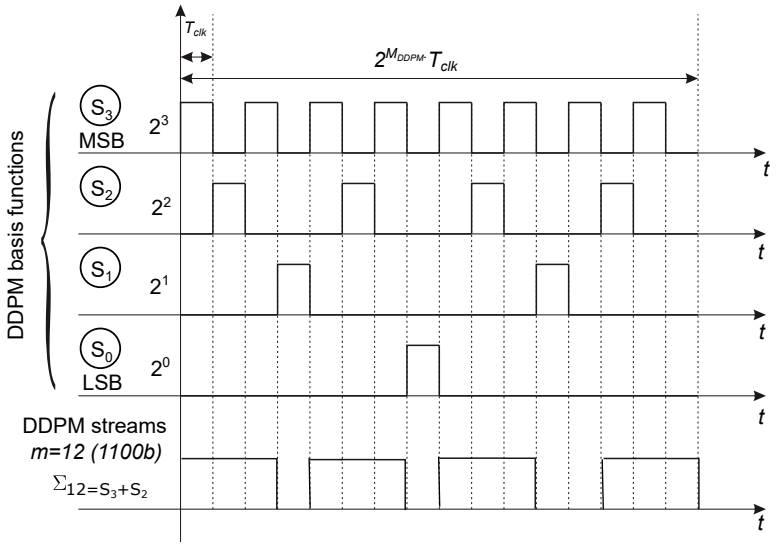

Fig. 2.17 4-bit DDPM basis functions and DDPM pattern for m = 12 (1100b).

The modulation definition of DDPM, which is given in (2.50), can be expressed as $\Sigma_m = [\Theta_{M_{\text{DDPM}}}, 0]$, where, Θ_0 is equal to zero, and Θ_i where $i = 1, \cdots, M_{\text{DDPM}}$, are defined recursively by the following equation:

$$\Theta_i = [\Theta_{i-1}, b_{M_{\text{DDPM}}-i}, \Theta_{i-1}] \tag{2.52}$$

The operator $[\cdot, \cdot]$ is used to concatenate binary strings.

DDPM streams have been used in a variety of practical applications, including power electronics and baseband DAC and ADC conversion. This is because of their high-frequency spectral characteristics, which make it easy to extract their DC component using a low-pass filter with relaxed requirements [80, 88].

2.4.5.2 DDPM Spectral Characteristics

The Fourier transform of eq. (2.50) can be used to obtain the spectral analysis of a DDPM stream. This yields:

$$X_m^{\text{DDPM}}(f) = \sum_{k=-\infty}^{+\infty} a_k c_{k,m} \delta(f - k f_0) \tag{2.53}$$

where, $f_0 = 1/T_0$, and the coefficients are defined as follows:

$$a_k = \frac{1}{2^{M_{\text{DDPM}}}} \text{sinc}\left(\frac{k}{2^{M_{\text{DDPM}}}}\right) \text{e}^{-\frac{jk\pi}{2^{M_{\text{DDPM}}}}} \tag{2.54}$$

$$c_{k,m} = \sum_{i=0}^{M_{\text{DDPM}}-1} b_{i,m} 2^i \sum_{p=0}^{2^{M_{\text{DDPM}}}-i-1} (-1)^p \delta\left[k - 2^i p\right] \tag{2.55}$$

where $\delta[.]$ is the Kronecker function defined as:

$$\delta[n] = \begin{cases} 1, & n = 0 \\ 0, & n \neq 0 \end{cases} \tag{2.56}$$

An expression in closed-form is given by (2.55), but it doesn't reveal much about the spectral properties of DDPM signals. The reason for this is the nested summations in $c_{k,m}$, which make it challenging to observe their relationship with the input code B_m. In [88], a new formula is suggested that presents a unique method of computing the spectra of DDPM streams:

$$c_{k,m} = \begin{cases} m & k = 0 \\ -b_{\nu_2(k)} 2^{\nu_2(k)} + \sum_{i=0}^{\nu_2(k)-1} b_i 2^i & k \neq 0 \end{cases} \tag{2.57}$$

where

$$\nu_2(k) = \max\{\nu \in N : k | 2^\nu\} \tag{2.58}$$

is the *dyadic order* of the integer k, i.e., the largest exponent ν such that 2^ν divides k [89].

The DC component ($k = 0$) of the DDPM stream is exactly the same as the binary input m. Meanwhile, the higher-order spectral coefficients related to the amplitude of the k-th harmonic component of the DDPM spectrum correspond to the value of the binary string $B_m[\nu_2(k) : 0]$.

$$B_m[\nu_2(k) : 0] = (b_{\nu_2(k)}, \ldots, b_0)$$

This binary string comprises the final $\nu_2(k) + 1$ LSBs of the input code m binary representation. The input code m is interpreted as a signed integer in two's complement notation.

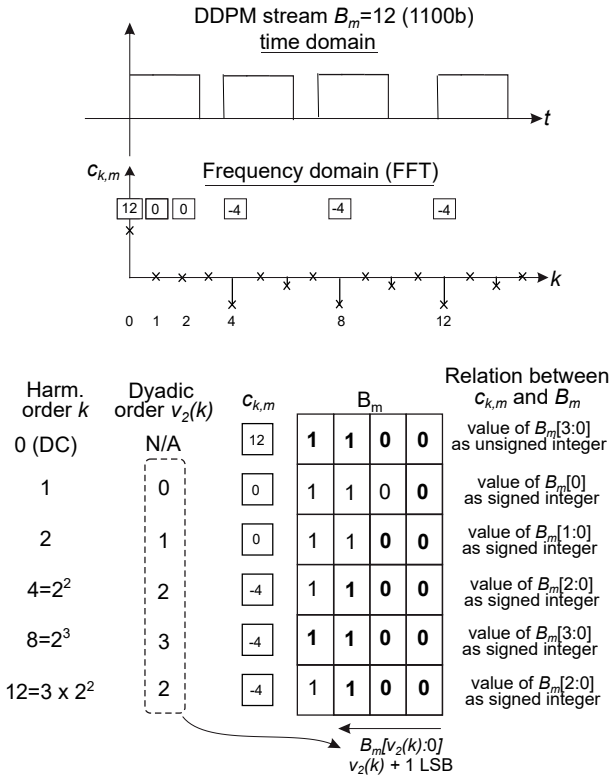

Fig. 2.18 Harmonic spectral coefficients $c_{k,m}$ and the binary representation B_m of $m = 10$ (i.e. $B_m = (1,0,1,0)$).

The spectra of DDPM signals are evaluated as (2.58) for different input codes m, and the maximum value of these spectra is determined as

$$S(kf_0) = \max_m \left| X_m^{\mathrm{DDPM}}(kf_0) \right| \tag{2.59}$$

which corresponds to the envelope. It is presented in Fig.2.19 (top) for $M_{\mathrm{DDPM}} = 16$ bit.

DDPM is a technique used in power electronics that enhances the effective resolution of DPWM modulators in digitally controlled switching mode power converters. It is utilized to suppress limit cycle oscillations resulting from quantization, reduce output voltage ripple degradation, and sustain dynamic performance [80]. The technique leverages the low-frequency characteristics of DDPM streams.

It is possible to easily filter out the high-frequency AC spectral components of DDPM streams while the DC component is directly proportional to the digital input m. The energy contained in the spectral components is linked to $2^{\nu_2(k)}$, and the rate at which it increases with k is 20 dB/Dec, as can be observed in (2.57).

It is possible to maintain all the spurious DDPM spectral components $-6(M_{\mathrm{DDPM}}+1)$ dB below the DC component in a DDPM-based DPWM, using a first-order filter that has a cutoff frequency of $f_c = f_{\mathrm{clk}}/2^N\sqrt{3}$. The effectiveness of this approach is illustrated in Fig. 2.19 (bottom).

2.4.5.3 DDPM Modulator Implementations

DDPM modulators have been efficiently synthesized starting from a hardware description language implemented either on an FPGA [3, 90, 91] or in an application-specific integrated circuit (ASIC) [4, 92, 93].

A. Parallel DDPM Modulator

An article titled [3] discusses a DDPM modulator that uses a digital register with a parallel input and serial output (PISO) configuration. This modulator loads the register bits in parallel with the input code bits, following the DDPM pattern shown in Fig. 2.20, and then streams the bits serially to the output.

This particular design operates at high clock frequencies and does not necessitate combinational logic. However, when the modulator's number of bits M_{DDPM}

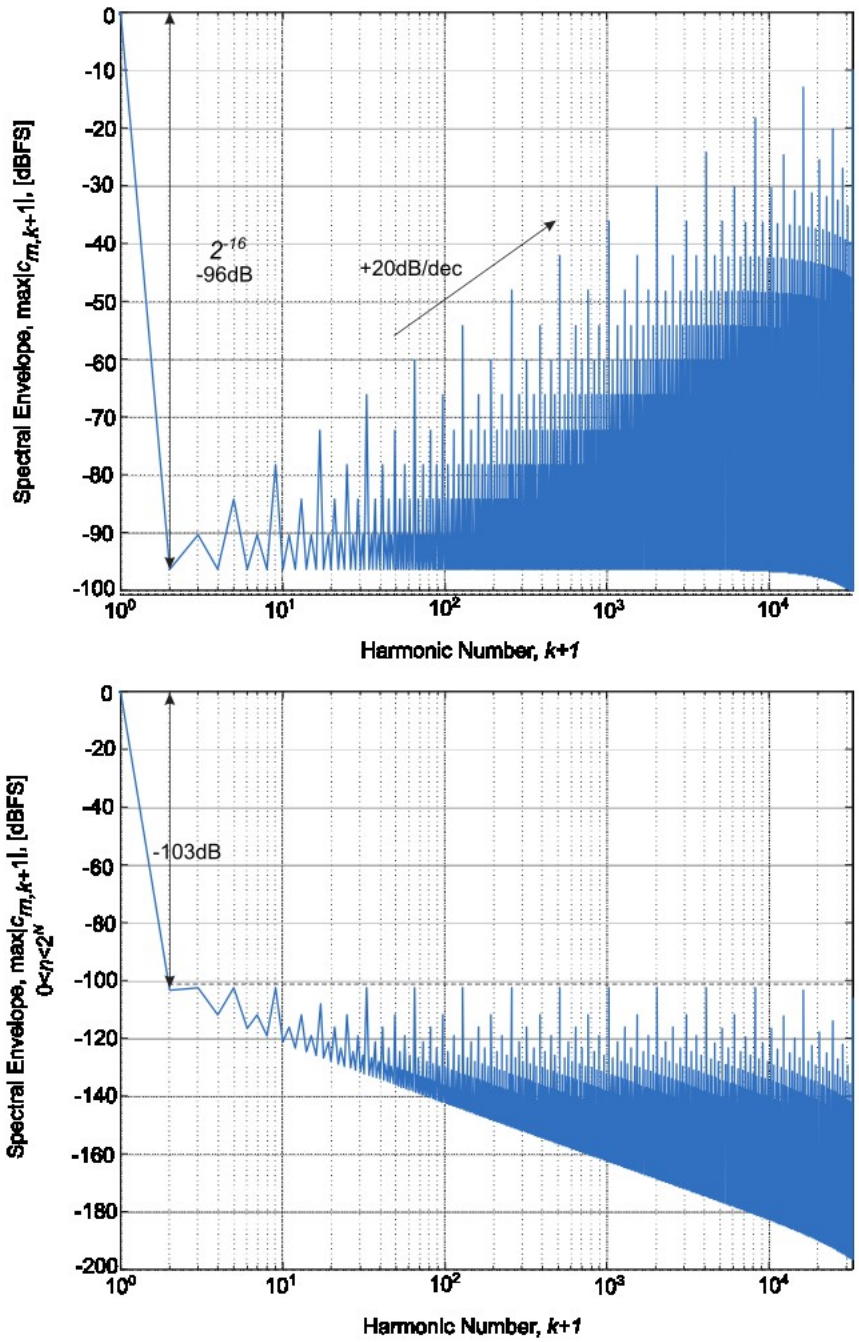

Fig. 2.19 Spectral envelope of M_{DDPM} = 16-bit DDPM streams before (top) and after (bottom) low pass filtering.

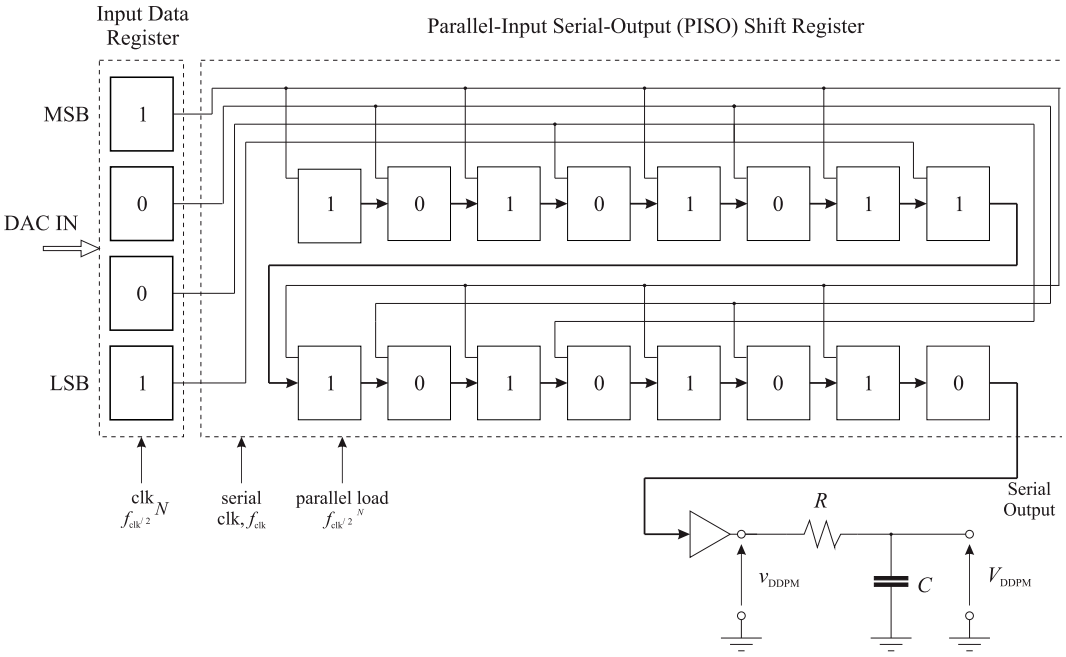

Fig. 2.20 Parallel Hardware implementation of a 4-bit DDPM modulator [3].

increases, the design's complexity (i.e., the number of D flip-flops) increases exponentially. Therefore, the design's area and power efficiency are relatively low for values of M_{DDPM} greater than 4-5. As a result of this limitation, no FPGA and ASIC implementations have utilized the parallel architecture shown in Fig. 2.20.

B. Priority MUX-Based DDPM Modulator

It was previously explained that simple digital hardware can be used to create DDPM streams. To be specific, a binary counter controls a priority multiplexer (Priority MUX), which is shown in Fig. 2.21. The Boolean function that the Priority MUX executes is as follows:

$$O = \sum_{i=0}^{M_{\text{DDPM}}-1} b_{M_{\text{DDPM}}-i-1} \cdot S_i \cdot \prod_{k=0}^{i-1} (\bar{S}_k) \tag{2.60}$$

The priority MUX has selection inputs that are labeled as $S_{M_{\text{DDPM}},\ldots,0}$. These inputs are determined by an M_{DDPM}-bit counter. The selection input is replaced with a new counter value when the counter advances. After this, the input is checked for a "one" bit starting from the LSB. Due to the priority configuration of the multiplexer, the output O takes on the value of $b_{M_{\text{DDPM}}-k}$ from the data input $B_m[M_{\text{DDPM}}-1,\ldots,0]$. If all the selection inputs are zero, the output O will stay at zero.

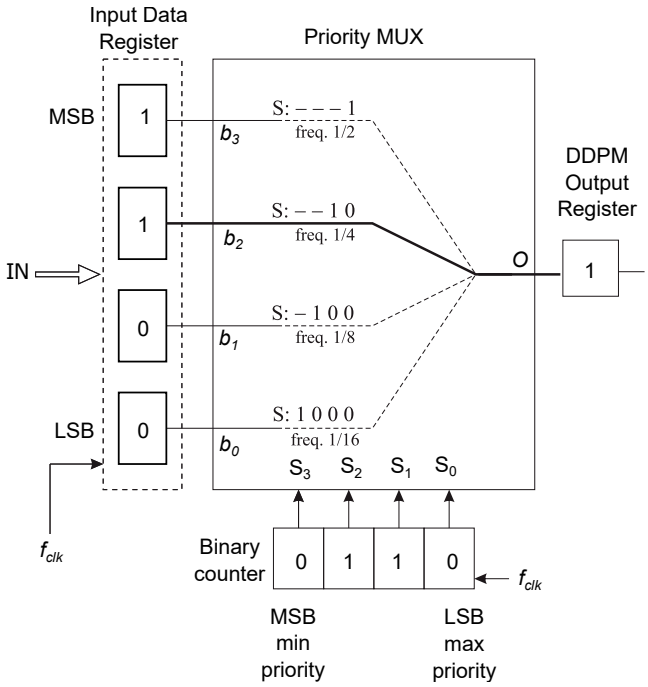

Fig. 2.21 Priority MUX-based Hardware implementation of a 4-bit DDPM modulator.

The graph shown in Fig. 2.22 demonstrates that for a 4-bit M_{DDPM}, the output O changes its value to match b_i exactly 2^i times during the total counting period of $2^{M_{\text{DDPM}}} = 16$ in accordance with the DDPM pattern. The output O takes on the value of $b_{M_{\text{DDPM}}-1} = b_3$ during every other clock cycle (i.e., $2^{M_{\text{DDPM}}-1} = 8$ times) when $S_0 = 1$. In the remaining counting periods, if $S_0 = 0$, the output O matches the logic value of $b_{M_{\text{DDPM}}-2} = b_2$ in half of these cases (i.e., $2^{M_{\text{DDPM}}-2} = 4$ times) because $S_1 = 1$. It can be inferred that the output O changes its value to match b_i precisely 2^i times following the DDPM pattern over a complete counting period.

The excellent balance between complexity and performance is achieved by the hardware architecture of the DDPM modulator, which is based on priority MUX. ASIC and FPGA have widely adopted their implementation [3, 4, 90–93]. In [92], a revised DDPM modulator architecture has been proposed. This new version showcases a customized implementation of the priority MUX, as displayed in Fig. 2.23. It can gracefully degrade performance when clock frequency and supply voltage are scaled.

C. Iterative DDPM Modulator

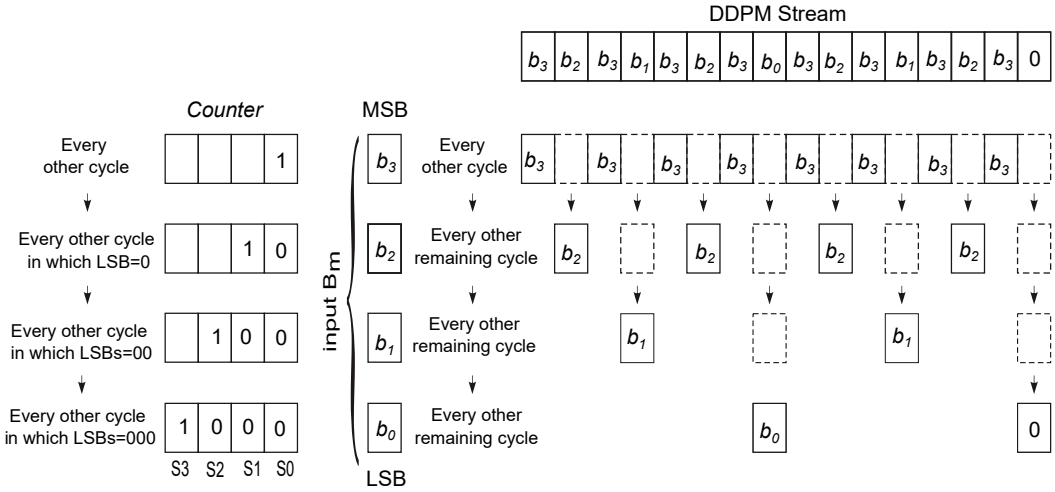

Fig. 2.22 Timing waveform of DDPM streams.

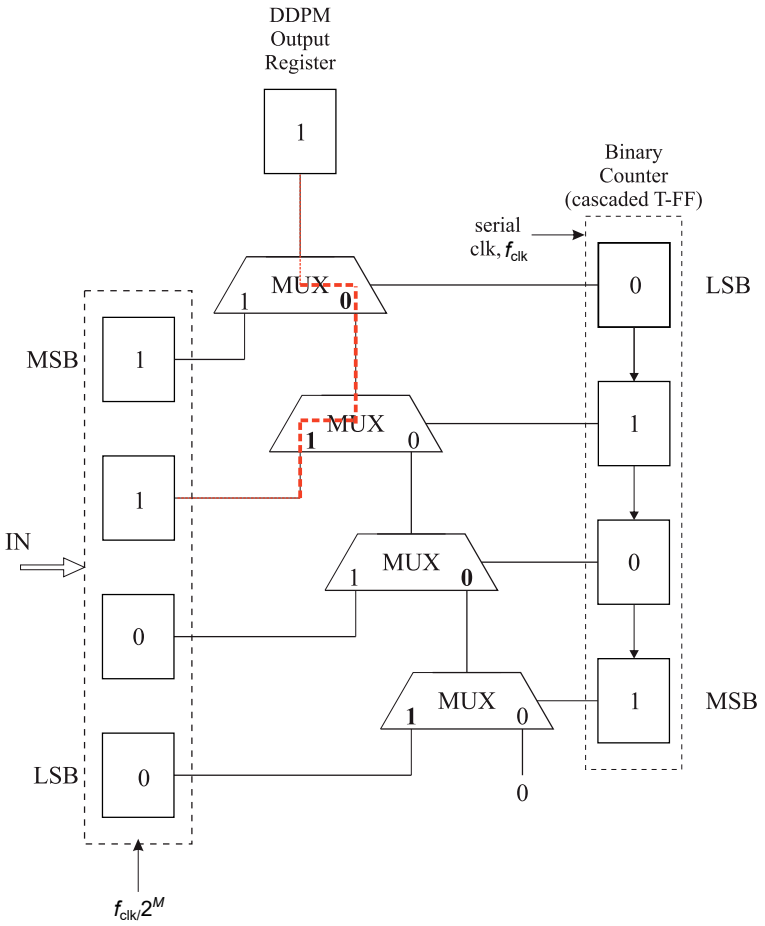

Fig. 2.23 4-bit DDPM modulator implementation featuring graceful performance degradation and dynamic power-resolution scaling [4].

In this architecture, the initial step is to examine the LSB of the binary counter. If $S_0 = 1$, the DDPM output is assigned the value of the MSB of the input data register, i.e., $O = B_{m_{M_{\text{DDPM}}-1}}$, and the procedure is stopped. If $S_1 = 1$, we check the second LSB of the binary counter and the DDPM output is updated with the second MSB of the input data register, i.e., $O = B_{m_{M_{\text{DDPM}}-2}}$, before the iteration ends. This process is repeated for all the remaining bits of the counter until we reach the MSB of the counter. Finally, when $S_{M_{\text{DDPM}}-1} = 1$, the value of B_{m_0} is assigned to the DDPM output, and the iteration is terminated.

In the context of an HW iterative DDPM modulator for $N = 4$, an implementation is shown in Fig. 2.24. The implementation consists of two shift registers which function as "one hot" counters. At the beginning, the registers are initialized with binary values $1,0,0\ldots,0$ and $0,0,\ldots,0,1$. The RSR is a right-shift register, and the LSR is a left-shift register. The LSR output is combined with the binary counter value during each iteration using an AND operation. If the result of the AND operation is true, the DDPM output bit is updated based on the result of the RSR ANDed with the input data register. The iteration is concluded at this point. The iteration persists until the RSR's "hot one" is eliminated from the MSB location and the RSR register's content is reduced to zero.

2.4.5.4 Dyadic Digital Pulse Width Modulation (DDPWM)

The DDPWM technique is utilized to enhance the effective resolution of N_{DPWM}-bit DPWM to $N_{\text{DPWM}} + M_{\text{DDPM}}$ bits, enabling LCO-free operation without compromising switching frequency or DC accuracy in digitally controlled DC-DC converters. Hardware architecture as illustrated in Fig. 2.25 and timing waveform for 8-bit DDPWM (employing 4-bit DPWM and 4-bit DDPM modulator) is shown in Fig. 2.26. A duty cycle u derived from the PID compensator is divided into N_{DPWM} MSBs representing the number $u_{h,M}$, and M_{DDPM} LSBs containing $u_{h,L}$. The DDPM modulator, operated at $f_{\text{clk}}/2^{N_{\text{DPWM}}}$, generates a DDPM signal based on the input to DDPM, i.e., $u_{h,L}$. This DDPM signal, with values of either 0 or 1, is added to $u_{h,M}$, yielding the resulting DDPWM signal fed into a basic N_{DPWM}-bit DPWM modulator running at f_{clk}. This modulator ultimately produces a duty cycle that oscillates between two adjacent quantization levels, $D_1 = \frac{u_{h,M}}{2^{N_{\text{DPWM}}}}$ or $D_2 = \frac{(u_{h,M}+1)}{2^{N_{\text{DPWM}}}}$.

Considering D_1 applied $2^{M_{\text{DDPM}}} - m$ times and D_2 applied $u_{h,M}$ times over a pattern of $2^{M_{\text{DDPM}}}$ switching periods, the average duty cycle throughout $2^{M_{\text{DDPM}}}$ is

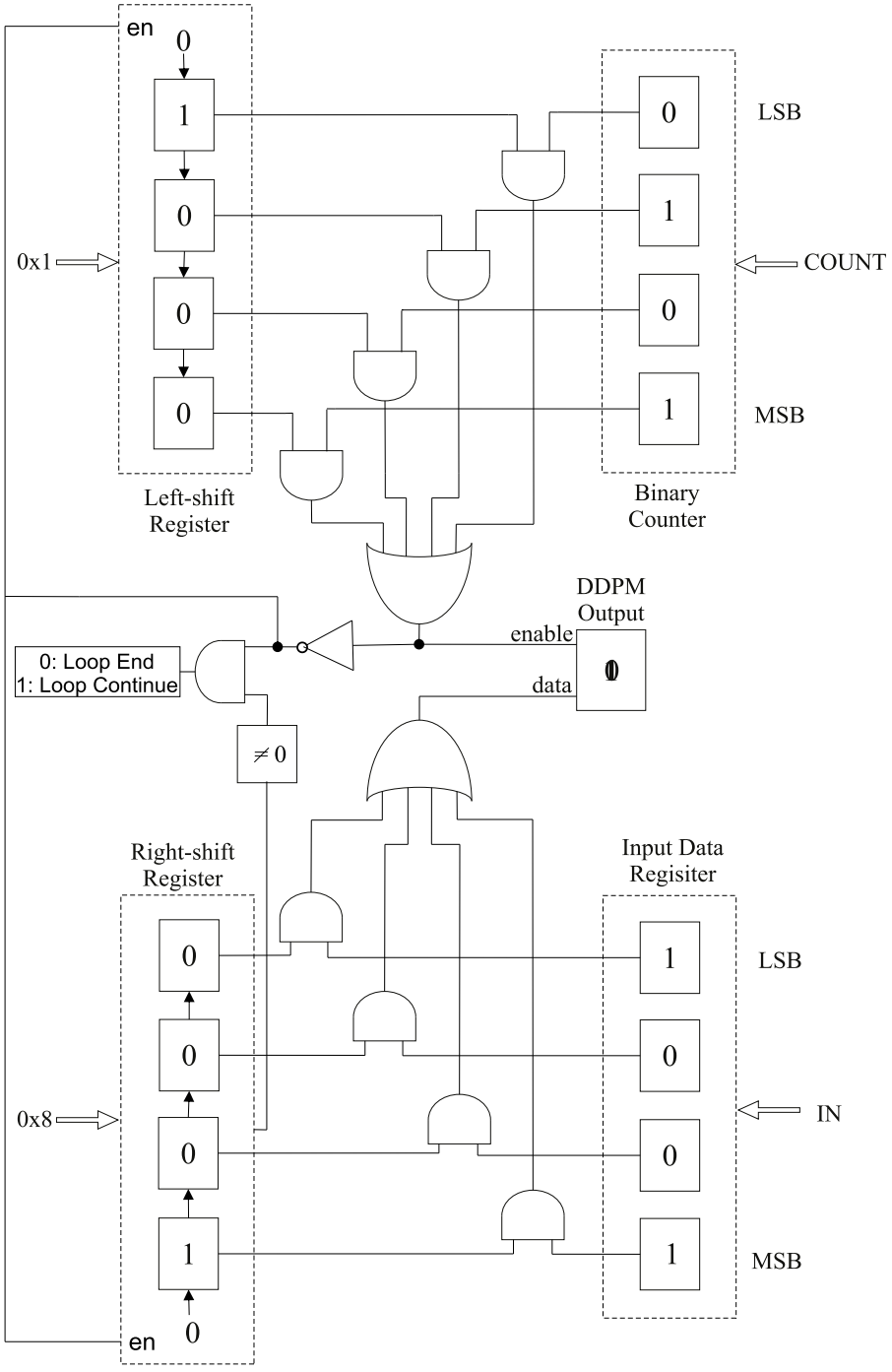

Fig. 2.24 Hardware architecture of a 4-bit iterative DDPM modulator.

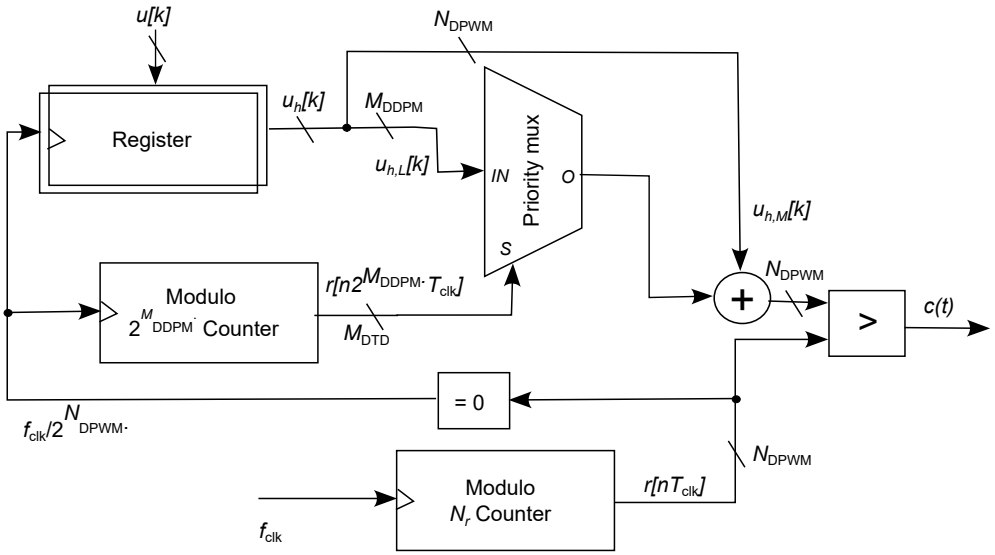

Fig. 2.25 DDPWM Architecture.

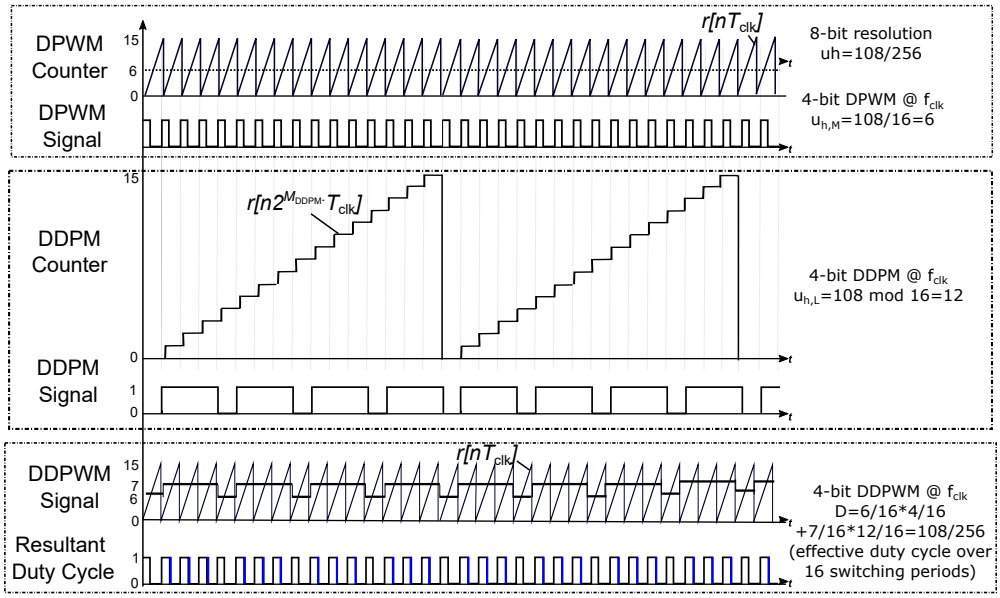

Fig. 2.26 8-bit Dyadic digital pulse width modulation having 4-bit DPWM and 4-bit DDPM.

calculated as:

$$D = \frac{u_{h,M}}{2^{N_{\text{DPWM}}}} \cdot \frac{2^{M_{\text{DDPM}}} - u_{h,L}}{2^{M_{\text{DDPM}}}} + \frac{u_{h,M}+1}{2^{N_{\text{DPWM}}}} \cdot \frac{u_{h,L}}{2^{M_{\text{DDPM}}}} = \frac{u_{h,M} \cdot 2^{M_{\text{DDPM}}} + u_{h,L}}{2^{N_{\text{DPWM}}+M_{\text{DDPM}}}} \quad (2.61)$$

For instance, for 8-bit duty cycle $D = \frac{108}{256}$, splitted in to 4-most significant bits ($N_{\text{DPWM}} = 6$) and 4-least significant bits ($M_{\text{DDPM}} = 12$), the average duty cycle ($D = \frac{7}{16} \cdot \frac{12}{16} + \frac{6}{16} \cdot \frac{4}{16} = \frac{108}{256}$) is achieved over $2^4 = 16$ switching cycles based on DDPM pattern.

Employing DDPWM increases the effective resolution without compromising DC accuracy or clock frequency, thus achieving LCO-free operation. DDPWM's spectral properties allow for improved resolution while minimizing output ripple degradation. This is because the ripple components in DDPWM are moved to higher frequencies which can be more effectively suppressed by the output filter.

2.4.5.5 Spectral Analysis of an $N_{\text{DPWM}} + M_{\text{DDPM}}$ DDPWM Signal

The discussion that follows will provide a detailed examination of the spectral characteristics of DDPWM signals, as presented in [80].

An $N_{\text{DPWM}} + M_{\text{DDPM}}$-bit DDPWM signal $x_{n,m}^{\text{DDPWM}}(t)$ can be represented as:

$$x_{n,m}^{\text{DDPWM}}(t) = x_n^{\text{DPWM}}(t) + x_{m,n}^{\text{DDPM}}(t) \quad (2.62)$$

where,

$$x_{m,n}^{\text{DDPM}}(t) = x_m^{\text{DDPM}}(t) \left[x_{n+1}^{\text{DPWM}}(t) - x_n^{\text{DPWM}}(t) \right] \quad (2.63)$$

where $x_{n+1}^{\text{DPWM}}(t) - x_n^{\text{DPWM}}(t)$ denotes the difference between DPWM waveforms with duty cycles of $(n-1)/2^{N_{\text{DPWM}}}$ and $n/2^{N_{\text{DPWM}}}$, resulting in a stream of one-clock-period pulses at frequency f_{sw}, delayed by $nT_{\text{sw}}/2^{N_{\text{DPWM}}}$ and $x_m^{\text{DDPM}}(t)$ represents a DDPM signal with a unit-time slot T_{sw} and period $2^{M_{\text{DDPM}}} T_{\text{sw}}$. The signal $x_{m,n}^{\text{DDPM}}(t)$ can be described in an alternate way as a DDPM signal that contains a unit-time slot T_{sw}. In this alternate description, the unit pulses $\prod_{T_{\text{sw}}(t)}$ are replaced with time-scaled and delayed pulses $\prod_{\frac{T_{\text{sw}}}{2^{N_{\text{DPWM}}}}} (t - \frac{2}{N_{\text{DPWM}}} T_{\text{sw}})$.

Using eq. (2.53), the spectrum of $x_{n,m}^{\text{DDPWM}}(t)$ can be expressed as:

$$X_{n,m}^{\text{DDPWM}}(f) = X_n^{\text{DPWM}}(f) + X_{m,n}^{\text{DDPM}}(f) \quad (2.64)$$

where the first term $X_n^{\mathrm{DPWM}}(f)$ is the spectrum of an $N_{\mathrm{DPWM}}-$bit DPWM signal at frequency f_{sw} with a constant duty cycle $n/2^{N_{\mathrm{DPWM}}}$, given by:

$$X_n^{\mathrm{DPWM}}(f) = \frac{n}{2^{N_{\mathrm{DPWM}}}} \sum_{k=-\infty}^{+\infty} \mathrm{sinc}\left(\frac{kn}{2^{N_{\mathrm{DPWM}}}}\right) \mathrm{e}^{-\frac{j\pi kn}{2^{N_{\mathrm{DPWM}}}}} \delta\left(f - kf_{\mathrm{s}}\right) \tag{2.65}$$

The second term in eq. (2.64), i.e., $X_{m,n}^{\mathrm{DDPM}}(f)$ is described as:

$$X_{n,m}^{\mathrm{DDPM}}(f) = \sum_{k=-\infty}^{+\infty} b_{k,n} c_{k,m} \delta\left(f - k\frac{f_{\mathrm{s}}}{2^{M_{\mathrm{DDPM}}}}\right) \tag{2.66}$$

where, $c_{k,m}$ are the coefficients of the DDPM sequence spectrum explained above, and

$$b_{k,n} = \frac{1}{2^{N_{\mathrm{DPWM}}+M_{\mathrm{DDPM}}}} \mathrm{sinc}\left(\frac{k}{2^{N_{\mathrm{DPWM}}+M_{\mathrm{DDPM}}}}\right) \mathrm{e}^{-\frac{j\pi k\left(2^{N_{\mathrm{DPWM}}}+n\right)}{2^{N_{\mathrm{DPWM}}+M_{\mathrm{DDPM}}}}} \tag{2.67}$$

describes period-by-period duty cycle variations closely related to the spectrum of a DDPM signal.

In contrast to traditional dithering methods like DTD, DDPWM achieves enhanced resolution while minimizing output ripple and dynamic performance degradation.

2.4.5.6 Comparison of Spectral Characteristics of DTDPWM and DDPWM Signal

According to the previous analysis, the DC component of eq. (2.66) for $X_{m,n}^{DDPM}(f)$ (and eq. (2.45) for $X_{m,n}^{\mathrm{DTD}}(f)$) adjusts the DC value of $X_n^{DDPM}(f)$ (and $X_n^{DTD}(f)$) to enhance the resolution of $N_{\mathrm{DPWM}} + M_{\mathrm{DDPM}}$-bits (and $N_{\mathrm{DPWM}} + M_{\mathrm{DTD}}$-bits). Additionally, the other spectral components simultaneously generate tones at subharmonics $k/2^{M_{\mathrm{DDPM}}}$ (and $k/2^{M_{\mathrm{DTD}}}$) with k ranging from 0 to $2^{M_{\mathrm{DDPM}}-1}$ (and 0 to $2^{M_{\mathrm{DTD}}-1}$) of the switching frequency. As the resolution enhancement M_{DDPM} (and M_{DTD}) increases, the fundamental frequency $f_{\mathrm{sw}}/2^{M_{\mathrm{DDPM}}}$ (and $f_{\mathrm{sw}}/2^{M_{\mathrm{DTD}}}$) exponentially decreases towards the passband of the output filter. As a result, output voltage ripple occurs [80].

In thermometric dithering, the amplitude of subharmonic tones reduces steadily with an increase in k, as determined by $d_{k,m}$ in eq. (2.47). This amplitude is at its highest at lower-order harmonics. In contrast, in DDPWM, the amplitude of these tones increases with k as per $c_{k,m}$ in eq. (2.55). DDPWM results in the spectral energy of the baseband sub-switching frequency being distributed more effectively towards higher frequencies. This is because the output filter has a greater attenuation at higher frequencies. The energy produced by DDPWM is very low at the lowest frequency of harmonic components. These components are closer to the passband of the LC filter and have a significant impact on the output voltage ripple. DDPWM has the ability to enhance output accuracy, but only if the lowest frequency spurious component at frequency $f_{\mathrm{sw}}/2^{M_{\mathrm{DDPM}}}$ exceeds the cutoff frequency f_c of the output filter. This means that DDPWM can be utilized to improve output resolution in bits up to a certain limit [80].

$$M_{\max} = \left\lfloor \log_2 \left(\frac{f_{\mathrm{sw}}}{f_{\mathrm{c}}} \right) \right\rfloor \tag{2.68}$$

where $\lfloor . \rfloor$ denotes the floor rounding operator [80].

Feature	**Delay Line DPWM**	**Sigma-Delta DPWM**	**Thermometric Dithering DPWM**	**Dyadic DPWM**
Resolution	High	Very high	High	High
Complexity	High	Moderate to high	Low	Low
Power Consumption	High	Moderate	High	High
Quantization Noise	Minimal	Low	Minimal	Minimal
Latency	Very low	Moderate	High	High
Ease of Design and Implementation	Challenging	Moderate	Easy	Easy
Area Consumption	High	Moderate	High	High
Scalability	Moderate	Good	Moderate	Moderate

Table 2.1 Comparison of Different DPWM Techniques

2.5 Conclusion

In conclusion, this chapter sheds light on the critical issues causing limit cycle oscillations in digitally controlled power converters. By delving into the intricate dynamics between ADCs and DPWM quantizations, strategies have been discussed to address and prevent the onset of LCOs. Implementing LCO-free operating conditions and state-of-the-art DPWM techniques offers a pathway toward improved regulation accuracy and performance in digitally controlled power converters.

Chapter 3

Limit-Cycle Free, Digitally-Controlled Boost Converter based on DDPWM

3.1 Motivation

As discussed in the introductory chapter, digital controllers, despite their numerous benefits, face challenges such as the onset of LCOs caused by quantization effects in ADC and DPWM [94, 95]. Addressing this issue is crucial as LCOs can disrupt voltage regulation, increase power losses, and increase output ripple.

LCOs can be prevented by adhering to the guidelines outlined in Chapter 2. While meeting conditions (2.34) and (2.35) with suitable PID coefficients is relatively straightforward, condition (2.28) concerning the resolution of the ADC and DPWM presents a more challenging requirement. Enhancing the DPWM resolution to satisfy (2.28) may elevate costs and complexity, particularly for converters operating at high switching frequencies utilizing advanced semiconductor technologies such as GaN and SiC power transistors [96]. Conversely, reducing ADC resolution to mitigate LCOs can compromise DC accuracy.

To tackle this issue, the DDPWM introduced in Chapter 2 offers a cost-effective solution with minimal design complexity and minimal output ripple degradation [97, 98]. The effectiveness of DDPWM in enhancing DPWM resolution for LCO-

free operation in a DC-DC Buck converter has been demonstrated in [99, 100] through experimental validation conducted by implementing DDPWM on an FPGA.

A Buck converter undergoes a continuous change in output voltage quantization steps as the duty cycle varies, whereas a Boost converter undergoes a non-linear change in output voltage quantization steps with respect to the duty cycle [101]. As a result, ensuring that the DPWM resolution requirements (2.28) meet over a wide range of duty cycles in the Boost converter is a significant challenge.

In a novel approach to mitigate LCOs, DDPWM is implemented in a voltage-mode, digitally controlled Boost converter for the first time [102], substantiating its effectiveness through experimental results, which will be elaborated on in this chapter.

3.2 Minimum DDPWM resolution required to avoid LCOs in Boost converter

In this section, we will compare the ADC resolution and the minimum required DPWM resolution to meet the condition (2.28) for the Buck and Boost converters.

The quantization of the output voltage in the Buck converter can be described as a result of the DPWM resolution in eq. (2.16):

$$q_{v_o}^{(\mathrm{DPWM})} = q_{\mathrm{D}}^{(\mathrm{DPWM})} \cdot V_{\mathrm{IN}} \tag{3.1}$$

since the $\mathrm{M}(D) = D$ [101].

The Buck converter has an output voltage that changes proportionally to the change in the duty cycle. For this converter, the value of $q_{v_o}^{(\mathrm{DPWM})}$ is independent of D. By replacing (2.13) and (2.10) in (3.1), we arrive at the LCO-free operating condition (2.28). This equation can be expressed as:

$$2^{N_{\mathrm{DPWM}}} > \frac{2^{N_{\mathrm{ADC}}} \cdot V_{\mathrm{in}} \cdot H}{V_{\mathrm{FS}}}, \tag{3.2}$$

By taking the logarithm in base 2 of the above equation, we get:

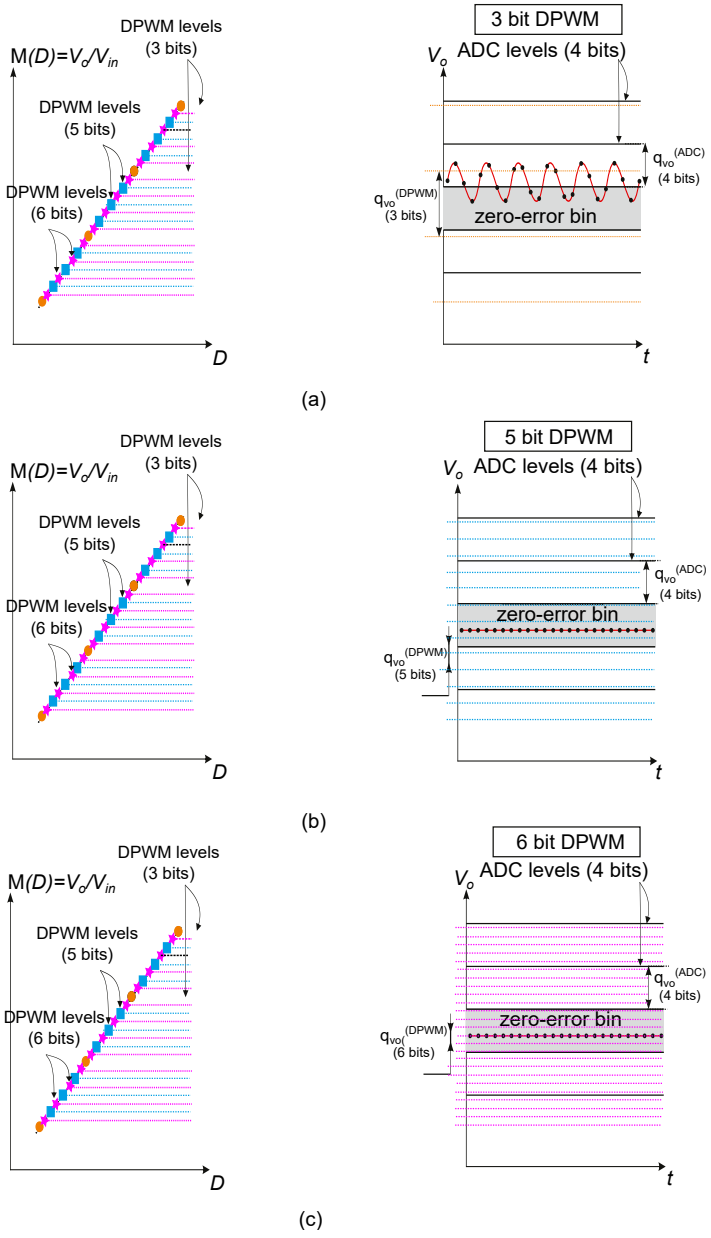

Fig. 3.1 Quantization of Output Voltage in Buck Converter Induced by DPWM with $N_{\mathrm{DPWM}} = 3$, $N_{\mathrm{DPWM}} = 5$ and $N_{\mathrm{DPWM}} = 6$ having $N_{\mathrm{ADC}} = 4$

$$N_{\text{DPWM}} > N_{\text{ADC}} + A, \tag{3.3}$$

where A is a constant that depends on the design parameters and specifications and can be calculated as:

$$A = \left\lceil \log_2 \frac{V_{\text{IN}} \cdot H}{V_{\text{FS}}} \right\rceil. \tag{3.4}$$

We can observe an instance of a buck converter with output voltage quantization induced by $N_{\text{DPWM}} = 3$-bit DPWM in Fig. 3.1(a). The quantized output voltage is represented by circle markers, and the output voltage ranges that stem from $N_{\text{ADC}} = 4$-bit ADC quantization can also be seen in the figure. In this scenario, none of the DPWM output voltage quantization levels are aligned with the ADC zero-error bin, resulting in a limit cycle.

In Fig. 3.1(b) and Fig. 3.1(c), the resolution of DPWM has been increased to 5-bits (denoted by square markers) and 6-bits (depicted with star markers), respectively. This increase in resolution fulfills the criteria for LCO-free operation (2.28). One of the DPWM quantization levels falls within the ADC zero-error bin, enabling the controller to stabilize the output voltage. By satisfying conditions (2.34) and (2.35), limit cycles can be avoided.

By contrast, in the Boost converter in Fig. 2.2(a), $\mathrm{M}(D) = 1/(1-D)$ [101], so (2.16) becomes:

$$q_{v_{\text{o}}}^{(\text{DPWM})} = \frac{1}{(1-D)^2} \cdot q_{\text{D}}^{(\text{DPWM})} \cdot V_{\text{in}} \tag{3.5}$$

It is suggested that the output voltage quantization of $q_{v_{\text{o}}}^{(\text{DPWM})}$ is dependent on D. The quantization steps become finer for lower duty-cycle values, while the step size increases as the duty cycle goes up. Due to the non-linear quantization of the output voltage, satisfying the LCO-free operation condition (2.28) is more critical for the Boost converter than the Buck converter.

Similar to the calculations performed for the Buck converter, it is possible to determine the minimum DPWM resolution required for the Boost converter. The result obtained is:

$$N_{\text{DPWM}} > N_{\text{ADC}} + B \tag{3.6}$$

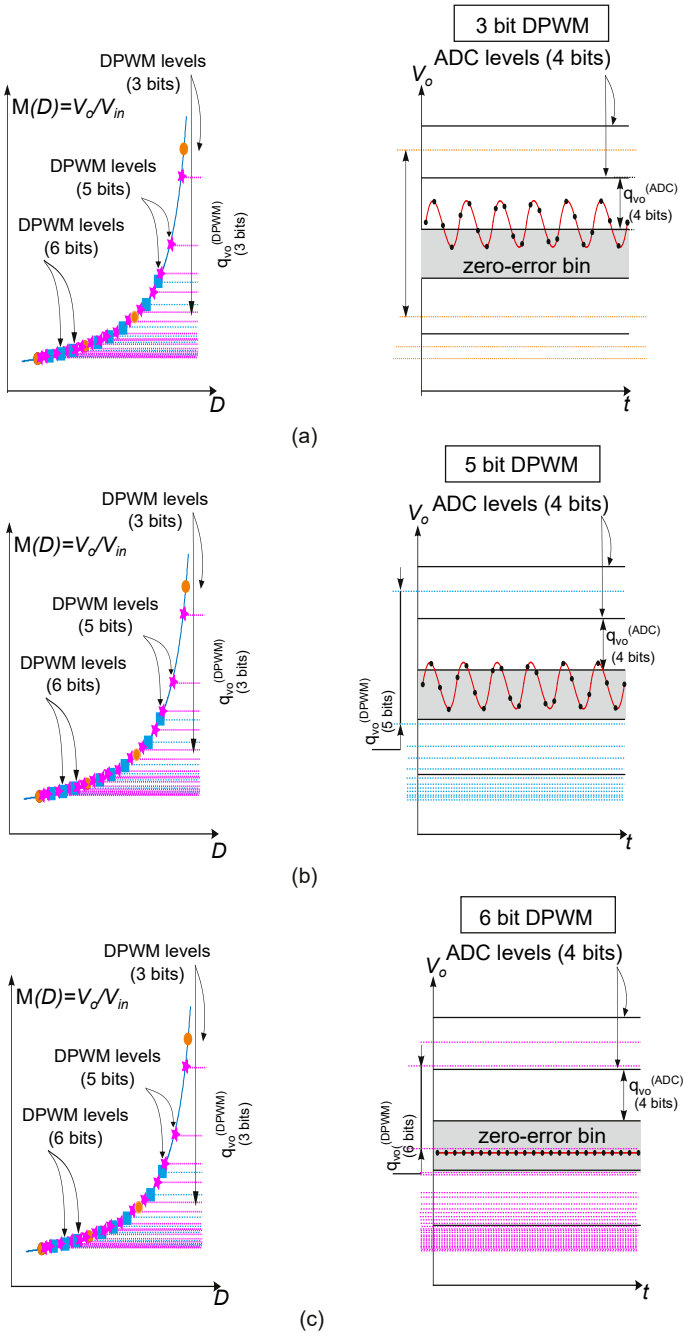

Fig. 3.2 Quantization of Output Voltage in Boost Converter Induced by DPWM with $N_{\mathrm{DPWM}} = 3$, $N_{\mathrm{DPWM}} = 5$ and $N_{\mathrm{DPWM}} = 6$ having $N_{\mathrm{ADC}} = 4$

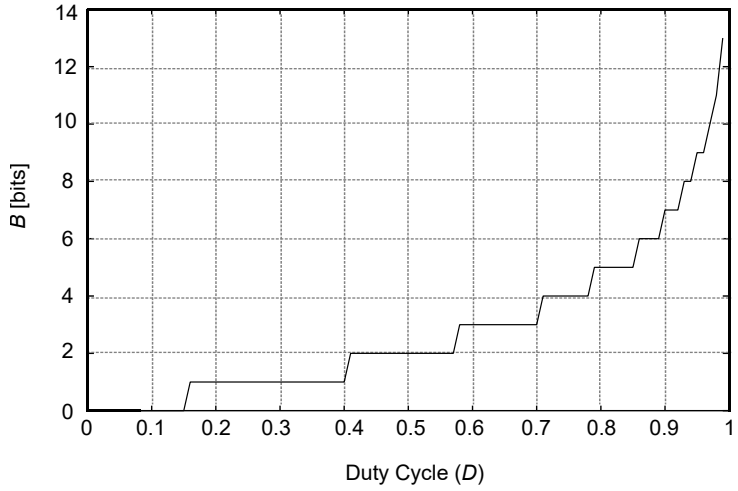

Fig. 3.3 Smallest amount by which N_{DPWM} must be increased compared to N_{ADC} in order to meet the LCO-free operation requirement stated in equation (2.28) for a Boost converter

where,

$$B = \left\lceil \log_2 \frac{V_{\text{IN}} \cdot H}{V_{\text{FS}}} + \log_2 \frac{1}{(1-D)^2} \right\rceil$$

is depending on the duty cycle. Fig. 3.3 presents the graph of B across the entire range of duty cycle values. The plot in Fig. 3.2(a) shows a Boost converter with a $N_{\text{DPWM}} = 3$-bit DPWM quantization range (represented by circles) and $N_{\text{ADC}} = 4$-bit ADC quantization segments in relation to the output voltage. It can be observed that none of the DPWM quantization levels fall within the ADC zero-error bin, which results in limit cycles. Fig. 3.2(b) displays the same circuit with an increased DPWM resolution of $N_{\text{DPWM}} = 5$-bits (indicated by square markers); however, once again, there is no DPWM quantization interval that lies in the zero-error bin.

It's important to consider the duty cycle's operating value or range when dealing with Boost converters, as simply having the DPWM resolution higher than the ADC resolution is not a straightforward process. Figuring out the minimum DPWM resolution needed relative to the ADC resolution for various duty cycle values to achieve LCO-free operation for both Buck and Boost converters can be seen in Fig. 3.4.

The information presented in Fig. 3.2(c) shows the increase in DPWM resolution to $N_{\text{DPWM}} = 6$-bits (represented by star markers), which satisfies the LCO-free operation criteria (2.28) as per eq. (3.6). Due to the increase, the DPWM quantization level is now in the ADC zero-error bin, which helps avoid limit cycles.

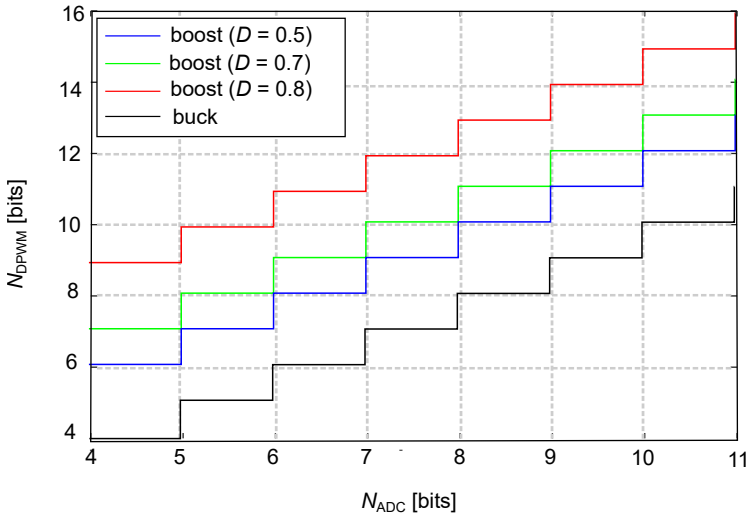

Fig. 3.4 Minimum N_{DPWM} versus N_{ADC} for various duty cycle values for Buck and Boost converter

Implementing DDPWM along with the PID compensator is possible by following the eq. (3.6). The implementation of the PID compensator with DDPWM is shown in Fig. 3.5. The PID compensator calculates the duty-cycle $u[k]$, and then it is split into N_{DPWM} MSBs and M_{DDPM} LSBs. These MSBs are sent to the input of a counter-based DPWM modulator that operates at f_{clk}. On the other hand, the remaining M_{DDPM} LSBs are given as input to the priority multiplexer (Mux) of the DDPM modulator. The sampling of the duty-cycle $u[k]$ is done at $f_{\text{clk}}/2^{N_{\text{DPWM}}}$.

3.3 Experimental Validation

The Boost converter has been tested and verified using the DDPWM method discussed earlier through simulations and measurements. It includes a digital controller with a digital compensator, an ADC, the DDPWM, and a power stage, as shown in Fig. 2.2(a). The converter is specifically designed to operate in CCM mode and can handle input voltages ranging from 7 to 10 V. Its output voltage is regulated at a constant value of 13.8 V, with a switching frequency of 1.17 MHz, and is controlled by a voltage-mode digital control algorithm. All the necessary specifications, values, and parasitics of the components used have been reported in Table 3.1.

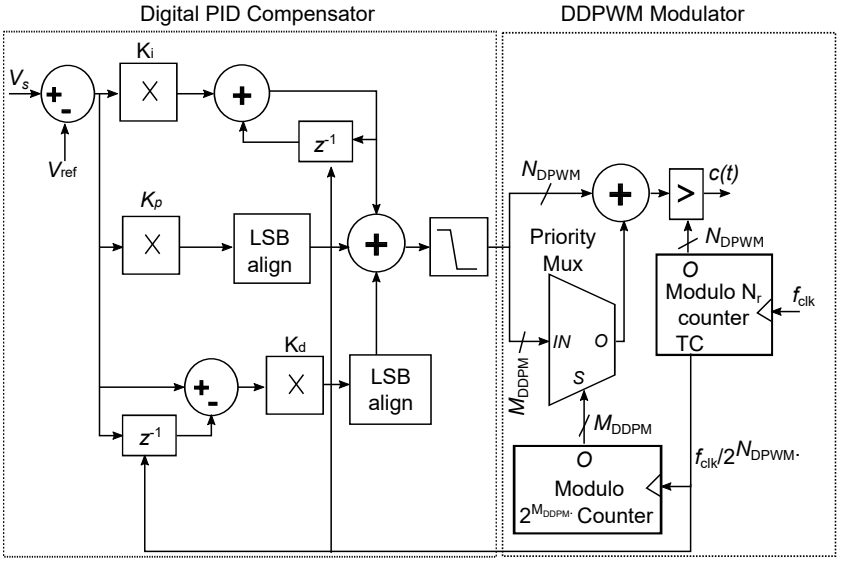

Fig. 3.5 Block diagram of digital PID compensator and DDPWM

Using the eq.(2.4), the power stage z-domain transfer function can be computed as:

$$G_{vu}(z) = \frac{04206z - 0.01327}{z^2 - 1.96z + 0.9882}. \tag{3.7}$$

The gains for the PID compensator have been calculated using the method outlined in Appendix A. The goal was to achieve a crossover frequency of $f_c = 100$ kHz and a phase margin of $\phi_m = 45^o$. The values obtained are tabulated in Table 3.1, with reference to eq. (2.8).

Simulink/Modelsim co-simulation [103] and experimental tests were carried out on a hardware prototype to evaluate the effectiveness of the DDPWM in suppressing LCOs, enhancing DC accuracy, and reducing output voltage ripple.

3.3.1 Co-simulation test setup

The Matlab/Simulink software was used to simulate a synchronous DC-DC Boost converter, as depicted in Fig. 3.6 and with the values of components as described in Table 4.1. The Verilog description of the digital PID compensator and DDPWM have been implemented in Modelsim. A Simulink-ADC block was used to quantize the output voltage into a digital value, which has been further processed by the Modelsim Simulator block. The processing involved performing error signal computation, PID

Table 3.1 System Design Specifications

Parameters	Name	Values	Unit
Input Voltage	V_{in}	7 - 10	V
Input Capacitor	C_{in}	1	μF
Capacitor Equivalent Series Resistance	r_{C}	10	mΩ
Inductor	L	900	nH
Inductor series Resistance	r_{L}	8	mΩ
FET ON Resistance	R_{on}	24	mΩ
Output Capacitor	C_{o}	3	μF
Capacitor Equivalent Series Resistance	$r_{\text{C}_{\text{o}}}$	3.3	mΩ
Load Resistor	R_{L}	25-30	Ω
Voltage Divider Gain	H_0	1 / 9.2	-
ADC Input Range	V_{FS}	3	V
Clock Frequency	f_{clk}	18.75, 37.5, 75, 150	MHz
Switching Frequency	f_{sw}	1.17	MHz
Proportional Gain	K_{p}	20	-
Derivational Gain	K_{d}	79	-
Integral Gain	K_{i}	0.009	-
ADC resolution	N_{ADC}	4 - 11	bits
DPWM resolution	N_{DPWM}	4 - 7	bits
DDPM resolution	M_{DDPM}	4	bits
DTD resolution	M_{DTD}	4	bits

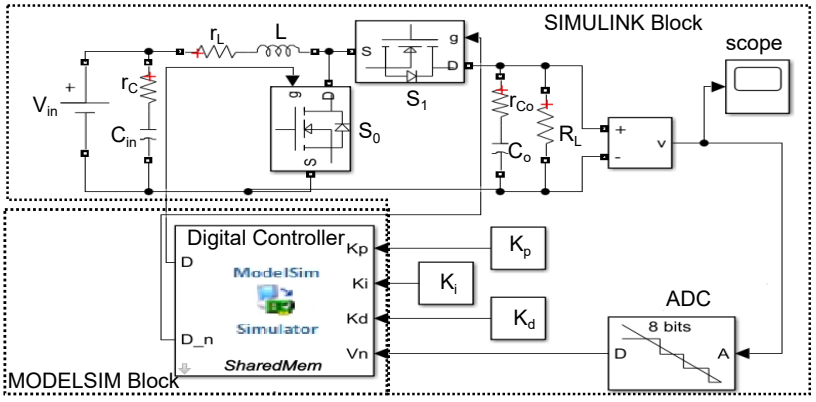

Fig. 3.6 Digitally controlled Boost converter simulation test setup

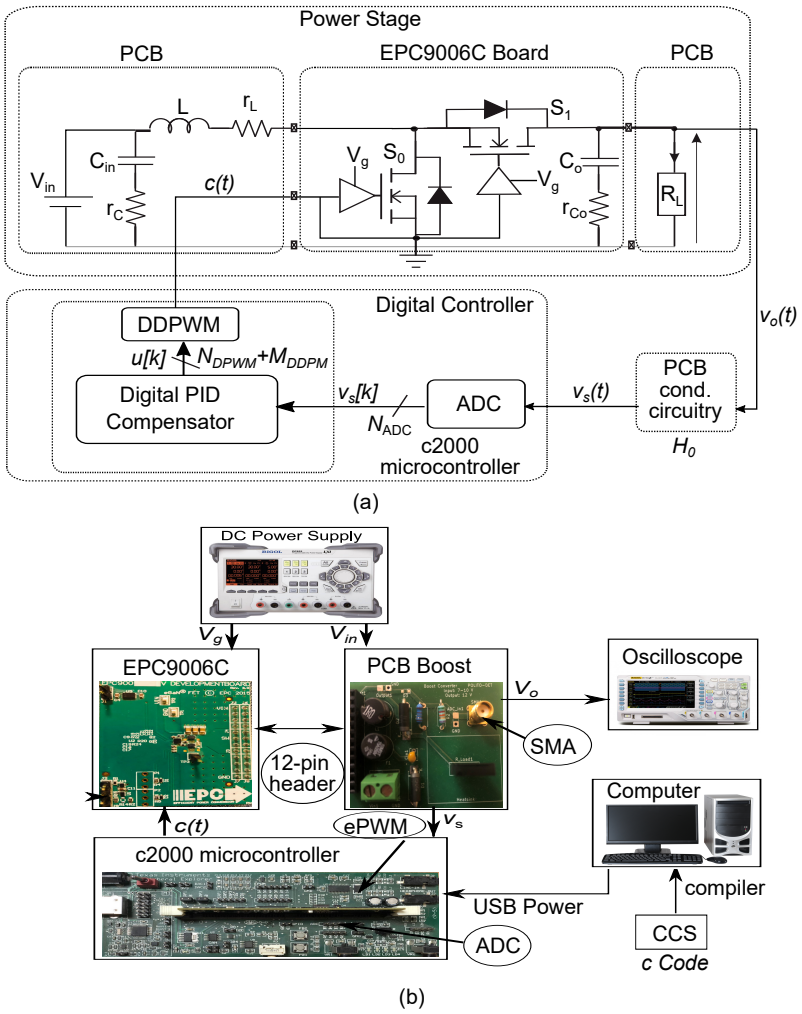

Fig. 3.7 Digitally controlled boost converter (a) Experimental test setup schematic (b) experimental testbench

calculations, and DDPWM evaluation. Finally, the Modelsim block produced a square-wave PWM signal that was used to control the switching of the MOSFETs.

The Simulink environment can simulate the Modelsim block using the co-simulation wizard tool available in MATLAB [103].

The output voltage's behavior has been monitored using a scope with a load resistor attached. Various ADC and DPWM resolutions have been used, and different input voltages have been supplied to the converter to obtain these results. The subsequent section will compare and analyze these findings with experimental results.

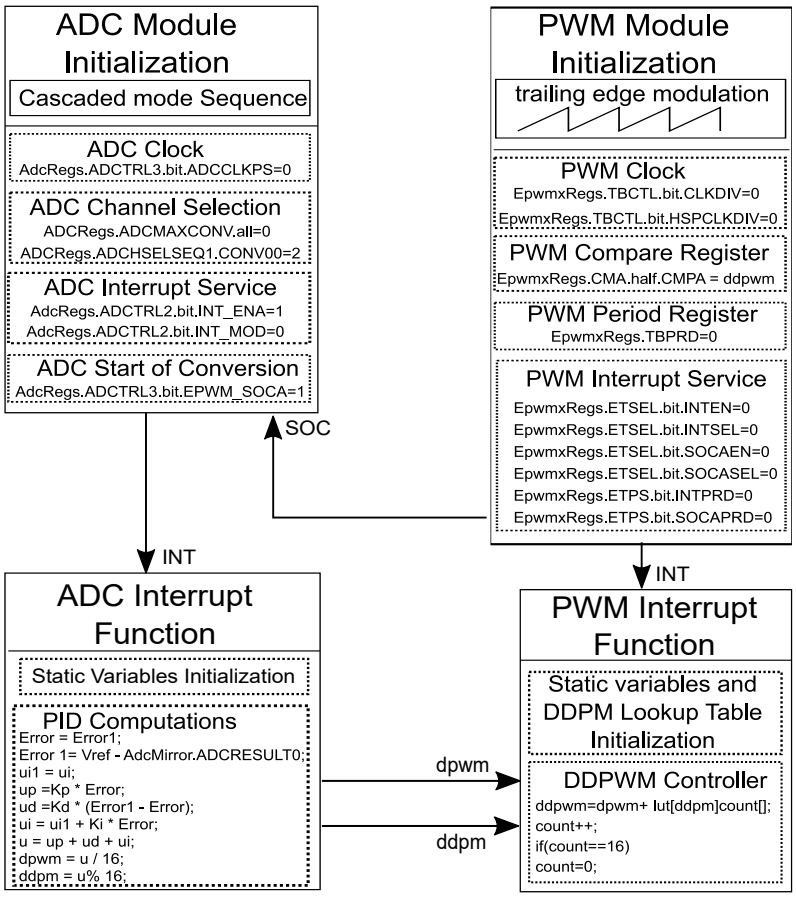

Fig. 3.8 Architecture of C code .

3.3.2 Experimental Test Setup

The experimental test setup diagram is illustrated in Fig. 3.7(a). This setup includes the development board, named EPC9006C, which comes with onboard gate drivers and a half-bridge configuration. The board uses eGaN FETs that are designed for high-switching frequency applications. The primary goal of this development board is to operate at high frequencies and simplify the EPC2007C eGaN FET assessment process. It is a single board that includes all the essential components, making it easy to connect to external components and create different switching converter topologies. A printed circuit board (PCB) has been designed to assign the inductor L and load resistor R_{L} and achieve the Boost in Fig.2.2(a). This PCB is used along with the EPC9600C board which can be connected through a 12-pin female header.

A prototyping board based on a c2000 microcontroller has been utilized to store the digital control algorithm, performing tasks such as digital PID compensation and DDPWM. The TMS320F2833F processor with a clock speed of 150 MHz, an onboard 8-channel 12-bit ADC module, and an enhanced PWM (ePWM) module are all available on the board [104]. The ePWM output pin has been connected to the EPC9006C PWM input pin, while an SMA cable has been used to ensure the connection between the Boost and the ADC module. The experimental test setup consists of a DC power supply and a digital storage oscilloscope, as shown in Fig. 3.7(b).

The architecture of the digital control system used in this project is illustrated in Figure 3.8. To set up the system, the microcontroller, ADC, and ePWM module must be connected. At the outset, the ePWM module is configured to achieve a specific DPWM resolution, N_{DPWM}, and a fixed switching frequency f_{sw}. The DPWM counter operates at a clock frequency of $f_{\mathrm{clk}} = f_{\mathrm{sw}} \times 2^{N_{\mathrm{DPWM}}}$. Once the counter value reaches its maximum count, an interrupt is triggered to start an ADC conversion. The ADC samples data based on defined parameters such as ADC channels and frequencies. The controller must complete the control algorithm calculations within the sampling period to ensure proper functionality at the desired frequency.

A clock frequency of 150 MHz, a switching frequency of 1.17 MHz, and a controller processing time of 172 clock cycles per operation are used. The sampling frequency is set to half the switching frequency (i.e., $f_s = f_{sw}/2$). The PID compensator processes the error signal to calculate a new duty-cycle value at each

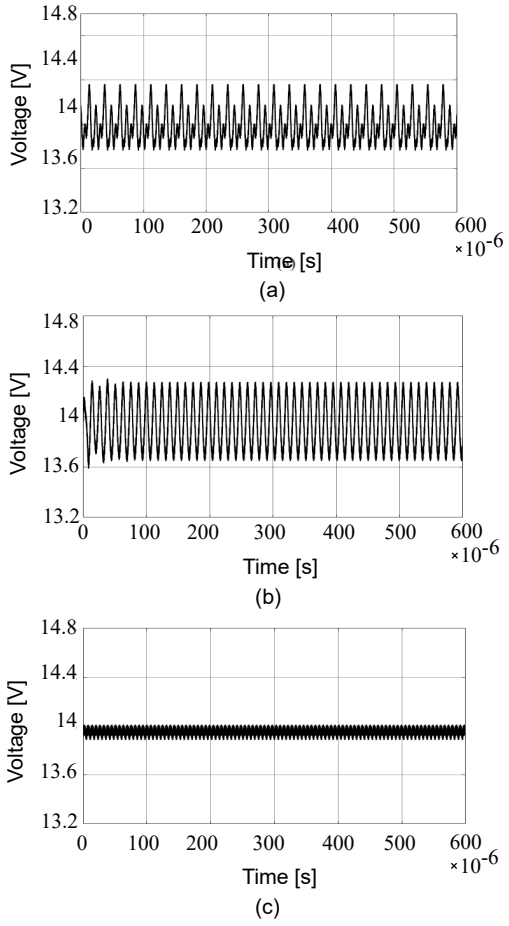

Fig. 3.9 Simulated output voltage of the Boost converter. (a) $N_{\mathrm{ADC}} = 7$, $N_{\mathrm{DPWM}} = 5$; (b)$N_{\mathrm{ADC}} = 7$, $N_{\mathrm{DPWM}} = 5$, $M_{\mathrm{DTD}} = 4$; (c) $N_{\mathrm{ADC}} = 7$, $N_{\mathrm{DPWM}} = 5$, $M_{\mathrm{DDPM}} = 4$

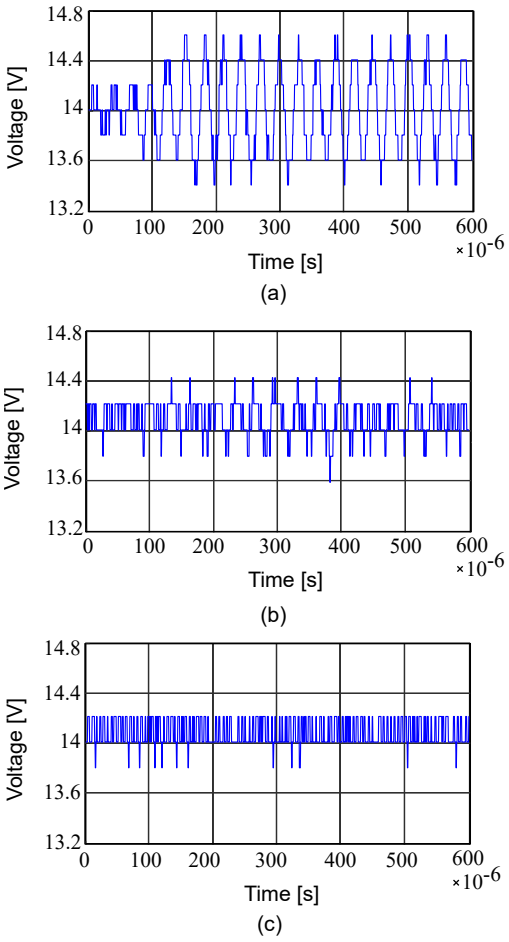

Fig. 3.10 Measured output voltage of the Boost converter. (a) $N_{\mathrm{ADC}} = 7$, $N_{\mathrm{DPWM}} = 5$; (b)$N_{\mathrm{ADC}} = 7$, $N_{\mathrm{DPWM}} = 5$, $M_{\mathrm{DTD}} = 4$; (c) $N_{\mathrm{ADC}} = 7$, $N_{\mathrm{DPWM}} = 5$, $M_{\mathrm{DDPM}} = 4$

sampling instance. The updated duty cycle resulting from this calculation is stored in the compare register of the ePWM module during each switching period. This generates a square-wave PWM signal at the designated ePWM output pin on the prototype board.

Several experiments have been conducted using different converter parameters, and the test results have been acquired and analyzed as reported below.

3.4 Results and Discussions

The results obtained both through simulations and experiments are presented in what follows.

3.4.1 LCOs Suppression

The simulated output voltages of the Boost converter, which represent different configurations of the ADC and DPWM resolution parameters, can be seen in Fig. 3.9.

The outcomes for $N_{\text{ADC}} = 7$-bits and $N_{\text{DPWM}} = 5$-bits are depicted in Fig. 3.9(a). The DPWM modulator functions at $f_{\text{clk}} = 37.5$ MHz. However, these settings and resolutions do not meet the conditions described in Chapter 2 for LCO-free operation because $N_{\text{DPWM}} \not> N_{\text{ADC}}$. Therefore, the output voltage contains low-frequency LCOs.

In Fig. 3.9(b), we can see a $M_{\text{DTD}} = 4$-bit DTD alongside a $N_{\text{DPWM}} = 5$-bit DPWM modulator, which effectively resolves the overall DTDPWM modulator of $N_{\text{DPWM}} + M_{\text{DTD}} = 9$-bits. However, while this approach suppresses LCOs, it also leads to a noticeable ripple voltage at the frequency of the thermometric dithering pattern. This is due to the distortion and noise introduced by the DTD pattern within the controller bandwidth, which a low-pass LC filter cannot effectively filter. In trying to enhance the resolution of DPWM to mitigate LCOs, the DTD performance is compromised as DTD-induced ripple is introduced. The frequency of the DTD-induced ripple is calculated as $f_{\text{sw}}/2^{M_{\text{DTD}}}$ (i.e., 73.125 kHz).

Fig. 3.9(c) presents a DDPWM modulator with a $M_{\text{DDPM}} = 4$-bit DDPM modulation and a $N_{\text{DPWM}} = 5$-bit DPWM modulator. This results in an effective resolution

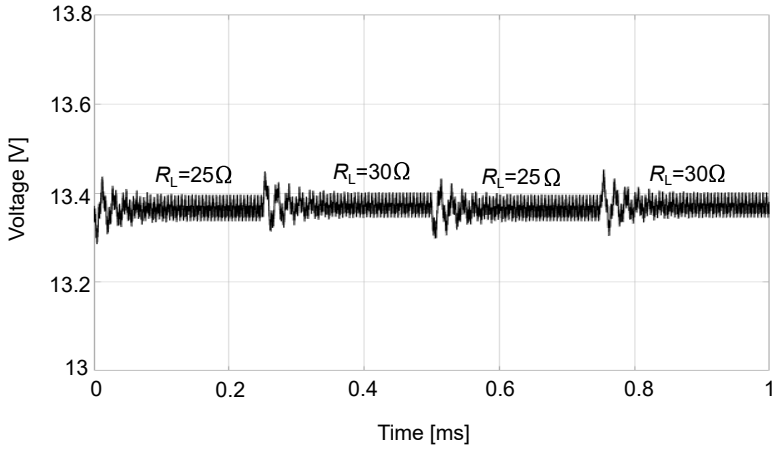

Fig. 3.11 Simulated step load transient response at output voltage.

of $N_{\text{DPWM}} + M_{\text{DDPM}} = 9$-bits. Notably, the output voltage has no ripple, and no LCOs indicate high regulation. The PID compensator generates a constant duty cycle, allowing the controller to drive the output to the zero-error bin. The dyadic pattern produces distortion and noise at high frequencies, which a low-pass LC filter can filter them effectively.

The results of a comparable experiment are shown in Fig. 3.10. The simulation outcomes are consistent with the measured voltage regulation, LCO behavior, and ripple amplitude. The observed offset in the output voltage aligns with the DC accuracy results for $N_{\text{DPWM}} = 7$ bits, as explained in the following subsection.

In addition, Fig. 3.11 illustrates the simulated transient response of the output voltage during a load step change from a minimum of 25Ω to a maximum of 30Ω. The narrow range of load resistance is dictated by the need to limit current on the lower end and to avoid bringing the right half-plane zero too close to the crossover frequency on the upper end. The results confirm that the controller effectively maintains the regulated output voltage, even with the implementation of the DDPWM modulator.

3.4.2 DC Accuracy

The ADC resolution primarily influences the output voltage's DC error, which is simulated across the entire input voltage range. To ensure LCO-free operation,

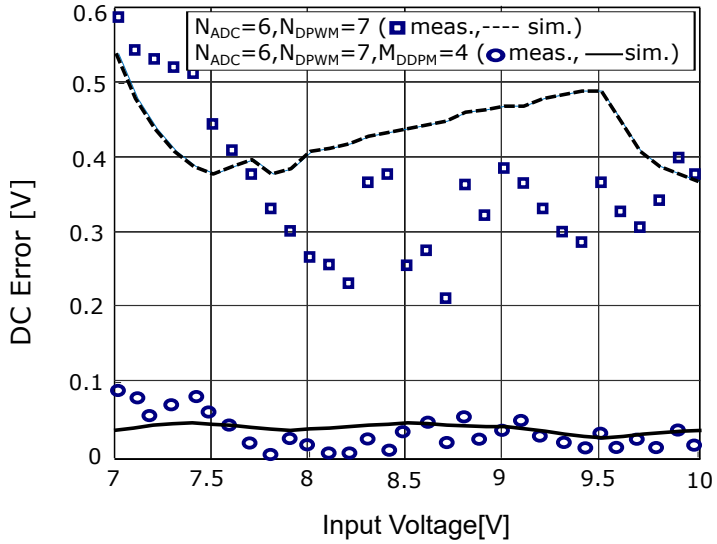

Fig. 3.12 The DC error simulated and measured, with and without 4-bit DDPM.

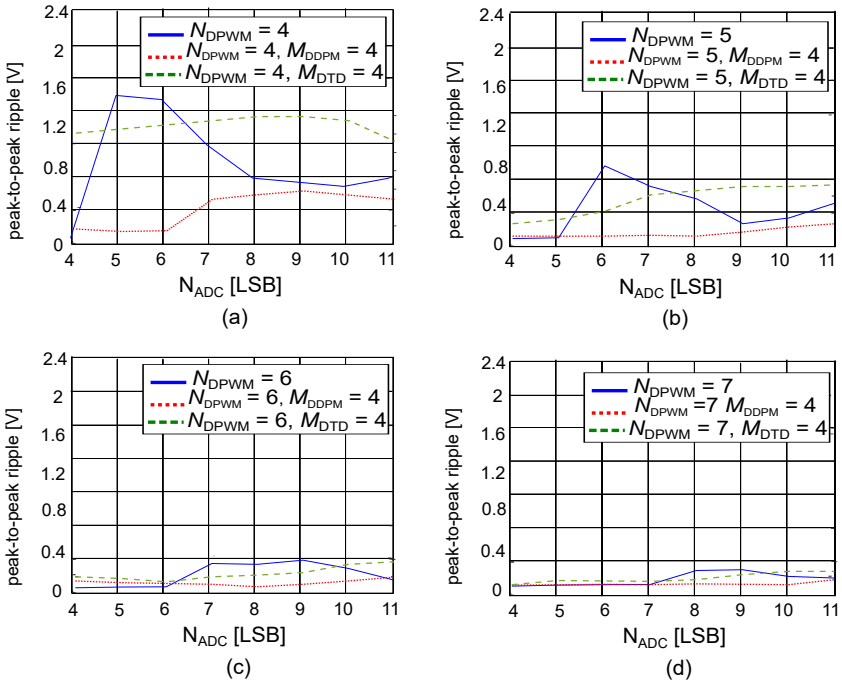

Fig. 3.13 Simulated ripple of the output voltage (a) $N_{\mathrm{DPWM}} = 4$ (b) $N_{\mathrm{DPWM}} = 5$ (c) $N_{\mathrm{DPWM}} = 6$ (d) $N_{\mathrm{DPWM}} = 7$

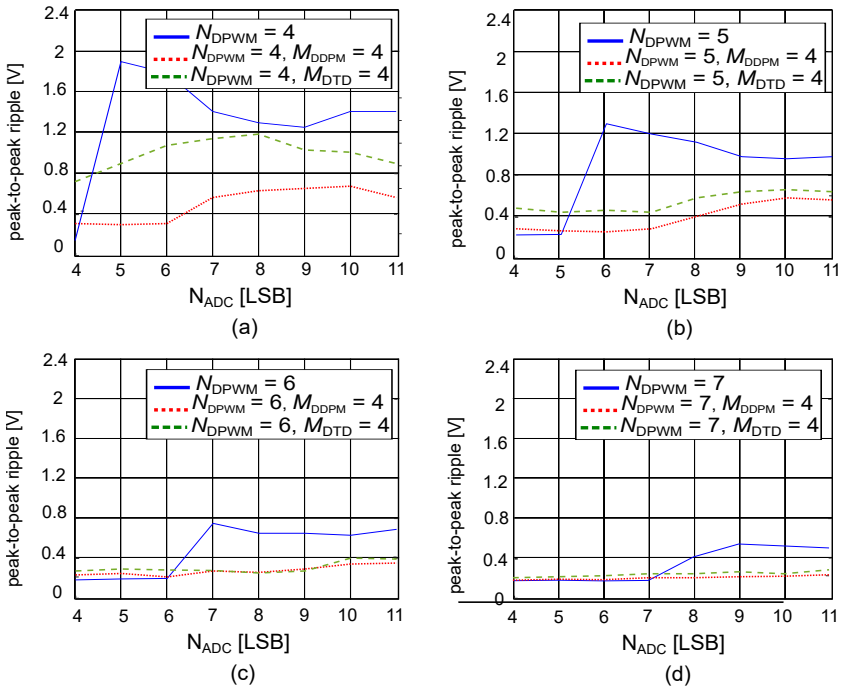

Fig. 3.14 Measured ripple of the output voltage (a) $N_{\text{DPWM}} = 4$ (b) $N_{\text{DPWM}} = 5$ (c) $N_{\text{DPWM}} = 6$ (d) $N_{\text{DPWM}} = 7$

the DPWM resolution is set to $N_{\text{DPWM}} = 7$-bits, while the ADC resolution is set to $N_{\text{ADC}} = 6$-bits. The maximum DC error, which is 540 mV, is calculated and presented in Fig. 3.12 as a dotted line.

A test with the same DPWM resolution is carried out. However, $M_{\text{DDPM}} = 4$-bits DDPM modulation is included alongside the $N_{\text{DPWM}} = 7$-bit DPWM modulator. This increases the effective resolution of the overall DDPWM modulator to $N_{\text{DPWM}} + M_{\text{DDPM}} = 11$-bits. As a result, the operation criteria mandates an ADC resolution of $N_{\text{ADC}} = 10$-bits to ensure LCO-free operation. The solid line in Fig. 3.12 shows the resulting DC error, which exhibits a maximum DC error of 60 mV, approximately 9X less than the previous case. This highlights the efficacy of DDPWM in significantly enhancing the DC accuracy of the output voltage.

Furthermore, measurement results are shown in Fig. 3.12, indicating a 6.5X reduction in DC error.

3.4.3 Output Ripple

The experiment aims to explore the amplitude of output ripple generated by different types of modulators. The experiment commences by utilizing a 4-bit plain-DPWM modulation ($N_{\text{DPWM}} = 4$) and then measures the amplitude of ripple produced across various ADC resolutions ($N_{\text{ADC}} = 4, 5, \cdots, 11$). The findings are depicted graphically in Fig. 3.13. The study is repeated for 4-bit DDPM and 4-bit DTD modulators in addition to DPWM modulation, and the results are plotted on the same graph. Additionally, the experiment is conducted again for $N_{\text{DPWM}} = 5, 6$, and 7 bits.

The data gathered indicates that the plain-DPWM modulator generates substantial output ripple as a result of limit-cycle oscillations, except in cases where $q_{\text{v}_\text{o}}^{(\text{DPWM})} \leq q_{\text{v}_\text{o}}^{(\text{ADC})}$, which satisfies the LCO-free operation criteria. The peak-to-peak amplitude of the maximum ripple reached 1.8V. The introduction of 4-bit DTD modulation considerably reduces LCOs, but the ripple amplitude remains significant and peaks at 1.5V peak-to-peak due to the impact of the DTD pattern. Conversely, the use of 4-bit DDPM modulation eliminates LCOs and reduces ripple amplitude to 0.5V peak-to-peak, a 3X enhancement.

The effectiveness of the proposed methodology is confirmed by the experimental results shown in Fig. 3.14. These results indicate that the output voltage and LCO amplitudes closely match the simulation results. The slight differences between the simulation and experimental results is due to several factors such as parasitic elements, thermal effects, and measurement inaccuracies.

3.5 Conclusion

In this chapter, a new DDPWM method is applied to a DC-DC Boost converter to enhance the DPWM resolution to eliminate LCOs. The Boost converter's efficiency is assessed through Simulink/Modelsim co-simulation and experimental testing of the hardware prototype. The Boost converter is built for Continuous Conduction Mode operation at different input voltages while keeping a fixed output voltage. The converter employs a voltage-mode digital control algorithm and works at a switching frequency in the MHz range. A comparison between the previously used thermometric dithering technique and the simulated and measured outcomes of the DDPWM modulator is made. The efficiency of DDPWM in mitigating LCO onset,

improving DC precision, and reducing ripple under various operating conditions and different ADC and DPWM resolutions is verified. The outcomes of the simulation and measurement are mainly in agreement, verifying the technique's effectiveness.

Chapter 4

Software-Defined DDPM Modulators for D/A Conversion

4.1 Motivation

Chapter 2 delves into how the spectral properties of DDPM streams have been utilized to alleviate constraints on the reconstruction filter in baseband digital-to-analog conversion [3, 4, 92]. Various hardware (HW) implementations of DDPM modulators have been explored, starting with that described in [3], which proposed two distinct DDPM modulator architectures for FPGA DAC implementation as an alternative to DPWM DAC [105] and $\Sigma - \Delta$ DAC[106]. The HW architecture presented in [3] was subsequently utilized in standard-cell-based synthesized DDPM modulators, which were integrated into 40nm CMOS, as described in [93, 107, 108]. This particular HW architecture is the basis for the DDPM modulator found in the DDPWM and the DDPM-based RF modulator presented in [91]. Another HW implementation of the DDPM modulator was proposed in [4] to achieve graceful performance degradation under frequency and supply voltage over scaling.

While implementing DDPM modulators in digital hardware has received much attention, there has been little focus on implementing DDPM modulators using software on traditional microprocessor/microcontroller hardware. This lack of attention often restricts the practical use and advantages of DDPM modulation, making it mostly suitable for ASIC or FPGA implementations.

This chapter compares different DDPM modulator architectures regarding their HW and SW implementation. Specifically, it introduces a novel DDPM modulator SW architecture and compares it with a SW architecture derived directly from the HW implementation [6]. The development of a software-defined 8-bit DDPM DAC on a readily available Texas Instruments c2000 microcontroller platform [109] is used to demonstrate the efficiency and effectiveness of these implementations.

4.2 Software Implementation of the DDPM Modulator

The following section briefly discusses the software implementations of the hardware architectures presented in Chapter 2.

The DDPM block present in the parallel DDPM modulator is described in section 2.4.5.3.A is hardwired through interconnections of different memory elements in the circuit. Therefore, this solution is not suitable for software implementation.

The Priority Mux-based DDPM modulator described in section 2.4.5.3.B poses challenges for software implementation as it relies on a priority Mux combinational network. Such networks are typically not part of arithmetic logic units (ALUs) or implemented through dedicated opcodes in general-purpose microcontrollers, making them incompatible with immediate software implementation.

In contrast, the iterative approach described in section 2.4.5.3.C is well-suited for software implementation on a general-purpose microcontroller. This approach can be converted into C-code, as outlined in Figure 4.1. Here, the LSR and RSR correspond to the `mask` and `cmask` variables, respectively. These variables are subjected to left- and right-shifting by "one" bit within each iteration of the `while` loop. The content of `mask` is combined via logical AND with the binary counter value `COUNT`. The outcome of the AND operation is examined using an `if-else` construct. The function sets the output variable `bit` to either "one" or "zero" if the condition is true. This is determined by the outcome of the AND operation between `cmask` and the input data value. This action concludes the iteration of the `while` loop. If the condition is not met, the `while` loop continues with an additional iteration, repeating the same sequence of operations until the `mask` variable reaches zero.

```
int ddpm_eval (int IN, int COUNT)
{
 int mask = 0x01;
 int cmask = 0x80;
 int loop = 1;
 int bit = 0;

 while ((loop != 0) & (cmask != 0))
    {if ((mask & COUNT) != 0)
   {bit = (cmask & IN) != 0;
    loop = 0;}
      else
  {cmask >>= 1;
   mask <<= 1;};
    }
  return bit;
}
```

Fig. 4.1 C code of an iterative 8-bit DDPM Modulator in Fig.2.24.

Nevertheless, while effective, the iterative SW implementation described above lacks efficiency in execution time. In the worst-case scenario, where only the MSB of `COUNT` is set to "one" while all other bits are "zero", it necessitates M_{DDPM} iterations of the `while` loop to produce one bit of the DDPM output stream. It is important to maintain a consistent sample rate for any input code. This consistency in sample rate limits the maximum sample rate at which the DDPM can operate, resulting in moderate performance.

4.2.1 Optimized DDPM Modulator

A new DDPM architecture has been introduced to address the limitations of the iterative DDPM modulator. This new architecture is designed to be more suitable for software implementation, and it is illustrated in Fig. 4.2.

The way this architecture works is by determining the position of the first "one" in the binary counter `COUNT` starting from the least significant bit (LSB). To accomplish this task, a bitwise XOR operation is executed by taking the counter's current value, denoted as "COUNT", and performing the XOR operation with its previous value,

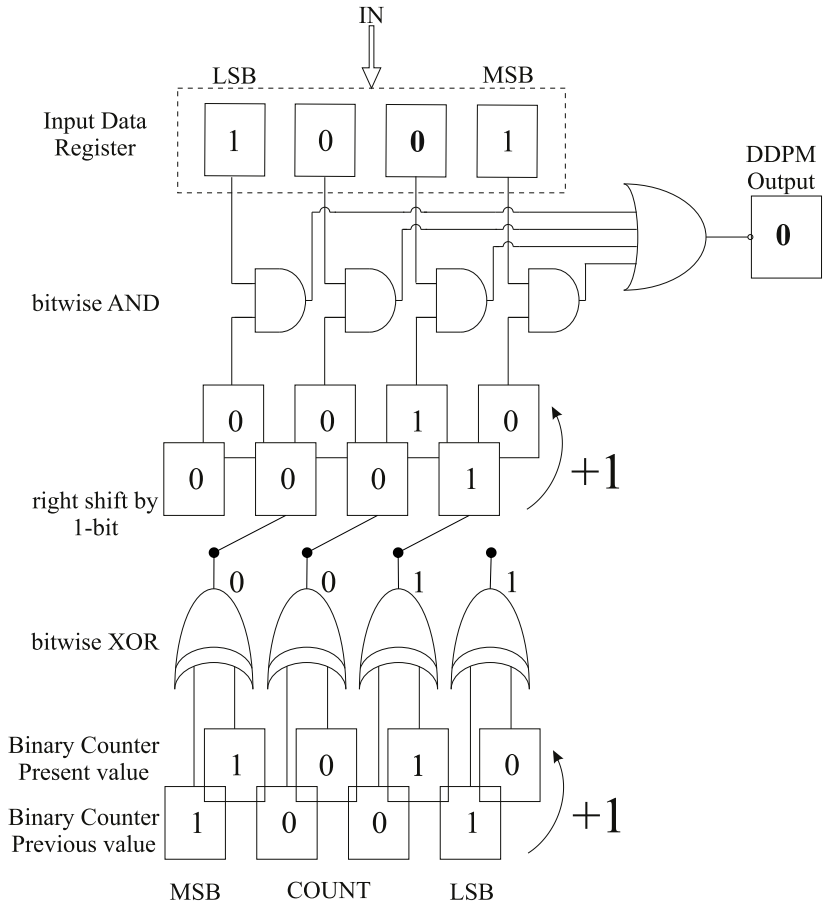

Fig. 4.2 A new optimized 4-bit DDPM modulator architecture.

```
int ddpm_eval(IN)
{
static COUNT = 0;
if(((((COUNT^(COUNT++))>>1)+1)&IN))
          bit= 1;
        else
          bit= 0;
return bit;
}
```

Fig. 4.3 C code of the new optimized DDPM Modulator in Fig.4.2.

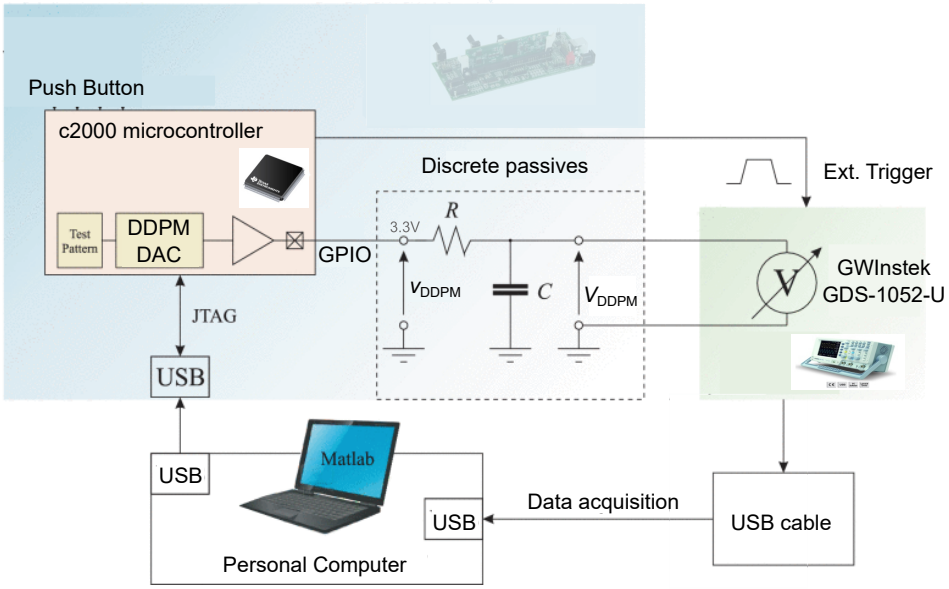

Fig. 4.4 Experimental test setup.

which is "COUNT-1". As a result of this XOR operation, a thermometric-encoded binary word is obtained. In this binary word, all bits from the least significant bit (LSB) up to the first "one" in "COUNT" are set to high, while the remaining bits, up to the most significant bit (MSB), are set to low.

The next step involves shifting the thermometric-encoded binary word to the right by one position while incrementing it by one unit. This creates a new word with a single "one" bit positioned at the location of the first "one" in the binary counter from the LSB.

Finally, the DDPM stream bit corresponding to `COUNT` is obtained by logically ANDing the bit-reversed DDPM input with the word created in the previous step. This output results from the DDPM procedure, which can be used for various software applications. The presented architecture is more suitable for software implementation and can be transformed into C code, as shown in Fig. 4.3. The XOR operation between `COUNT` (pre-increment) and `COUNT++` (post-increment, representing the current counter value) identifies the position of the first "one" in a thermometric-encoded format. For instance, if the first "one" is positioned at the second LSB position (`COUNT=1010`), the XOR output will contain two "ones" (`0011`). The position of the first "one" can be determined by right-shifting this result by one position and then increasing it by one unit. The output obtained from the previous

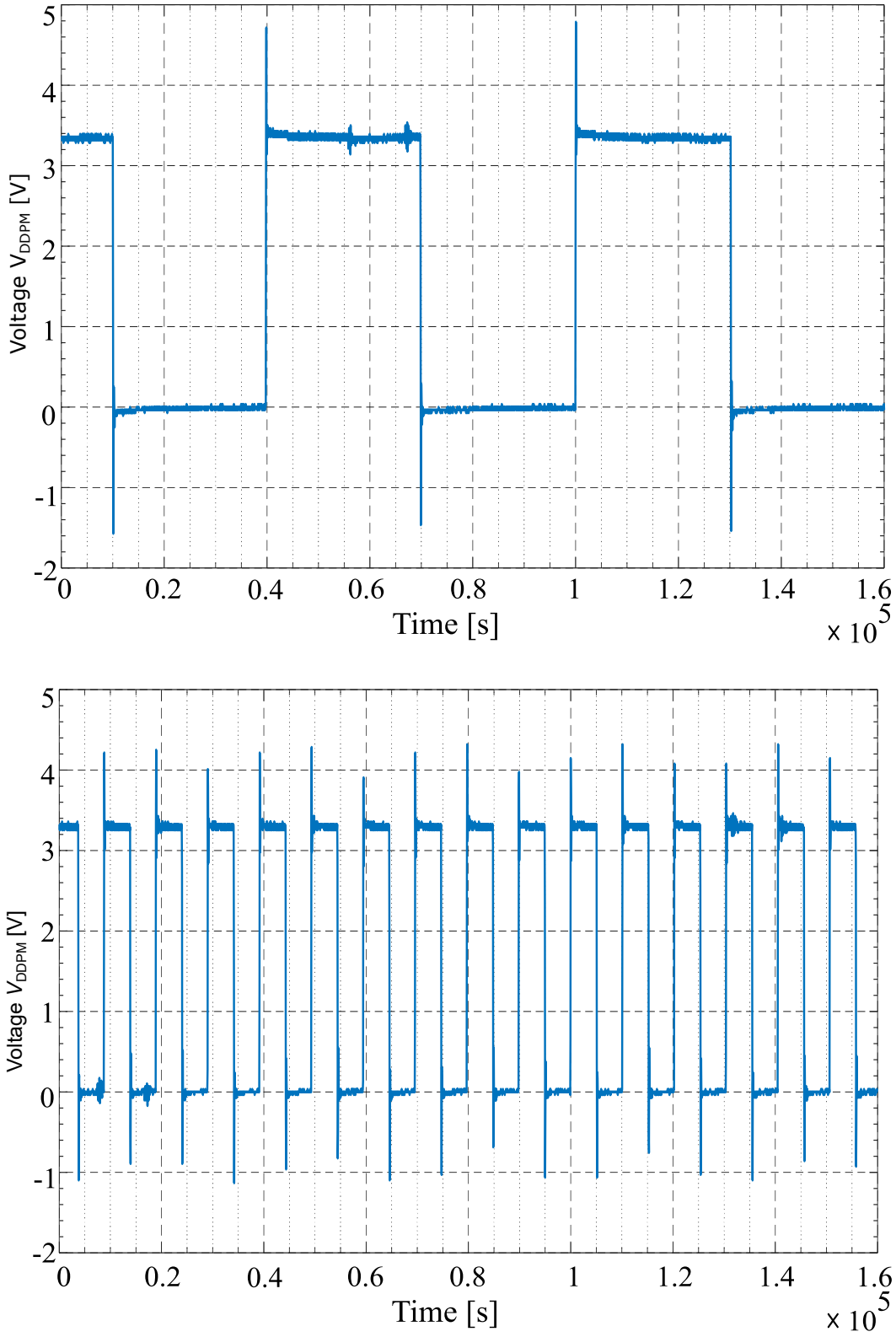

Fig. 4.5 iterative 8-bit DDPM bitstream and proposed 8-bit DDPM bitstream for input code m=127 (0x7F) over time.

step, such as "0010" in the given example, is subjected to an AND operation with the input data. To ensure proper alignment of respective bit positions, bit reversal of the input data is necessary. It is worth noting that the input bit-reversal operation is only necessary once in a DDPM pattern that covers $2^{M_{\mathrm{DDPM}}}$ clock periods and DDPM function evaluations, thus having a negligible impact on execution time. Finally, based on the outcome of the logical AND operation (the if-condition in the code), the DDPM output is updated. In the given example, when the input data is set as `IN=1001`, the DDPM output considers a value of "zero". This is because the second MSB of the input data corresponds to the second LSB of the counter value, which is set to "zero".

The entire M_{DDPM}-bit binary counter is evaluated concurrently in this architecture to determine the DDPM output code, significantly reducing execution time. This improvement ensures that the achievable sample rate is independent of the modulator's bit length M_{DDPM}, thereby significantly boosting performance, particularly for larger values of M_{DDPM}.

4.3 Hardware Test Setup and Experimental Results

Two DDPM DAC prototypes were created on a c2000 microcontroller platform [109] to assess the efficacy of the DDPM modulators. These prototypes had 8-bit resolution and utilized the straightforward iterative method and the optimized SW implementation. Their static and dynamic performance was assessed and compared through experimental means.

4.3.1 Microcontroller-Based DDPM DAC and Experimental Test Setup

The proposed DDPM technique's effectiveness has been demonstrated by implementing both the proposed and iterative 8-bit software-defined DDPM modulators. These modulators are based on the architectures depicted in Fig. 4.2 and Fig. 2.24, respectively. They have been implemented using the C language on a Texas Instruments c2000 microcontroller. These implementations aim to drive a 3.3 V general-purpose digital output with a DDPM pulse. The DDPM pulse is obtained by running the

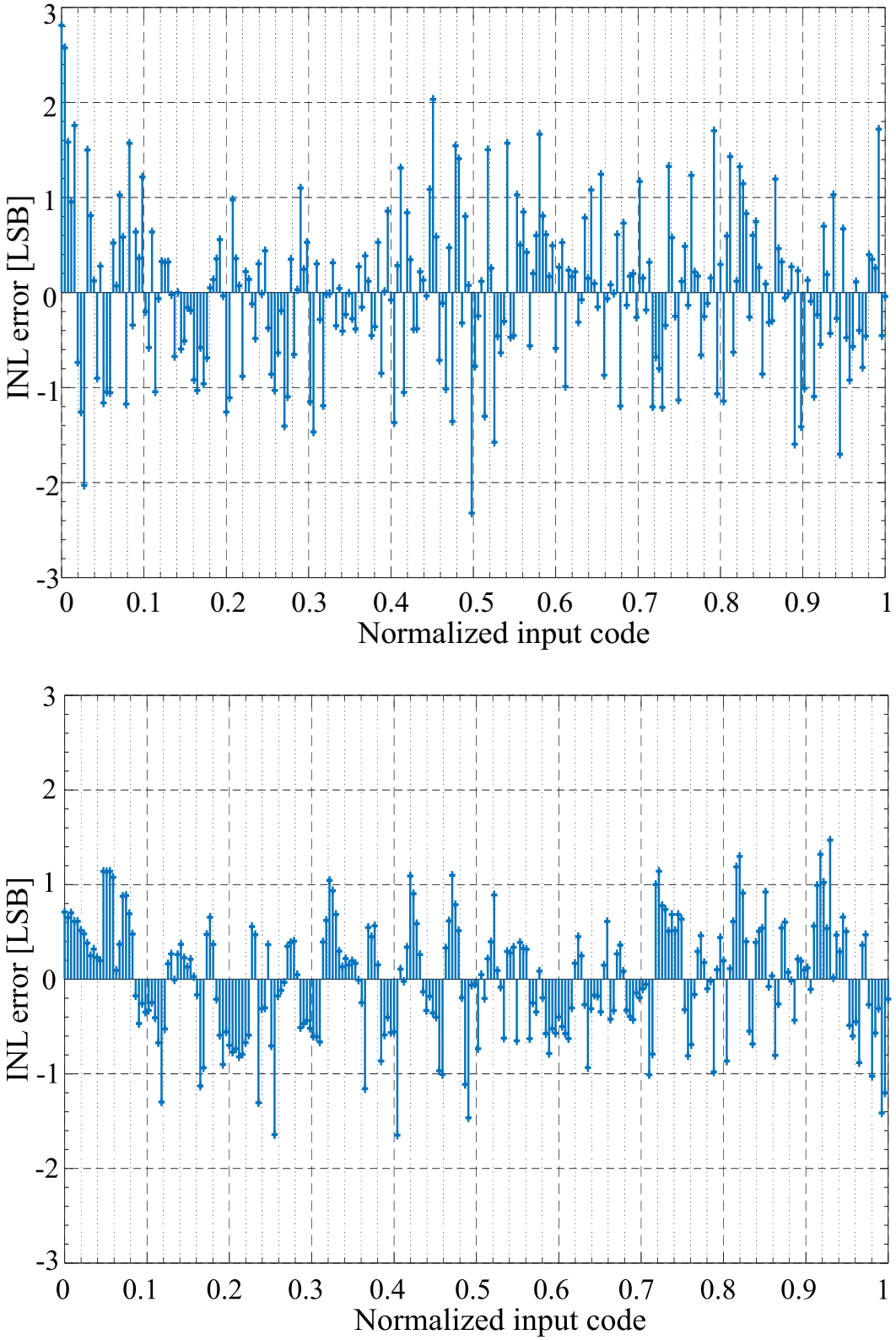

Fig. 4.6 Comparison of Integral non-linearity (INL) error between the iterative 8-bit DDPM DAC (top) and the proposed 8-bit DDPM DAC (bottom) against normalized input code.

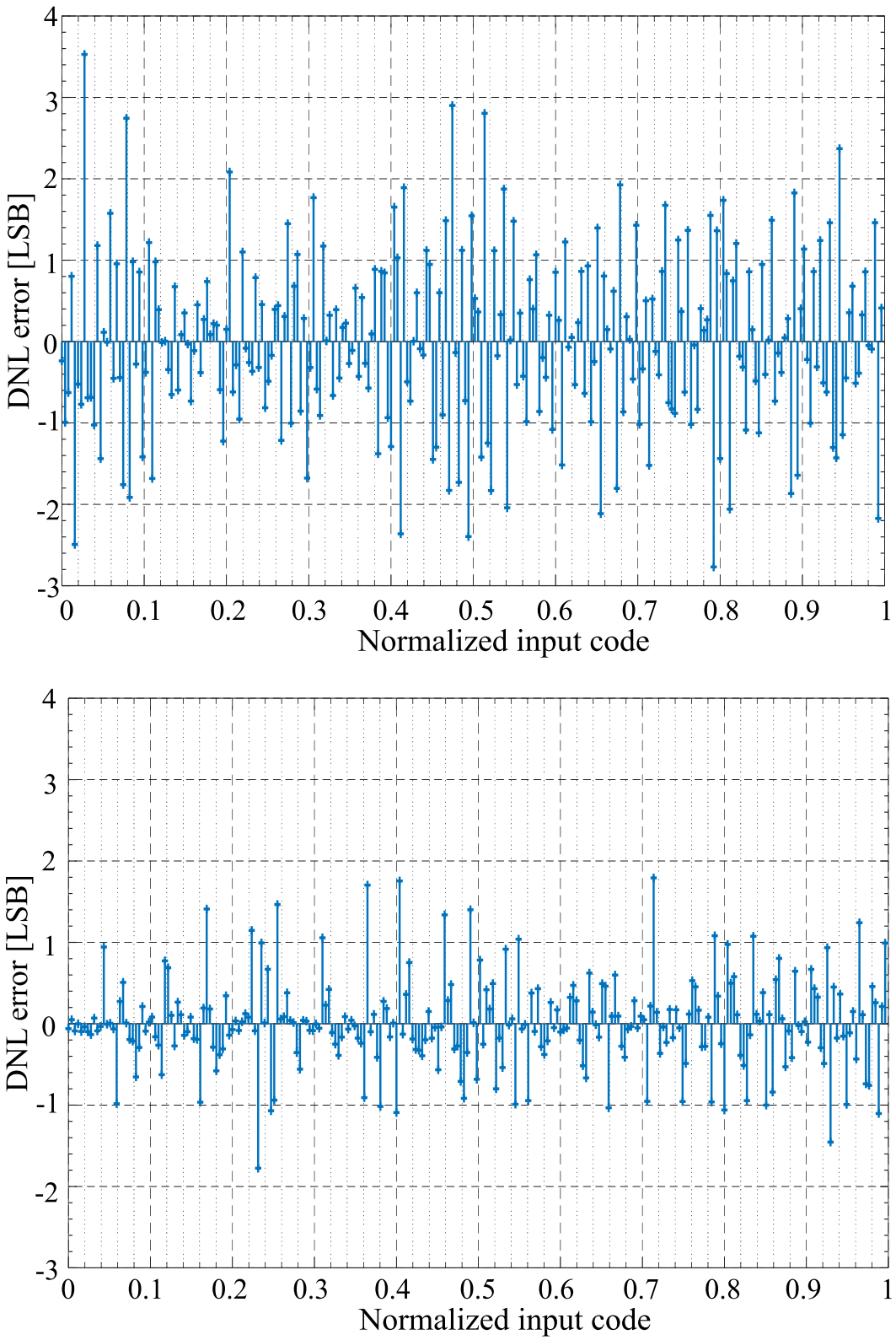

Fig. 4.7 Comparison of Differential non-linearity (DNL) error between the iterative 8-bit DDPM DAC (top) and the proposed 8-bit DDPM DAC (bottom) against normalized input code.

code in Fig. 4.1 for the iterative implementation and in Fig. 4.3 for the proposed optimized implementation. This corresponds to a periodically-generated interrupt signal from the c2000 microcontroller timer peripheral [109].

To ensure that the DDPM DAC operates correctly, both the iterative and optimized DDPM modulators are adjusted to the minimum interrupt period. The DDPM DACs are software-defined and function at a system clock frequency of 150MHz. An onboard output *RC* filter is included in the DDPM DACs, with $R = 100$ kΩ and $C = 1$ nF.

The measurement process of the DAC output voltage $V_{\mathrm{DDPM}}(m)$ has been conducted under static conditions and sine-wave input. The test setup depicted in Fig. 4.4 has been employed for this purpose. The double-slope error digital compensation technique described in [3, 4, 92, 93, 107] has also been used in the measurement process. This technique involves applying a digitally-pre-distorted input code m', derived from the integer m to be converted to ensure accurate measurement.

$$m' = \begin{cases} \lceil \frac{m}{1+\alpha} \rfloor & \text{for } 0 \leq m < 2^{M_{\mathrm{DDPM}}-1}(1+\alpha) \\ \lceil \frac{m-(2^{M_{\mathrm{DDPM}}}-1)\alpha}{1-\alpha} \rfloor & \text{for } 2^{M_{\mathrm{DDPM}}-1}(1+\alpha) \leq m < 2^{M_{\mathrm{DDPM}}} \end{cases} \tag{4.1}$$

The operator $\lceil \cdot \rfloor$ rounds to the nearest integer. A compensation factor α is determined through one-time calibration. This factor compensates for errors arising from the unbalanced rise/fall times in the digital pulses generated by the microcontroller output drivers [3].

4.3.2 Experimental Results

A Fig.4.5 displays the digital bitstream outputs obtained by a digital oscilloscope for both the iterative and proposed optimized DDPM modulators for the input code m = 127 (0x7F).

The input code results in a bitstream sequence alternating between "zero" and "one". The sequence comprises $2^{M_{\mathrm{DDPM}}}/2$ pulses representing "ones" and the remaining $2^{M_{\mathrm{DDPM}}}/2$ pulses representing "zeros". Each pulse's minimum duration, denoted as T_{DDPM}, is determined by the internal timer interrupts within our microcontroller platform. For the optimized DDPM implementation, T_{DDPM} is 500ns, while for the iterative implementation, it is 3μs. With an $M_{\mathrm{DDPM}} = 8$-bit DDPM DAC, the

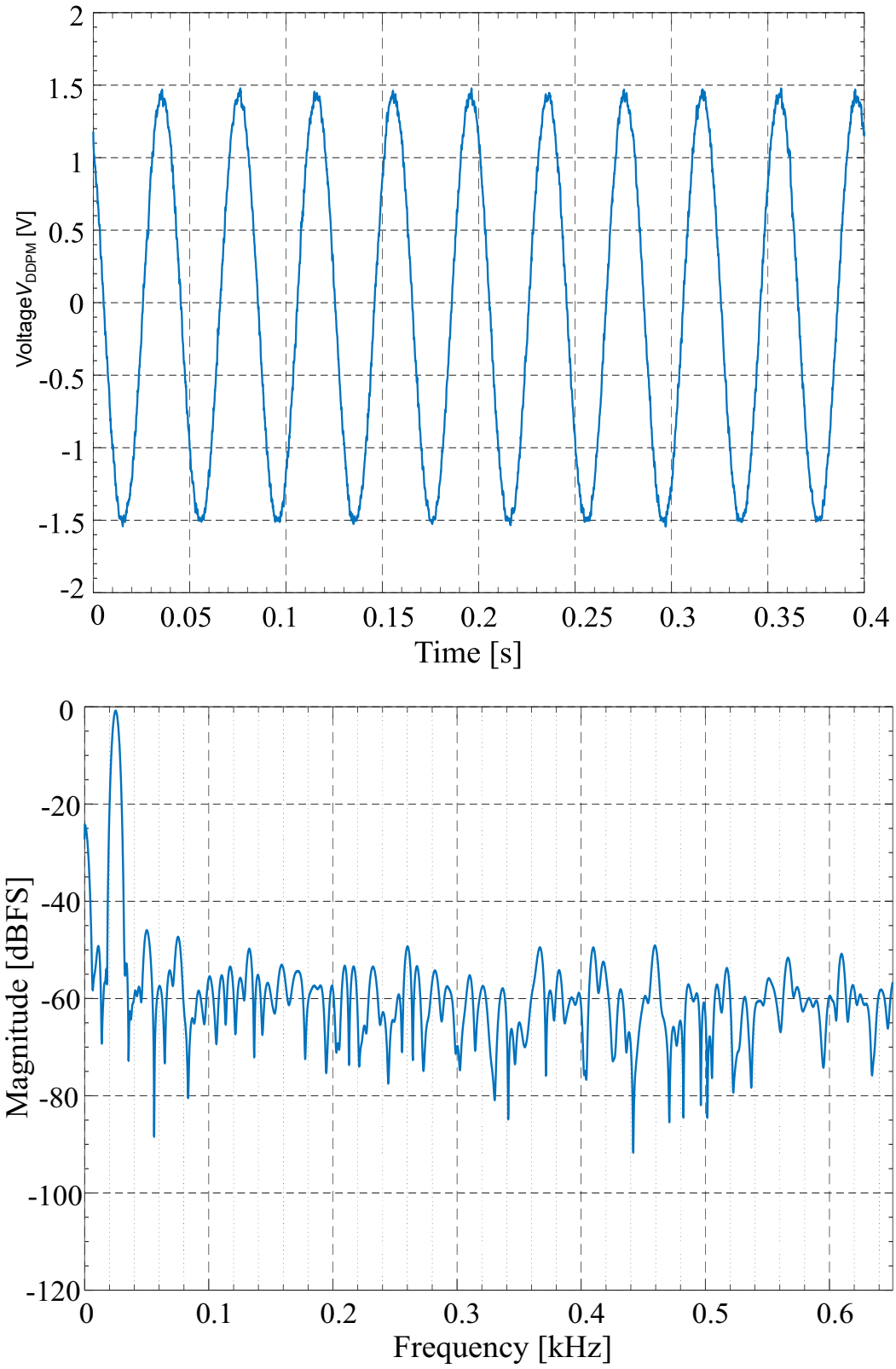

Fig. 4.8 The performance of the iterative 8-bit DDPM DAC under a 25 Hz sine wave input evaluated by analyzing its time-domain output waveform (top) and power spectral density (bottom).

maximum sample rate f_S can be calculated using the formula $f_S = f_{DDPM}/2^{M_{DDPM}}$. For the optimized and iterative implementations, this implies maximum sample rates of 7.81 kS/s and 1.30 kS/s, respectively, as summarized in Tab. 4.1.

The integral non-linearity (INL) error of the two DDPM DACs can be determined by analyzing their static input-output trans-characteristic, i.e.,

$$\mathrm{INL}[m] = \frac{V_{DDPM}[m] - \frac{V_{DD}}{2^{M_{DDPM}}} \cdot m}{\mathrm{LSB}_8}, \tag{4.2}$$

where $\mathrm{LSB}_8 = V_{DD}/2^8 = 12.9$ mV is the LSB at 8-bit resolution and the differential nonlinearity (DNL), error evaluated as:

$$\mathrm{DNL}[m] = \mathrm{INL}[m+1] - \mathrm{INL}[m] \tag{4.3}$$

are reported in Fig.4.6 and Fig.4.7, respectively. The (iterative) optimized DDPM DAC displays a maximum INL of below 2.80 (1.64) LSBs and a maximum DNL below 3.53 (1.79) LSBs. This demonstrates superior static linearity for the optimized converter, with a maximum INL improvement of 1.19 LSB and a maximum DNL improvement of 1.74 LSB. The improvement is attributed to the simpler implementation of the converter, which leads to reduced internally generated switching noise.

The input codes $x[m]$ are generated to achieve dynamic characterization. These codes correspond to a sine wave with a frequency of 25Hz and an amplitude that is 90% of the full swing.

$$x[m] = 2^{M_{DDPM}-1} + 0.9 \cdot 2^{M_{DDPM}-1} \cdot \sin(2\pi m f_o/f_S) \tag{4.4}$$

where, f_o = 25 Hz and m is the discrete-time index.

The time-domain and frequency-domain output of the DACs under a sine wave input are shown in Fig. 4.8 and Fig. 4.9. We utilized the "pwelch" MATLAB function to obtain the DAC waveforms' power spectra (PS). Using eqs. (4.5), (4.6), and (4.7), we calculated the signal-to-noise and distortion ratio (SNDR), spurious-free dynamic range (SFDR), and an effective number of bits (ENOB) based on these power spectra measurements. SNDR, which is the ratio of the fundamental signal power to the

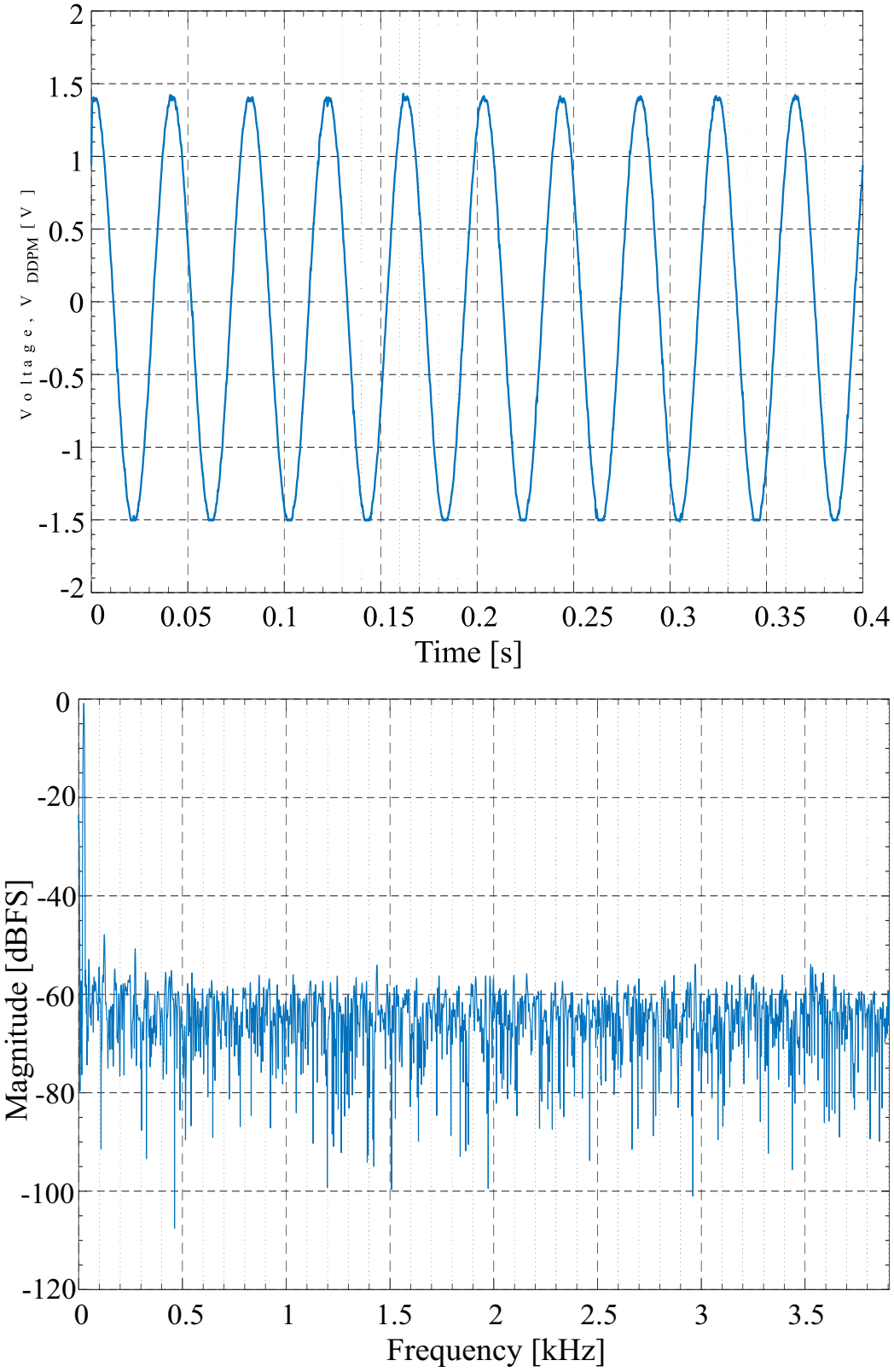

Fig. 4.9 The performance of the proposed 8-bit DDPM DAC under a 25 Hz sine wave input was evaluated by analyzing its time-domain output waveform (top) and power spectral density (bottom).

power of all other spectral components (excluding DC), was calculated as:

$$\mathrm{SNDR_{dB}} = 10\log_{10}\frac{\mathrm{PS}(f_0)}{\sum \mathrm{PS}(f)_{|f\neq f_0 \vee f\neq 0}} \tag{4.5}$$

The SFDR is defined as

$$\mathrm{SFDR_{dB}} = \mathrm{PS_{dBFS}}(f_0) - \mathrm{PS_{dBFS}}(f_m) \tag{4.6}$$

where $\mathrm{PS_{dBFS}}(f_0)$ is the power of the fundamental frequency f_0 and $\mathrm{PS_{dBFS}}(f_m)$ is the largest spurious power in dB for the full swing (dBFS).

The effective number of bits (ENOB) of the converter is ultimately determined based on the SNDR as

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76\mathrm{dB}}{6.02\mathrm{dB/bit}} \tag{4.7}$$

The results from the measurements have been used to calculate the SNDR, SFDR, and ENOB for the proposed and iterative DDPMs. The equations mentioned earlier are used to present the results in Tab. 4.1. The optimized SW DDPM DACs have SFDR values of 47.02dB and 45.16dB for the proposed and iterative converters, respectively. The measured SNDR values are 45.27dB and 41.61dB for the two converters, corresponding to 7.23 and 6.62 effective bits (ENOB). These values are comparable. The optimized DDPM DAC has a 6X higher sample rate and 0.61 bit higher effective resolution.

4.3.3 Discussion and Comparison

The measurements conducted on the microcontroller have been compiled in Tab.4.1. The table also compares these measurements with the DDPM and non-DDPM FPGA DAC implementations proposed in recent years.

The improved SW DDPM DAC presented in this thesis outperforms the basic iterative SW implementation in all aspects, as shown in the table. The maximum achievable sample rate is 7.812 kS/s, marking a significant 6X increase over the 1.302 kS/s of the iterative SW DDPM DAC implementation, which broadens its potential applications. The proposed converter's peak INL error amounts to 1.64 LSBs, while the iterative converter records 2.8 LSBs, as revealed by the examination of static characteristics. The superiority of the proposed DAC is further highlighted

Table 4.1 Comparison table based on experimental results [6]

Param.	Unit	Prop.SW DDPM	Iter.SW DDPM	FPGA DDPM	FPGA DPWM	FPGA ΣΔ
Pubbl.		This Work	This Work	[3]	[106]	[105]
Res.	bit	8	8	16	8	16
Syst. Clk. f_{clk}	MHz	150	150	100	25	10
Mod.Clk. f_{DDPM}	MHz	2	0.33	100	N/A	N/A
Sample Rate	kS/s	7.812	1.302	1.525	20	20
Supply	V	3.3	3.3	1.8	±9	3.3
INL	LSB	1.64	2.80	13	N/A	N/A
DNL	LSB	1.79	3.53	1	N/A	N/A
SNDR	dB	45.27	41.61	N/A	N/A	57.3
SFDR	dB	47.02	45.16	N/A	78	37
ENOB	bit	7.23	6.62	12.1	N/A	9.2
Memory	kB	1638	1720	N/A	N/A	N/A
Res.	kΩ	100	100	180	N/A	0.1
Cap.	nF	1	1	1	N/A	80

by the measured DNL, which is 1.793 LSBs compared to 3.53 LSBs for the iterative approach. Dynamic characterization metrics such as SNDR, SFDR, and ENOB also clearly indicate the improvements achieved. In addition, the proposed SW DDPM is more memory-efficient than the iterative iteration.

As outlined in the table, in comparison to FPGA implementations of both DDPM and non-DDPM DACs, such as the Digital PWM FPGA DAC in [106] and the FPGA ΣΔ DAC in [105], the proposed DDPM DAC achieves similar sample rate performance (5X greater than [3], 2.5X less than [105, 106]) but exhibits slightly lower effective resolution (2.0-4.8 effective bits less than [3, 105]. This proposed DDPM DAC stands out from the other alternatives by not requiring expensive programmable logic devices. Instead, it can be easily implemented through software on a general-purpose microcontroller at a significantly lower cost.

Chapter 5

Conclusion

Power electronics has developed into a well-established discipline with proven technologies, particularly in Switch-mode Power Supplies (SMPS) based on discrete components and conventional analog control strategies. However, recent advancements in large bandgap semiconductor devices, including silicon carbide (SiC), gallium arsenide (GaAs), and gallium nitride (GaN), offer new opportunities for high-frequency power conversion up to multi-MHz. These advancements have the potential to significantly increase achievable power densities, driving innovation in power electronics. They have also spurred research into integrating control circuits and power devices on the same semiconductor chip, a concept known as digital control in power electronics. Digital controllers increasingly replace analog counterparts in modern SMPS due to their flexibility, reliability, cost-effectiveness, and reduced susceptibility to aging.

Although they have several benefits, they encounter a specific problem: low-frequency steady-state Limit-cycle Oscillations (LCOs). These LCOs are caused by quantization effects from the Analog-to-Digital Converter (ADC) and the Digital Pulse Width Modulator (DPWM). Although high-resolution ADCs and DPWMs can alleviate these problems, they also introduce higher costs and more complexity, particularly for SMPS operating at high switching frequencies using emerging semiconductor technology like GaN and SiC power transistors.

Several high-resolution DPWM techniques have been proposed to address these challenges and enhance DPWM resolution. This has motivated further research into high-resolution DPWM in digitally controlled SMPS and the design of DPWM-based

Digital-to-Analog Converters (DACs), as explored and presented in this thesis. The contributions related to these areas are summarized below.

Digitally Controlled Power Converters:
An in-depth theoretical analysis of LCOs in digitally controlled power converters has been presented. The discussion outlines quantization effects, techniques for determining steady-state DC solutions, and guidelines for preventing LCOs. This analysis has explored state-of-the-art DPWM techniques, including Sigma-Delta ($\Sigma\Delta$) modulation, delay line modulation, Digital Thermometric Dithering Pulse Width Modulation (DTDPWM) modulation, and the recently proposed Dyadic Digital Pulse Width Modulation (DDPWM), aimed at enhancing resolution and mitigating LCO onset. In comparing Buck and Boost converters regarding the output voltage quantization steps in terms of the duty cycle., it has been highlighted that meeting DPWM resolution requirements is more challenging in Boost converters than in Buck converters.

An approach to implement the digitally controlled Boost converter based on DDPWM has been presented. Through Simulink/Modelsim co-simulations and experimental testing on a voltage-mode, 7-10 V input, 13.8 V output Boost converter operated at a 1.17 MHz switching frequency under different operating conditions and ADC/DPWM resolutions, the effectiveness of DDPWM in suppressing the onset of LCOs, increasing DC accuracy, and reducing output ripple has been verified. The accuracy in DC has been increased by more than 6X compared to plain DPWM, while the output ripple has been reduced by approximately 3X compared to DTDPWM.

Software-Defined DDPM Modulators for DAC Conversion
As a second contribution, a theoretical evaluation of Dyadic Digital Pulse Modulation (DDPM) and its spectral characteristics have been presented, followed by a comparison of DDPM modulators' existing hardware (HW) implementations.

In addition, a newly developed optimized DDPM modulator architecture designed explicitly for software (SW) implementation has been introduced and compared with an SW architecture derived from directly transferring the HW implementation. To evaluate the proposed SW DDPM modulator's effectiveness and efficiency, an 8-bit DDPM DAC has been implemented using software on a commercially available Texas Instruments c2000 microcontroller platform, showcasing its practical application.

Table 5.1 Comparison table based on experimental results

Param.	Unit	Prop.SW DDPM	Iter.SW DDPM	FPGA DDPM	FPGA DPWM	FPGA ΣΔ
Pubbl.		This Work	This Work	[3]	[106]	[105]
Res.	bit	8	8	16	8	16
Syst. Clk. f_{CLK}	MHz	150	150	100	25	10
Mod.Clk. f_{DDPM}	MHz	2	0.33	100	N/A	N/A
Sample Rate	kS/s	7.812	1.302	1.525	20	20
Supply	V	3.3	3.3	1.8	±9	3.3
INL	LSB	1.64	2.80	13	N/A	N/A
DNL	LSB	1.79	3.53	1	N/A	N/A
SNDR	dB	45.27	41.61	N/A	N/A	57.3
SFDR	dB	47.02	45.16	N/A	78	37
ENOB	bit	7.23	6.62	12.1	N/A	9.2
Memory	kB	1638	1720	N/A	N/A	N/A
Res.	kΩ	100	100	180	N/A	0.1
Cap.	nF	1	1	1	N/A	80

The results obtained from the microcontroller tests are outlined in Tab. 5.1, which also includes a comparison to recent DDPM and non-DDPM FPGA DAC implementations.

The proposed SW DDPM DAC, as shown in the table, performs better than the simple iterative SW implementation in all aspects. Its maximum sample rate is 7.812 kS/s, which is 6X higher than the iterative SW DDPM DAC implementation, significantly expanding its potential applications. The static characteristics demonstrate that the peak INL error of the proposed converter is only 1.64 LSBs, compared to 2.8 LSBs for the iterative converter. Additionally, the superiority of the proposed DAC is evident through the measured DNL of 1.79 LSBs, which is much lower than the 3.53 LSBs for the iterative implementation. Finally, the proposed DAC shows considerable improvements regarding dynamic characterization metrics such as SNDR, SFDR, and ENOB.

The proposed DDPM DAC achieves similar sample rates as FPGA implementations of DDPM DACs [3] and non-DDPM DACs, such as the DPWM FPGA DAC

in [106] and the FPGA ΣΔ DAC in [105], as shown in Tab. 5.1. However, it has a marginally lower effective resolution, with 2.0-4.8 effective bits less than [3, 105]. Unlike these alternatives, it doesn't require costly programmable logic devices, and it can be easily integrated into software on widely available general-purpose microcontroller units at minimal expense.

Appendix A

Computation of PID Compensator Gains

The PID compensator transfer function as given in (2.8) is

$$G_{\mathrm{PID}}(z) = K_{\mathrm{p}} + \frac{T_{\mathrm{s}} K_{\mathrm{i}}}{1 - z^{-1}} + \frac{K_{\mathrm{d}}}{T_{\mathrm{s}}}(1 - z^{-1}) \tag{A.1}$$

By applying bilinear transformation (i.e., $z(p) = \frac{1+pT_s/2}{1-pT_s/2}$) in (A.1), the $G_{\mathrm{PID}}(z)$ can be transformed into p-domain, denoted as $G'_{\mathrm{PID}}(p)$, as

$$G'_{\mathrm{PID}}(p) = K_p + \frac{K_i}{T_{\mathrm{s}}}\left(1 + \frac{p}{\omega_p}\right)\frac{K_d T_{\mathrm{s}} p}{1 + \frac{p}{\omega_p}} \tag{A.2}$$

which asymptotic Bode plots are shown in Fig. A.1.

For design purposes, the (A.2) can be rewritten in the multiplicative form:

$$G'_{\mathrm{PID}}(p) = G'_{PI\infty}\left(1 + \frac{\omega_{PI}}{p}\right) G'_{PD0}\frac{1 + \frac{p}{\omega_{PD}}}{1 + \frac{p}{\omega_p}} \tag{A.3}$$

Calculating all the z-domain frequency specifications into corresponding p-domain specifications:

$$\omega'_c = \frac{2}{T_{\mathrm{s}}}\tan(\omega_c T_{\mathrm{s}}/2) \tag{A.4}$$

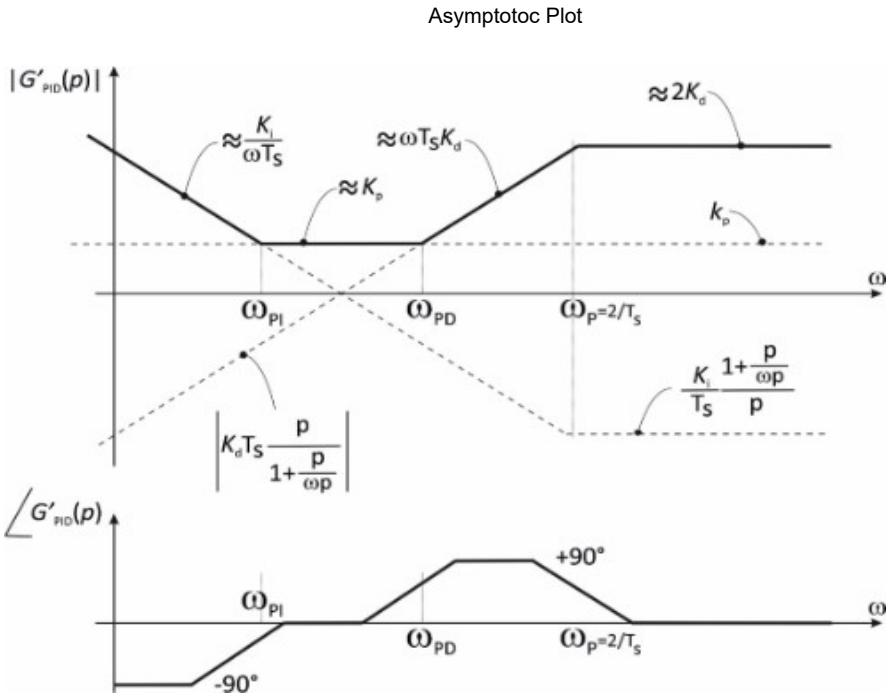

Fig. A.1 Asymptotic Bode plots of the digital PID compensator in the p-domain

$$\omega_p = \frac{2}{T_s} \tag{A.5}$$

Finally, the z-domain PID gains can be calculated as:

$$\begin{aligned}
K_p &= G'_{PI\infty} G'_{PD0} \left(1 + \frac{\omega_{PI}}{\omega_{PD}} - 2\frac{\omega_{PI}}{\omega_p}\right) \\
K_i &= 2G'_{PI\infty} G'_{PD0} \frac{\omega_{PI}}{\omega_p} \\
K_d &= \frac{G'_{PI\infty} G'_{PD0}}{2} \left(1 - \frac{\omega_{PI}}{\omega_p}\right)\left(\frac{\omega_p}{\omega_{PD}} - 1\right)
\end{aligned}$$

The ω_{PD} can be computed using Fig. A.1 as [110],

$$\omega_{PD} = \frac{\omega'_c}{\tan(\phi_m - \phi_{m,u} + \tan^{-1}(\omega'_c/\omega_p))} \tag{A.6}$$

where

$$\phi_{m,u} \triangleq \pi + \arg(G'_{uv}(j\omega'_c))$$

.

The upper and a lower bound for the achievable phase margin ϕ_m is,

$$\phi_{m,u} < \phi_m < \phi_{m,u} + \pi/2 - \arctan(\frac{\omega_c'}{\omega_p})$$

. The PD action is determined by imposing that loop gain has unity magnitude and $-\pi + \phi_m$ phase at ω_c':

$$G_{PD0}' = \frac{1}{|G_{uv}'(j\omega_c')|} \frac{\sqrt{1+(\omega_c'/\omega_p)^2}}{\sqrt{1+(\omega_c'/\omega_{PD})^2}} \tag{A.7}$$

An integral action is introduced to eliminate the steady-state regulation error, after which the zero related to the PI controller, denoted as ω_{PI}, must maintain the crossover frequency and phase margin achieved through the PD compensation. Any modifications to the high-frequency PI gain, denoted as $G_{PI\infty}'$, must not impact the magnitude of loop gain around the crossover frequency ω_C. For these reasons,

$$\omega_{PI} = \frac{1}{20}\omega_c \tag{A.8}$$

and

$$G_{PI\infty}' = 1 \tag{A.9}$$

For the HDL implementation through Verilog code, the hardware dynamic ranges of all the signals in the PID compensator can be computed using the following formula:

$$n = 1 + \left\lceil \frac{\mathrm{DR_{hw}}[x']_q^n}{20\log 2} \right\rceil \tag{A.10}$$

where,

$$\mathrm{DR_{hw}}[x']_q^n = 20\log_{10}\left(\left\lceil \frac{x'}{2^q} \right\rceil\right)$$

Appendix B

Published Papers

Journal Papers:

- **A. Abdullah**, F. Musolino and P. S. Crovetti, "Limit-Cycle Free, Digitally-Controlled Boost Converter Based on DDPWM," in IEEE Access, vol. 11, pp. 9403-9414, 2023, doi: 10.1109/ACCESS.2023.3239883.
- **A. Abdullah**, F. Musolino and P. Crovetti, "Software-Defined DDPM Modulators for D/A Conversion by General-Purpose Microcontrollers," in IEEE Access, vol. 10, pp. 17515-17525, 2022, doi: 10.1109/ACCESS.2022.3150865.
- **A. Abdullah**, F. Musolino and P. Crovetti, "Detection and Suppression of Intentional EMI Attacks to Smart Speakers," in IEEE TEMC, (Accepted for publication).

Conference Papers:

- P. Crovetti, R. Rubino, **A. Abdullah** and F. Musolino, "Emerging Relaxation and DDPM D/A Converters: Overview and Perspectives," 2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS), Fukuoka, Japan, 2022, pp. 1-6, doi: 10.1109/MWSCAS54063.2022.9859310.
- F. Musolino, **A. Abdullah**, M. Pavone, F. Ferreyra and P. Crovetti, "Design and efficiency analysis of an LCL Capacitive Power Transfer system with Load-Independent ZPA," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. 1-8.

Conference Presentation:

- **A. Abdullah**, F. Musolino, P. Crovetti, "Limit-Cycle free digitally controlled power converter", Conference presentation at 52nd Annual Meeting off the Associazione Società Italiana di Elettronica ((SIE)), 2021.

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