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Characterization of the radiation tolerant ToASt ASIC for the readout of the PANDA MVD strip detector

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Abstract: The ToASt ASIC is a 64-channel integrated circuit developed for the readout of the Silicon strip detector project designed to be placed in the Micro-Vertex Detector of the PANDA experiment. ToASt is implemented in a commercial 110 nm CMOS technology and can provide information on the position, time, and deposited energy of the particle passing through the detector. Its time resolution is given by its 160 MHz master clock. The ASIC has been developed in the framework of the European FAIRnet project. The chip has been characterized electrically both standalone and coupled with sensors, with focus on its noise performances. It has also been tested for radiation tolerance, both in terms of Total Ionizing Dose and Single Event Upset. In particular, this work aims to guarantee that the studied ASICs can sustain the levels of ionizing radiation expected in the PANDA experiment and to study the noise characteristics for the two polarities of the ASIC.

Keywords: Front-end electronics for detector readout; Radiation-hard electronics; VLSI circuits

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Contents

1 Introduction

The PANDA detector (figure 1) is an experimental apparatus that will be installed in the FAIR (Facility for Antiproton and Ion Research in Europe) accelerator facility currently under construction in Darmstadt, Germany. In the detector a beam of antiprotons will interact with a fixed proton or nuclear target inserted through a target pipe that crosses the beam pipe.

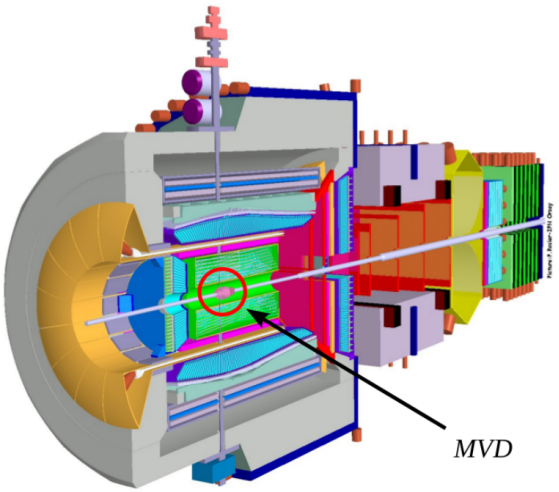

Figure 1. PANDA apparatus.

The Micro Vertex Detector (MVD) [1], shown in figure 2, is its innermost tracking system and is composed of two regions: the barrel region, made of 2 layers of Silicon Pixel Detectors (SPD) and 2 layers of Silicon Strip Detectors (SSD); the forward region, made of 4 SPDs disks and 2 disks of SPDs and SSDs.

The PANDA SSDs have been developed by the University of Giessen (Germany). The SSDs are designed as double-sided detectors, with a breakdown voltage of approximately 200 V and a depletion voltage of 100 V.

The estimated Total Ionizing Dose (TID) that the MVD will experience is up to 100 kGy over 10 years of operation. Such a radiation level does not significantly change the threshold voltage of modern deep-submicron transistors; however, problems can arise from the increase of leakage current and from higher sensitivity to Single Event Upset (SEU).

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The PANDA experiment is characterised by the absence of a hardware trigger at the front-end level, which implies that all data must be sent to the computing nodes in the counting room. To meet the challenges posed and to read out the SSDs, an ASIC called ToASt (Torino Amplifier for silicon Strip detectors) [2] has been developed in Turin by the National Institute of Nuclear Physics (INFN).

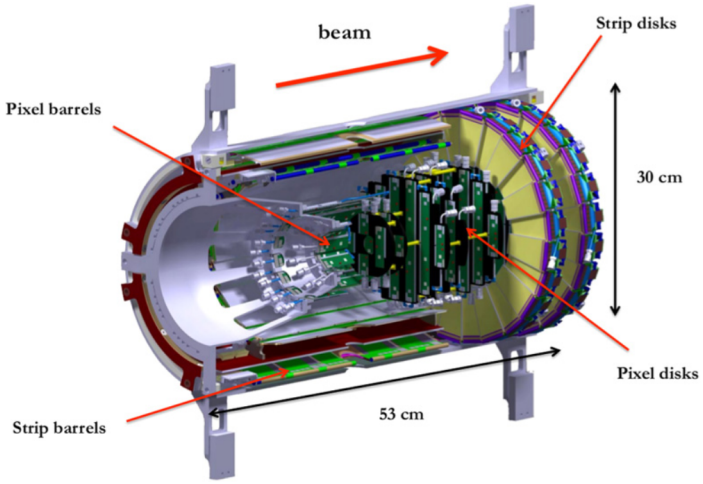

Figure 2. PANDA Micro Vertex Detector.

2 ToASt specifics and architecture

The ToASt ASIC is designed in a commercial 110 nm CMOS technology, with a dimension of $4.5 \times 3.5\,\mathrm{mm}^2$. It has a power consumption of 180 mW and a triplicate logic for SEU protection.

As required by the experiment, the ASIC provides spatial, energy and time information of the particle that crosses the detector. The spatial information is provided by the position of the strip, given by the associated channel number. The energy information is obtained by the charge deposited in the detector, which is measured from the difference between the trailing and the leading edge time stamps, i.e. with the Time-over-Threshold (ToT) method. The Time of Arrival (ToA), given by the rising edge time stamps, provides the timing information. The time is referenced to a global time generated by a 12-bit counter running at the master clock 160 MHz frequency. From this choice results a maximum peak-to-peak of 6.25 ns with a r.m.s. of 1.8 ns, appropriate for the experiment.

The ToASt specifications are summarized on table 1.

The ASIC provides 64 channels, divided into 8 regions with local 16 cells FIFOs. The regions are read out by a single Global Readout Unit, which features a 64 cells FIFO and two 160 Mb/s serial link, to transmit the event data, i.e. channel address, ToA and ToT, packaged in a 32-bit data word. ToASt is equipped with a fully digital interface to avoid the transmission of noise-sensitive analogue signals. The ToASt architecture is depicted in figure 3.

Analog Front-End. The Analog Front-End, depicted in figure 4, is formed by four main blocks: a charge sensitive amplifier with a nominal gain of 5 mV/fC, which can be configured to accept current inputs from either n-type or p-type detector signals; a shaper, with an adjustable peaking time to adapt to the increase of the leakage current in the detector due to the radiation damage; a current buffer which provides the current that will be integrated by the following stage; an integrator

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Table 1. ToASt specifics.

Input capacitance	2 ÷ 17 pF
Max rate per strip	50 kHz
Input charge range	1 ÷ 40 fC
Max noise	1500 e.n.c.
Peaking time	50–100 ns
Channels per chip	64
Channel pitch	66 µm
Reference clock	160 MHz
Charge resolution	8 bits
Time resolution	6.25 ns (pk-pk)
	1.8 ns (r.m.s.)
Output drivers	2 × 160 MS/s
Max output rate	2 × 4.9 Mevents/s
Power consumption	180 mW @ 1.2 V
Die size	3.24 × 4.41 mm^2
Pads position	On two sides only

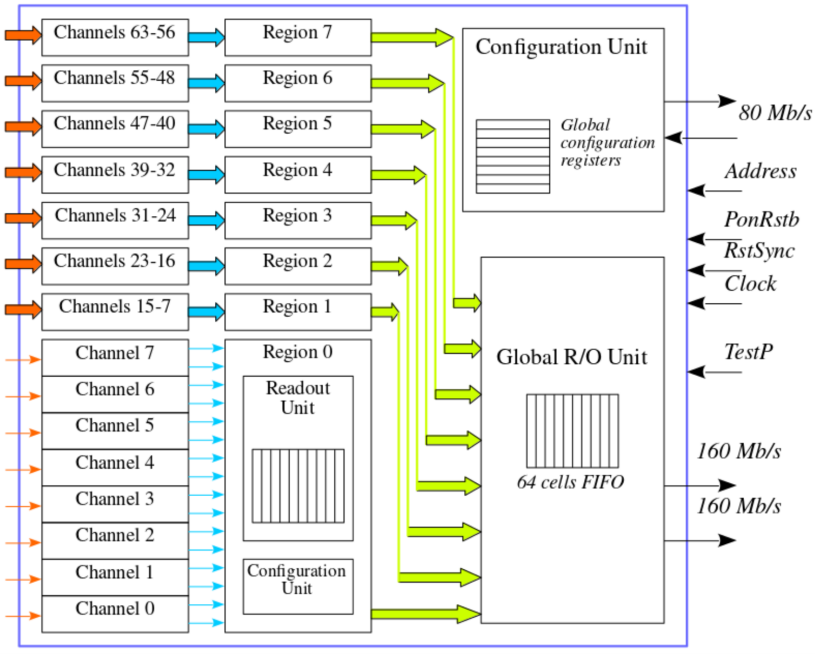

Figure 3. ToASt architecture schematic.

stage, where the feedback capacitor is discharged by a constant current to provide a linear ToT; finally, the output of the ToT stage is connected to two comparators with independent threshold. Owing to the linear discharge of the integrating capacitor, the duration of the comparator outputs is linearly proportional to the input charge.

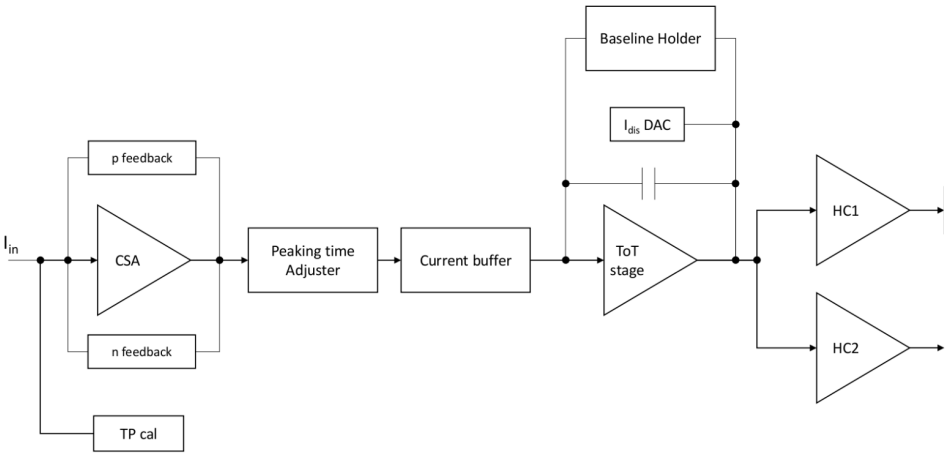

Figure 4. ToASt channel schematic.

By setting different thresholds on the two comparators, the time stamp is stored on the lower threshold (time threshold) and validated with the higher threshold (energy threshold), as shown in figure 5. By setting different thresholds on the two comparators, it is thus possible to reduce the jitter on small signals while keeping a good rejection of dark (noise) signals.

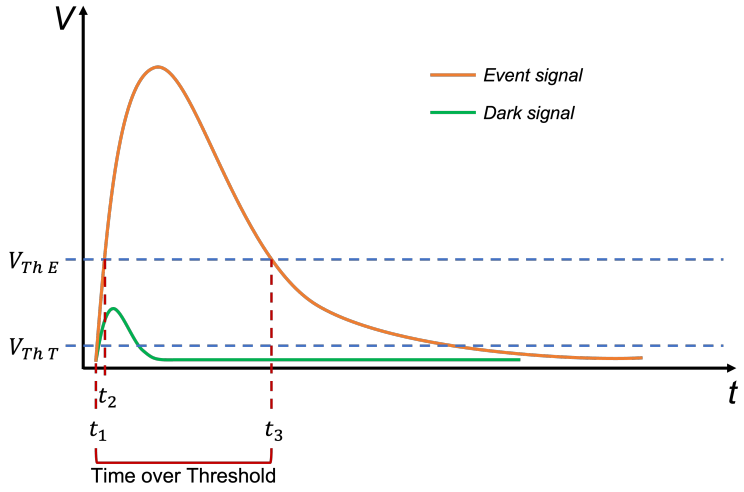

Figure 5. ToT measurement with dual-threshold method.

3 Test results

Calibration. ToT gains and offsets need to be adjusted channel by channel, due to the spread of process parameters. Each channel is equipped with DACs to fine tune the comparator thresholds and the ToT discharge current, thus providing gain and offset equalisation.

Figure 6 shows the measured gain for the 64 channels of a chip for both polarities, before and after calibration, by setting different reference gains. From the test results the gain for both polarities can be set between 50 and 60 ns/fC. By applying the calibration procedure, the gain spread among channels is reduced from 11.7% to 1.5% and the offset from 15.6% to 3.5%, as reported in figure 7.

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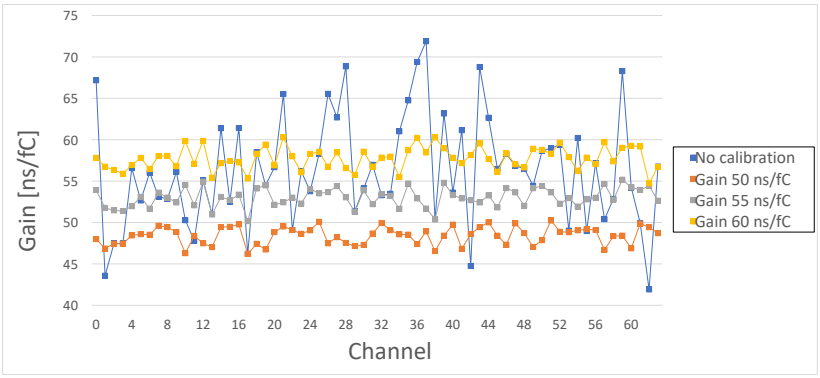
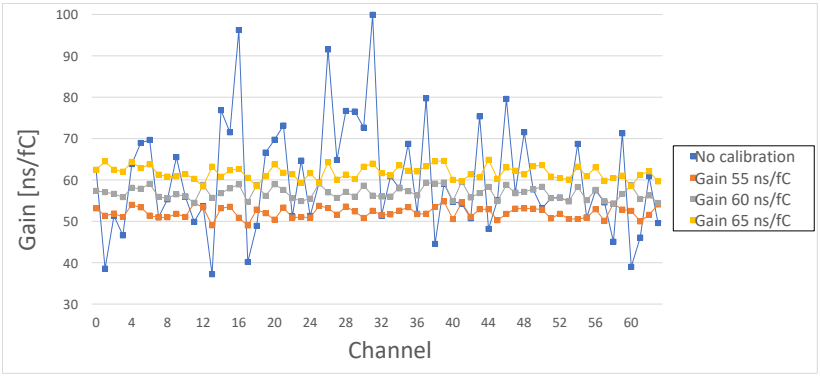
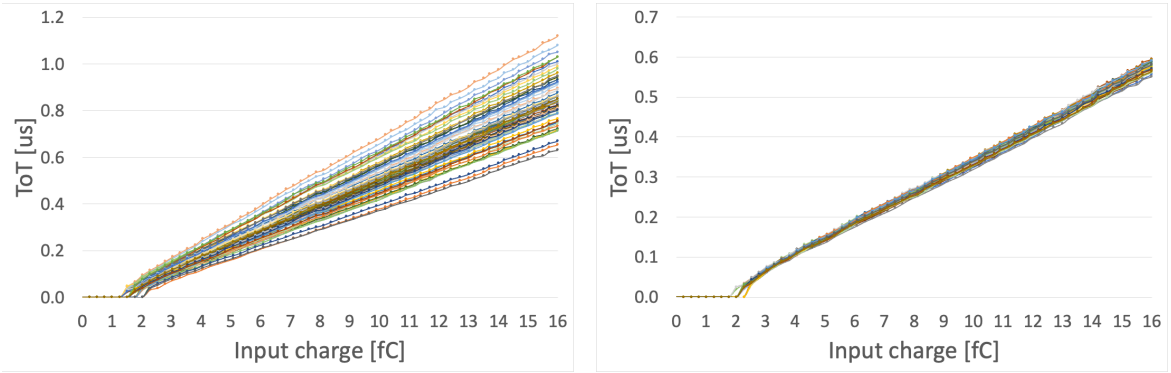


(a)



(b)

Figure 6. Gain calibration: (a) P-type input, (b) N-type input.



(a) (b)

Figure 7. ToT as a function of input charge before (a) and after (b) the calibration procedure.

Noise. Noise measurements were evaluated by scanning the channel's fine-tuning threshold and extracting the S-curve. The measured Equivalent Noise Charge (ENC) was between 100 and 400 electrons on all channels without capacitance connected to the inputs (figure 8). The noise values have been calculated with the error function, assuming a Gaussian noise distribution, and are limited by the resolution of the threshold DAC.

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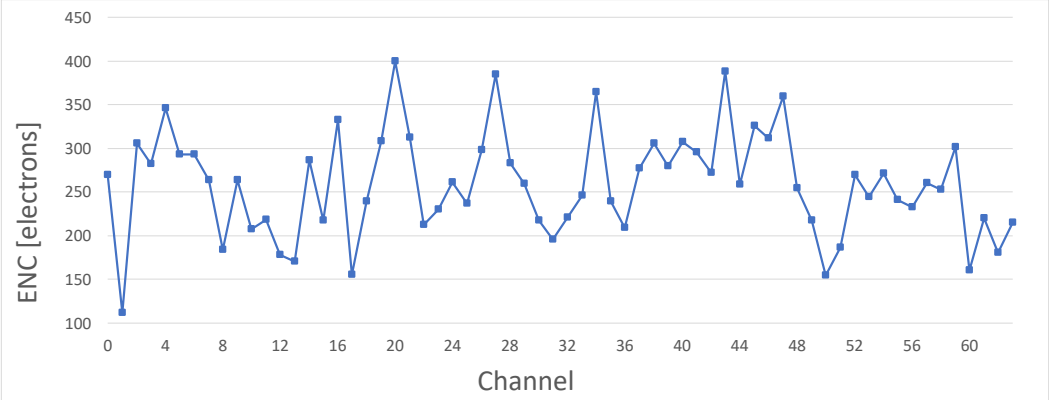
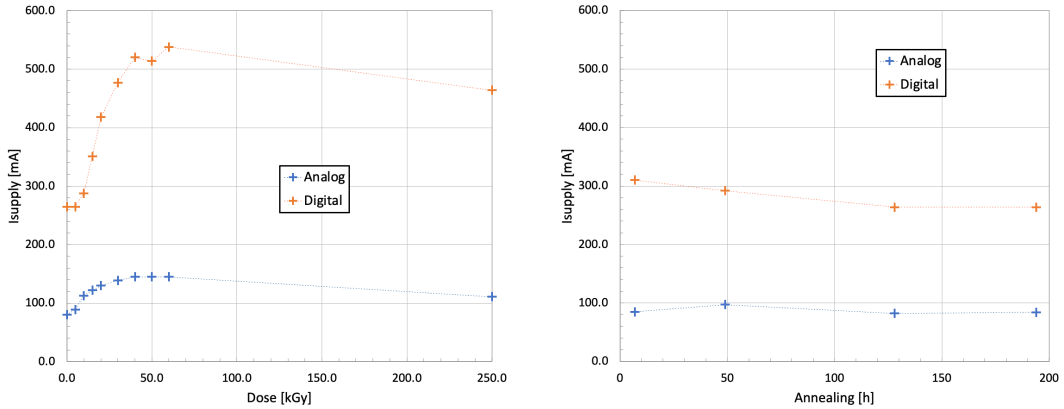


Figure 8. Equivalent Noise Charge per channel.

Total Ionizing Dose. The technology used has been reported to be tolerant to doses up to 50 kGy [3], therefore no special design techniques were adopted to improve TID tolerance.

The ToASt ASIC is expected to work in an environment with moderate radiation up to 20 kGy, so it was also tested for TID to see its tolerance to radiations. This test was performed at INFN in Padua, Italy, and the chip was irradiated up to 250 kGy with a dose rate of 3.5 Gy/s.

The digital logic was still working at 250 kGy; however a significant increase of both analog and digital supply current has been observed during irradiation (figure 9) due to radiation-induced leakage current.



(a) (b)

Figure 9. (a): Supply current as a function of dose; (b): Supply current after annealing.

After 4 kGy the ASIC was not able anymore to process test pulses (figure 10). However, it experienced a partial recovery after 1302 hours annealing at room temperature, and a full recovery after 152 hours annealing at 100 °C.

This finding led to a detailed analysis of the circuit, which showed that this is likely due to some leakage currents in the switch that disables the test pulse itself. As the design error has been identified, it will be corrected in the next version of the ToASt ASIC.

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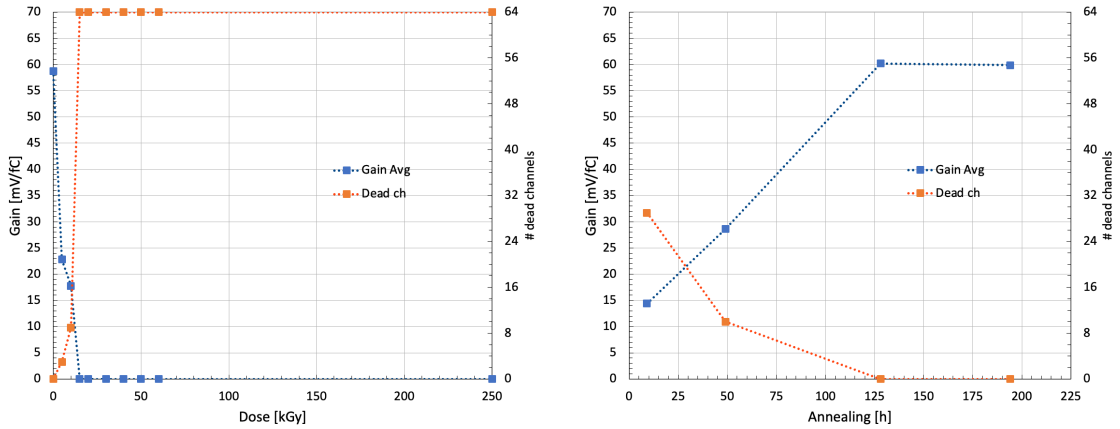

(a) (b)

Figure 10. (a): Gain in function of dose; (b): Gain in function of annealing.

Single Event Upset. The SEU protection of the digital logic was tested [4] at INFN LNL SIRAD facility located in Legnaro, Italy.

The Linear Energy Transfer (LET) of the ions used for the tests ranged from 4.6 to 38.7 MeV cm^2/mg with a fluence of about 5×10^7 ions/cm^2. An estimated cross-section of 3×10^{-15} cm^2, depicted in figure 11, was obtained using the method proposed in [5].

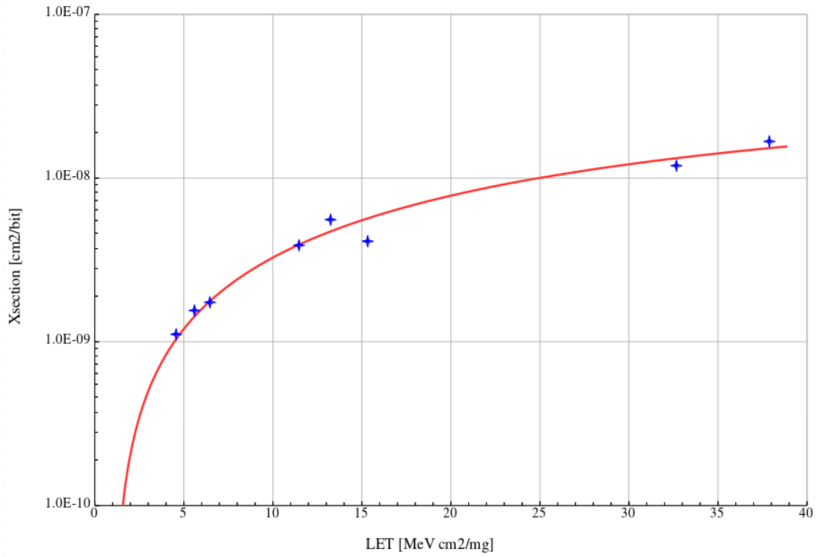

Figure 11. Cross section in function of Linear Energy Transfer.

Only upsets from logic-1 to logic-0 were observed. After verification, a triplication error was identified as the most likely cause of the observed behaviour, and such an error will get corrected in the next version of the chip.

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4 Conclusions

ToASt is a 64-channel ASIC designed in 110 nm CMOS technology for the readout of silicon strip detectors of PANDA Micro Vertex Detector. Each channel provides the Time of Arrival and the deposited energy (via ToT method) of the particles crossing the detector.

Tests showed that ToASt, as expected, has excellent performance in terms of time and energy. The measured noise with no input capacitance corresponds to what expected from the simulations. Noise measurements with the strip detector connected have been carried out and are currently under analysis.

The ASIC performances under irradiation are generally good. However, some issues with the operation of the TID and SEU channels must be fixed in the next version in order to improve the radiation tolerance of the ASIC.

A new version of ToASt with improvements in radiation tolerance is thus under development and will be produced during the next year.

Acknowledgments

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References

[1] PANDA collaboration, *Technical Design Report for the: PANDA Micro Vertex Detector*, arXiv:1207.6581.

[2] G. Mazza et al., *ToASt: A 64 Channels Readout ASIC for Silicon Strip Detectors in 0.11 µm CMOS Technology*, in the proceedings of the *2021 IEEE Nuclear Science Symposium (NSS) and Medical Imaging Conference (MIC) and 28th International Symposium on Room-Temperature Semiconductor Detectors*, Piscataway, NJ, U.S.A. (2021), p. 1–4 [DOI:10.1109/NSS/MIC44867.2021.9875549].

[3] E. Riceputi et al., *Total ionizing dose effects on CMOS devices in a 110 nm technology*, in the proceedings of the *2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Taormina, Italy (2017), p. 241–244 [DOI:10.1109/prime.2017.7974152].

[4] PANDA MVD collaboration, *A 64 channels ASIC for the readout of the silicon strip detectors of the PANDA micro-vertex detector*, 2023 *JINST* **18** C01020.

[5] M. Huhtinen and F. Faccio, *Computational method to estimate single event upset rates in an accelerator environment*, *Nucl. Instrum. Meth. A* **450** (2000) 155.

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