Summary

Digital electronics has led the development of finer silicon technology nodes improving performance, area, cost and computation efficiency in integrated circuits. The reduced dynamic range, degradation of the intrinsic transistor gain, physical limitations imposed by matching, have slowed down analogous advantages in analog and mixed-signals blocks, leading to increased design time and effort.

In the context of Internet of Things (IoT) and Biosensing applications this gap becomes more evident, since tiny ubiquitous nodes are required to sense and interact with the environment and the human body, power and area are heavily constrained, while design time and easy architecture reconfigurability and portability are a must to contain cost and being non-invasive.

Such applications usually require analog frontends with resolutions up to 12-14bits and moderate sample rates (up to MS/s), while required to operate over a wide, possibly unregulated, supply and achieving competitive energy and area figures of merit (FOM). This is the motivation to explore the design of novel digital-to-analog and analog-to-digital conversion techniques exploiting digitally intensive architecture to intrinsically benefit from scaled technology nodes and reduce design effort.

The Relaxation Digital-to-Analog Converter (ReDAC) has been extensively investigated in this thesis as a compact solution in IoT interfaces, starting from an analytical model of its operation, energy consumption, and intrinsic advantages with respect to known topologies. Integrated architectures featuring different calibration strategies based on clock frequency tuning have been developed in 40nm and 180nm CMOS technology and verified by post-layout simulations. Two ReDAC FPGA-based prototypes have been presented and a strategy to suppress parasitics-related nonlinearities has been studied and effectively demonstrated by measurements. A digital radix-based calibration strategy has been developed as a convenient alternative to the clock-tuning based calibrations, in a 180nm

simulated design.

A single-ended and a differential-output ReDAC implementation have been fabricated in a 180nm prototype featuring calibration and on-chip direct digital synthesis. The silicon verification validates the expected performance in terms of area and power dissipation of the ReDAC topology, proving to be a competitive solution compared to the state of the art in terms of area and power FOMs.

In the context of Biosensing interfaces, a Direct Digital Sensing Potentiostat (DDSP) has been presented aiming at non-enzymatic detection of glucose in Body-Dust particles. It replaces the conventional opamp-based architecture exploiting the concept of the digital-based operational transconductance amplifier to achieve order-of-magnitudes smaller area and power with respect to the state of the art while achieving good linearity in glucose detection. The design is verified based on post layout simulations developing an electrical model for the electrodes-solution interface.