Analysis and Conceptualization of a 400 V 100 kVA Full-GaN Double Bridge Inverter for Next-Generation Electric Vehicle Drives

# Analysis and Conceptualization of a 400 V 100 kVA Full-GaN Double Bridge Inverter for Next-Generation Electric Vehicle Drives

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***Abstract*—The rising demand for electric vehicles (EVs) is pushing the industry to develop cheaper, lighter and more efficient powertrains. In particular, the drive inverter represents a crucial component of an EV drive train, being responsible for the DC/AC power conversion between the battery and the electrical machine. As a result, advanced converter topologies and modern wide bandgap (WBG) semiconductor devices are being actively evaluated by both industry and academia, aiming to improve the performance of next-generation EV drive inverters. In this context, the double bridge inverter (DBI) represents a promising candidate for 400 V EV powertrains, allowing to increase the machine phase voltage and thus to reduce the inverter phase current for a given power level. Although a three-phase machine with an open-end winding configuration is required, the DBI unlocks significant benefits at the converter level, especially if state-of-the-art 600/650 V GaN high electron mobility transistors (HEMTs) are employed. Therefore, this paper proposes the analysis and the conceptualization of a full-GaN 100 kVA 400 V DBI for next-generation EV drives. A complete theoretical assessment of the system active and passive component stresses (i.e., semiconductor losses, machine phase flux ripple, DC-link capacitor RMS current and charge ripple) is performed, providing the basis for the converter sizing. Additionally, a DBI design concept is developed, achieving an estimated 99.7 % peak semiconductor efficiency (99.2 % at rated current) and a 192 kVA/dm$^3$ power density.**

***Index Terms*—double bridge inverter; traction inverter; wide bandgap (WBG) devices; gallium nitride (GaN); high electron mobility transistors (HEMTs); electric vehicles (EVs)**

## I. Introduction

The drive inverter represents a central component of an EV drive train, since it performs the DC/AC power conversion between the battery and the electrical machine (cf. Fig. 1). As a consequence, a great effort is currently being spent to improve the performance of this power electronic converter [1], [2], which requires high power density, high efficiency over a wide load range [3], high temperature operation capability, and high switching frequency (i.e., to provide sufficient control margin and reduce time-harmonic losses in low-inductance, high-speed machines with several pole pairs typically adopted in automotive [3]–[6]).

Two key enabling technologies may play a significant role in addressing these challenging requirements: novel drive inverter topologies (i.e., different from the widely adopted two-level voltage-source inverter) [7]–[9] and modern wide bandgap (WBG) semiconductor devices [9]–[11]. Whereas three-level inverter topologies are excellent candidates for upcoming 800 V EV powertrains [7], [12], [13], as they simultaneously reduce the stress on the supplied machine [6] and enable the adoption of semiconductor devices with lower blocking voltage (i.e., featuring higher conduction and switching performance [14]), also drive systems based on the widespread 400 V battery architecture can benefit from advanced converter topologies.

A particularly promising candidate for 400 V powertrains is the double bridge inverter (DBI), which consists of two separate three-phase two-level inverters connected as in Fig. 2 [15], [16]. Even though the electrical machine must feature an open-end winding configuration, the DBI allows to increase the machine phase voltage with respect to a two-level inverter (i.e., either by a factor of 2 or $\sqrt{3} \approx 1.73$, depending on the two-level inverter modulation strategy), thus reducing the phase current value for a given power level. The lower phase current of the DBI unlocks significant benefits, reducing the RMS current stress and/or charge ripple on the DC-link capacitor (i.e., requiring a lower capacitance and thus reducing the inverter size), and allowing for the adoption of semiconductor devices with reduced current rating and enhanced switching properties (i.e., enabling higher switching frequency operation). A further performance enhancement can be obtained by employing modern 600/650 V silicon carbide (SiC) and gallium nitride (GaN) semiconductor devices, which significantly outperform traditional silicon (Si) devices of the same voltage class [10], [11]. Although 600/650 V GaN high electron mobility transistors (HEMTs) are still not well established in the automotive industry, as opposed to SiC MOSFETs (i.e., which are already employed in several EV drive inverters), they promise higher theoretical performance and thus represent excellent candidates for next-generation EVs.

While several papers have already been published on GaN-based high-voltage ($> 100$ V) inverters, they either target a low power rating (i.e., $\leq 10$ kW) [17]–[21] or exploit GaN devices in a multi-level configuration [18]–[23], trading higher performance for increased complexity. To the best of the authors' knowledge, no GaN-based 400 V $\geq 50$ kW three-phase inverter design has been reported in literature.

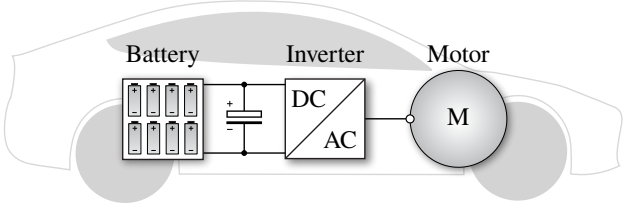


Fig. 1. Simplified schematic overview of an electric vehicle (EV) drive train, including the battery, the drive inverter and the electric motor.

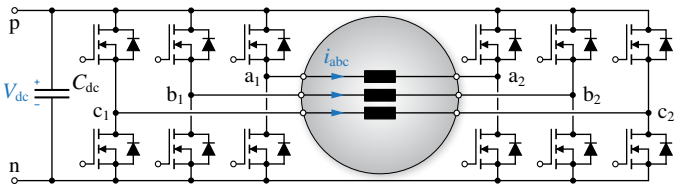


Fig. 2. Schematic of the considered double bridge inverter (DBI) drive system.

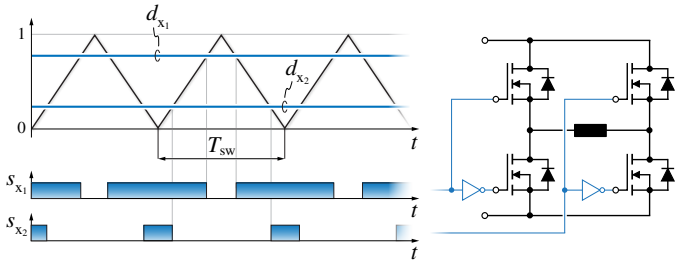


Fig. 3. Generation of the bridge-leg PWM switch signals $s_{x_1}$ and $s_{x_2}$.

Therefore, the main goal of this paper is to provide a detailed analysis and conceptualization of a GaN-based high-performance high-power DBI for next-generation 400 V EV drives. In particular, the main contributions of this work are:

- the comprehensive analysis of the stresses applied to the semiconductor devices (i.e., conduction and switching losses), the electrical machine (i.e., differential-mode and common-mode phase flux ripples) and the DC-link capacitor (i.e., RMS current and charge ripple) for all operating conditions;
- the conceptualization of a high-efficiency, high-power density 100 kVA 400 V full-GaN DBI employing state-of-the art semiconductor devices and ceramic capacitors, including the design and/or sizing of all converter components.

This paper is structured as follows. In Section II the operational basics of the DBI are described, including the AC-side voltage formation and the DC-side current generation processes. In Section III the drive system active and passive component stresses are analyzed in detail, providing the basis for the converter design. In Section IV a DBI design concept is proposed and its perfomance is assessed in simulation environment. Finally, Section V summarizes and concludes this work.

## II. Basics of Operation

The equivalent circuit schematic of the considered 400 V three-phase double bridge inverter (DBI) drive system is illustrated in Fig. 2. The electrical machine features an open-end winding configuration and each phase is connected between two independently controlled two-level inverter bridge-legs (i.e., adopting 600/650 V active switches).

The DBI can synthesize an average sinusoidal voltage across the machine phases in several ways, namely providing different modulation references to the two three-phase inverters. In the present work, two modulation strategies are selected and compared, both assuming synchronized and in-phase modulation carriers. The first modulation strategy is referred to as unipolar pulse-width modulation (PWM) [15]. This strategy continuously modulates both three-phase inverters according to opposite sinusoidal references, achieving a frequency doubling effect at the machine phase terminals (i.e., the first harmonic frequency of the machine phase flux ripple is $2f_{\mathrm{sw}}$). The second modulation strategy, referred to as unfolder PWM [15], differentiates the two inverter units by having one three-phase unit continuously modulated at $f_{\mathrm{sw}}$ and the other unit working in six-step operation at the machine fundamental frequency $f$ (i.e., providing the unfolding feature). Notably, the switching losses in the unfolding inverter can typically be neglected (i.e., $f \ll f_{\mathrm{sw}}$). Therefore, unfolder PWM allows to halve the total DBI switching losses at the expense of losing the frequency doubling feature at the machine phase terminals. It is worth noting that unipolar PWM and unfolder PWM both ensure an equal loss distribution among semiconductor devices of the same inverter unit. For instance, another modulation strategy is reported in [15], alternating the unfolding role between the two inverters. Nevertheless, even though this strategy allows to equally distribute the semiconductor losses between the two inverters, it does not ensure an equal loss sharing between devices of the same bridge-leg (i.e., leading to possible thermal issues), therefore it is not considered herein.

The bridge-leg PWM switch signals $s_{\mathrm{x}_1}$ and $s_{\mathrm{x}_2}$ ($\mathrm{x} = \mathrm{a}, \mathrm{b}, \mathrm{c}$) are generated from the comparison between the bridge-leg duty cycles and the modulation carrier, as illustrated in Fig. 3. The DBI modulation references are defined as

$$\begin{cases} m_{\mathrm{a}} = \dfrac{M}{2}\cos(\vartheta) \\ m_{\mathrm{b}} = \dfrac{M}{2}\cos(\vartheta - \frac{2}{3}\pi) \\ m_{\mathrm{c}} = \dfrac{M}{2}\cos(\vartheta - \frac{4}{3}\pi) \end{cases}, \tag{1}$$

where $M = 2V/V_{\mathrm{dc}}$ is the inverter modulation index (i.e., $0 \leq M \leq 2$), and the bridge-leg duty cycles are directly obtained from (1), as

$$d_{\mathrm{x}_1} = \frac{1 + m_{\mathrm{x}}}{2}, \quad d_{\mathrm{x}_2} = \frac{1 - m_{\mathrm{x}}}{2} \tag{2}$$

for unipolar PWM, and

$$d_{\mathrm{x}_1} = \begin{cases} m_{\mathrm{x}} & m_{\mathrm{x}} \geq 0 \\ 1 + m_{\mathrm{x}} & m_{\mathrm{x}} < 0 \end{cases} \qquad d_{\mathrm{x}_2} = \begin{cases} 0 & m_{\mathrm{x}} \geq 0 \\ 1 & m_{\mathrm{x}} < 0 \end{cases} \tag{3}$$

for unfolder PWM, with $\mathrm{x} = \mathrm{a}, \mathrm{b}, \mathrm{c}$.

### A. AC-Side Voltage Formation

The AC terminal of each bridge-leg may be actively connected either to the positive (p) or negative (n) DC-link rails. Therefore, the voltage applied to the machine phases can assume three different values:

- $v_{\mathrm{x}_1\mathrm{x}_2} = +V_{\mathrm{dc}}$, with $s_{\mathrm{x}_1} = 1$ and $s_{\mathrm{x}_2} = 0$,
- $v_{\mathrm{x}_1\mathrm{x}_2} = -V_{\mathrm{dc}}$, with $s_{\mathrm{x}_1} = 0$ and $s_{\mathrm{x}_2} = 1$,
- $v_{\mathrm{x}_1\mathrm{x}_2} = 0$, with $s_{\mathrm{x}_1} = s_{\mathrm{x}_2} = 1$ or $s_{\mathrm{x}_1} = s_{\mathrm{x}_2} = 0$,

where $s_{\mathrm{x}_1}$ and $s_{\mathrm{x}_2}$ are the switching signals of the two bridge-legs connected across phase x (1 if high-side ON, 0 if low-side ON, cf. Fig. 3). Therefore, the phase voltage can be expressed as

$$v_{\mathrm{x}_1\mathrm{x}_2} = (s_{\mathrm{x}_1} - s_{\mathrm{x}_2})\, V_{\mathrm{dc}} \qquad \mathrm{x} = \mathrm{a}, \mathrm{b}, \mathrm{c}. \tag{4}$$

Since the machine features an open-end winding configuration, its phases are subject to both the differential-mode (DM) and the common-mode (CM) components of the phase voltage, as opposed to conventional three-phase machines with an open star point (i.e., only subject to the DM voltage). Analyzing the two three-phase inverters independently, the zero-sequence (i.e., common-mode) voltage of each unit is obtained by averaging the three bridge-leg voltage contributions, as

$$v_{\mathrm{o_1}} = \frac{v_{\mathrm{a_1n}} + v_{\mathrm{b_1n}} + v_{\mathrm{c_1n}}}{3} = v_{\mathrm{o_1,LF}} + v_{\mathrm{o_1,HF}}, \tag{5}$$

$$v_{\mathrm{o_2}} = \frac{v_{\mathrm{a_2n}} + v_{\mathrm{b_2n}} + v_{\mathrm{c_2n}}}{3} = v_{\mathrm{o_2,LF}} + v_{\mathrm{o_2,HF}}, \tag{6}$$

and the differential-mode voltages are found by subtracting the zero-sequence component from the bridge-leg voltages, as

$$v_{\mathrm{x_1}} = v_{\mathrm{x_1n}} - v_{\mathrm{o_1}} = v_{\mathrm{x_1,LF}} + v_{\mathrm{x_1,HF}} \qquad \mathrm{x} = \mathrm{a,b,c}, \tag{7}$$

$$v_{\mathrm{x_2}} = v_{\mathrm{x_2n}} - v_{\mathrm{o_2}} = v_{\mathrm{x_2,LF}} + v_{\mathrm{x_2,HF}} \qquad \mathrm{x} = \mathrm{a,b,c}, \tag{8}$$

where subscripts LF and HF indicate the low-frequency (i.e., moving average) and high-frequency (i.e., switching frequency harmonics) voltage components, respectively. Therefore, the AC-side voltage formation process of the DBI can be represented with the equivalent circuit illustrated in Fig. 4(a). The low-frequency components of the DM voltage $v_{\mathrm{x_1,LF}}$, $v_{\mathrm{x_2,LF}}$ are regulated by means of the duty cycles in (2)–(3) to control the converter phase currents $i_{\mathrm{a}}$, $i_{\mathrm{b}}$, $i_{\mathrm{c}}$. The low-frequency components of the CM voltage $v_{\mathrm{o_1,LF}}$, $v_{\mathrm{o_2,LF}}$ are equal (i.e., $v_{\mathrm{o_1,LF}} = v_{\mathrm{o_2,LF}}$), ensuring that no low-frequency CM voltage is applied across the machine phases. Finally, the high-frequency components of both DM and CM voltages

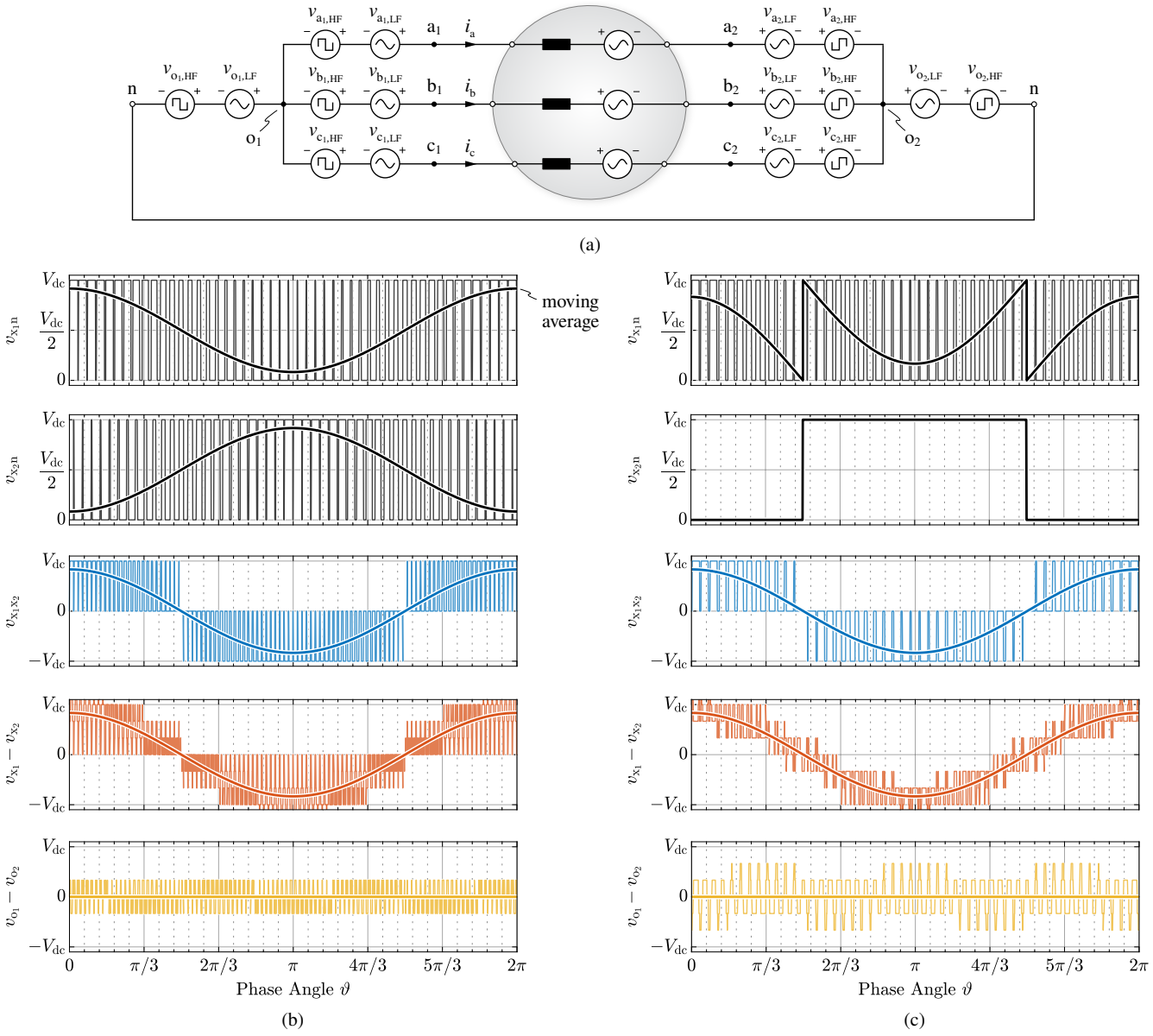


Fig. 4. (a) equivalent circuit schematic of the DBI AC-side voltage formation process. Qualitative overview of the inverter bridge-leg voltages $v_{\mathrm{x_1n}}$, $v_{\mathrm{x_2n}}$, phase voltage $v_{\mathrm{x_1x_2}}$, differential-mode (DM) voltage $v_{\mathrm{x_1}} - v_{\mathrm{x_2}}$ and common-mode (CM) voltage $v_{\mathrm{o_1}} - v_{\mathrm{o_2}}$ adopting (b) unipolar PWM and (c) unfolder PWM, assuming $M = 5/3$. The low-frequency (i.e., moving-average) component of each waveform is also shown for clarity.

$v_{x_1,HF}$, $v_{x_2,HF}$, $v_{o_1,HF}$, $v_{o_2,HF}$ define the stress applied to the machine phases in terms of flux and current ripples, which determine the machine PWM-induced losses [6].

A qualitative overview of the DBI bridge-leg voltages $v_{x_1 n}$, $v_{x_2 n}$, phase voltage $v_{x_1 x_2}$, DM voltage $v_{x_1} - v_{x_2}$ and CM voltage $v_{o_1} - v_{o_2}$ is reported in Fig. 4(a), (b) for unipolar PWM and unfolder PWM, respectively.

### B. DC-Side Current Generation

The DC-link current $i_{dc}$ is defined by the combination of the instantaneous phase current values $i_a$, $i_b$, $i_c$ and the bridge-leg switching signals $s_{x_1}$, $s_{x_2}$, as

$$\begin{aligned} i_{dc} &= i_{dc,a_1} + i_{dc,b_1} + i_{dc,c_1} + i_{dc,a_2} + i_{dc,b_2} + i_{dc,c_2} \\ &= (s_{a_1} + s_{a_2})\, i_a + (s_{b_1} + s_{b_2})\, i_b + (s_{c_1} + s_{c_2})\, i_c. \end{aligned} \quad (9)$$

Assuming sinusoidal phase currents with peak value $I$, i.e.,

$$\begin{cases} i_a = I\cos(\vartheta) \\ i_b = I\cos(\vartheta - \frac{2}{3}\pi - \varphi) \\ i_c = I\cos(\vartheta - \frac{4}{3}\pi - \varphi) \end{cases}, \quad (10)$$

the DC-link current average can be calculated as in [24], obtaining

$$I_{dc,avg} = \frac{3}{4} M I \cos\varphi. \quad (11)$$

The current flowing into the DC-link capacitor is finally obtained by difference, as

$$i_{C_{dc}} = i_{dc} - I_{dc,avg}, \quad (12)$$

leading to the equivalent circuit reported in Fig. 5(a). The instantaneous DC-link current waveforms are qualitatively illustrated in Fig. 5(b), (c) for unipolar PWM and unfolder PWM, respectively.

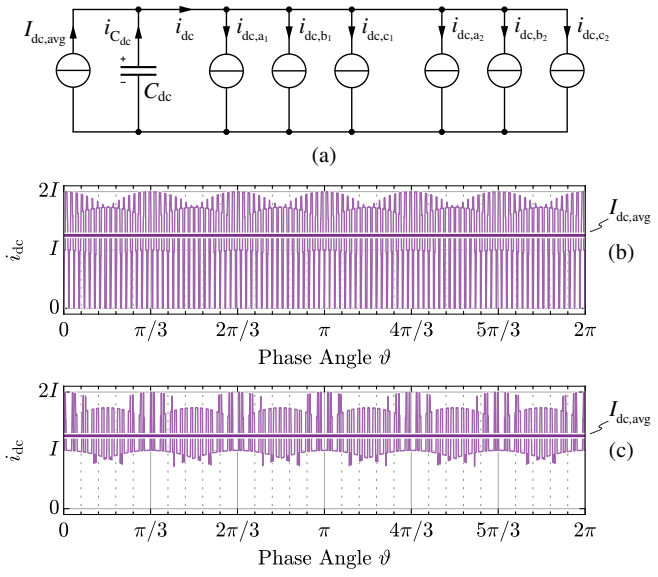


Fig. 5. (a) equivalent circuit schematic of the DBI DC-side current generation process. Qualitative overview of the DBI DC-link current $i_{dc}$ waveforms adopting (b) unipolar PWM and (c) unfolder PWM, assuming $M = 5/3$. The average DC-link current $I_{dc,avg}$ is indicated.

## III. Component Stress Analysis

In this section, the stresses applied to the semicondutor devices, the machine phases and the DC-link capacitor are analyzed, providing useful analytical expressions for the converter design in Section IV.

### A. Semiconductor Losses

Assuming the adoption of unipolar semiconductor devices (e.g., MOSFETs, HEMTs), the total conduction losses of the DBI can be expressed as [15]:

$$P_{cond,tot} = 3\, R_{ds,on}\, I^2, \quad (13)$$

where $R_{ds,on}$ is the semiconductor on-state resistance.

Additionally, since fast-switching devices are typically characterized by a linear dependence of the switching energies $E_{on}$, $E_{off}$ with respect to the switched current $i_{sw}$ (i.e., $E_{on} \approx k_{0,on} + k_{1,on}\, i_{sw}$, $E_{off} \approx k_{0,off} + k_{1,off}\, i_{sw}$ for $i_{sw} \geq 0$, and $E_{on} = E_{off} \approx 0$ for $i_{sw} < 0$) [7], the average switching losses generated by the DBI can be expressed as [15]

$$P_{sw,tot} = \alpha f_{sw} \left[ (k_{0,on} + k_{0,off}) + \frac{2}{\pi} I\, (k_{1,on} + k_{1,off}) \right], \quad (14)$$

where $\alpha = 6$ for unipolar PWM and $\alpha = 3$ for unfolder PWM (i.e., neglecting the losses related to switching transitions at fundamental frequency of the second inverter unit, being $f \ll f_{sw}$).

### B. Machine Phase Flux Ripple

The high-frequency voltage-time area applied to the machine phases generates a flux linkage ripple $\Delta\psi$ directly related to the magnetic flux density swing (and losses) within the machine stator/rotor cores and/or magnets. Furthermore, $\Delta\psi$ translates into a current ripple inversely proportional to the machine inductance, which generates additional winding losses. Therefore, $\Delta\psi$ is directly responsible for all PWM-induced high-frequency losses in the driven machine [6] and therefore represents a useful and comprehensive machine stress indicator.

Since a DBI drive system features an electrical machine with open-end windings (cf. Fig. 2), both DM and CM voltages fall across the machine phases (cf. Fig. 4). In particular, while the DM voltage sees the relatively large differential-mode phase mutual inductance $L_{DM}$, the CM voltage is applied to the much lower common-mode inductance $L_{CM}$ (i.e., being typically determined by the small leakage flux). Therefore, due to the different DM and CM flux paths within the machine (i.e., affecting core losses differently) and since $L_{DM} \gg L_{CM}$ (i.e., leading to very different current ripples and winding losses), the machine phase DM and CM flux ripple components

$$\Delta\psi_{DM,x} = \int_0^t (v_{x_1,HF} - v_{x_2,HF})\, dt \qquad x = a, b, c \quad (15)$$

$$\Delta\psi_{CM} = \int_0^t (v_{o_1,HF} - v_{o_2,HF})\, dt \quad (16)$$

must be analyzed independently. To take into account the flux ripple amplitude along the complete fundamental period,

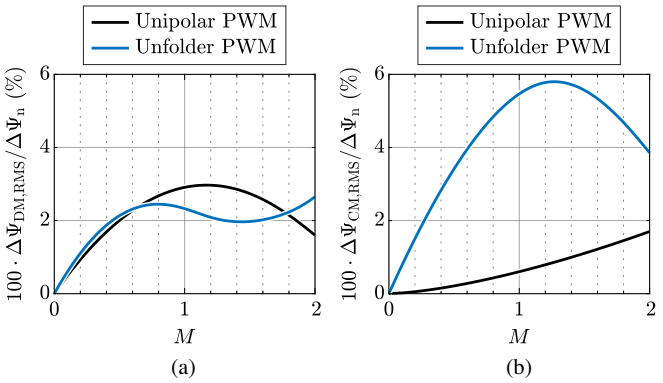


Fig. 6. Normalized DBI machine phase RMS flux ripple components as function of the inverter modulation index $M$ for unipolar PWM and unfolder PWM: (a) differential-mode (DM) flux ripple $\Delta\Psi_{\mathrm{DM,RMS}}$, (b) common-mode (CM) flux ripple $\Delta\Psi_{\mathrm{CM,RMS}}$. The results are normalized by $\Delta\Psi_{\mathrm{n}} = V_{\mathrm{dc}}/f_{\mathrm{sw}}$.

the global DM and CM RMS flux ripples are considered as performance indices, defined as [25]

$$\Delta\Psi^2_{\mathrm{DM,RMS}} = \frac{6}{T}\int_0^{\frac{T}{6}} \frac{\Delta\psi^2_{\mathrm{DM,a}} + \Delta\psi^2_{\mathrm{DM,b}} + \Delta\psi^2_{\mathrm{DM,c}}}{3}\,\mathrm{d}t \quad (17)$$

$$\Delta\Psi^2_{\mathrm{CM,RMS}} = \frac{6}{T}\int_0^{\frac{T}{6}} \Delta\psi^2_{\mathrm{CM}}\,\mathrm{d}t \quad (18)$$

Introducing a flux ripple normalization factor $\Delta\Psi_{\mathrm{n}} = V_{\mathrm{dc}}/f_{\mathrm{sw}}$, the following analytical expressions are derived, respectively

$$\frac{\Delta\Psi^2_{\mathrm{DM,RMS}}}{\Delta\Psi^2_{\mathrm{n}}} = \frac{M^2}{384} - \frac{M^3}{576}\left(\frac{\sqrt{3}}{\pi} + \frac{7}{3\pi}\right) + \frac{M^4}{2048} \quad (19)$$

$$\frac{\Delta\Psi^2_{\mathrm{CM,RMS}}}{\Delta\Psi^2_{\mathrm{n}}} = \frac{M^3}{576}\left(\frac{\sqrt{3}}{\pi} - \frac{5}{3\pi}\right) \quad (20)$$

for unipolar PWM, and

$$\frac{\Delta\Psi^2_{\mathrm{DM,RMS}}}{\Delta\Psi^2_{\mathrm{n}}} = \frac{M^2}{576}\left(4 - \frac{3\sqrt{3}}{\pi}\right) - \frac{M^3}{576}\left(\frac{4\sqrt{3}}{\pi} + \frac{3}{\pi}\right) + \frac{M^4}{512} + K_\Psi \quad (21)$$

$$\frac{\Delta\Psi^2_{\mathrm{CM,RMS}}}{\Delta\Psi^2_{\mathrm{n}}} = \frac{M^2}{576}\left(2 + \frac{3\sqrt{3}}{\pi}\right) + \frac{M^3}{576}\left(\frac{4\sqrt{3}}{\pi} - \frac{13}{\pi}\right) - K_\Psi \quad (22)$$

for unfolder PWM, where $K_\Psi = 0$ for $M \le 2/\sqrt{3}$ and

$$K_\Psi = \frac{1}{18\pi}\mathrm{acos}\left(\frac{2}{\sqrt{3}M}\right) - \frac{11}{216\pi}\sqrt{3M^2-4} + \frac{M^2}{576}\left[\frac{36}{\pi}\mathrm{acos}\left(\frac{2}{\sqrt{3}M}\right) - \frac{8}{\pi}\sqrt{3M^2-4}\right] \quad (23)$$

for $M > 2/\sqrt{3}$. The results of the analysis are illustrated in Fig. 6, where $\Delta\Psi_{\mathrm{DM,RMS}}$ and $\Delta\Psi_{\mathrm{CM,RMS}}$ are reported in normalized form as functions of the DBI modulation index $M = 2V/V_{\mathrm{dc}}$ for both unipolar PWM and unfolder PWM. It is observed that, while the two modulation strategies show similar values of DM RMS flux ripple, they yield very different CM flux ripple stresses. In particular, unfolder PWM leads to increased common-mode PWM-induced losses over the complete operating range.

### C. DC-Link Capacitor RMS Current and Charge Ripple

The DC-link capacitor sizing/design is both affected by the RMS current stress $I_{\mathrm{C_{dc},RMS}}$ and the peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{dc,pp}}}$ (i.e., directly proportional to the DC-link peak-to-peak voltage ripple and thus to the minimum required capacitance). Disregarding the AC-side switching frequency current ripple, both stresses can be analytically calculated.

The RMS current flowing into the DC-link capacitor can be calculated by difference, as

$$I^2_{\mathrm{C_{dc},RMS}} = I^2_{\mathrm{dc,RMS}} - I^2_{\mathrm{dc,avg}}, \quad (24)$$

where $I^2_{\mathrm{dc,RMS}} = {}^6\!/_T \int_0^{T/6} i^2_{\mathrm{dc}}\,\mathrm{d}t$ and $I_{\mathrm{dc,avg}}$ is defined in (11). Expanding and simplifying (24), the following analytical expressions are derived, respectively

$$I_{\mathrm{C_{dc},RMS}} = I\sqrt{M\left[\frac{\sqrt{3}-1}{4\pi} + \cos^2\varphi\left(\frac{\sqrt{3}+2}{\pi} - \frac{9}{16}M\right)\right]} \quad (25)$$

for unipolar PWM, and

$$I_{\mathrm{C_{dc},RMS}} = I\sqrt{M\left[\frac{\sqrt{3}}{4\pi} + \cos^2\varphi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\right] + K_{\mathrm{I}}} \quad (26)$$

for unfolder PWM, where $K_{\mathrm{I}} = 0$ for $M \le 2/\sqrt{3}$ and

$$K_{\mathrm{I}} = \frac{\sqrt{3}}{8\pi}M\sin\left[2\varphi + 3\mathrm{acos}\left(\frac{2}{\sqrt{3}M}\right)\right] + \frac{1}{M^2}\left[\sin 2\varphi\,\frac{9M^2-16}{12\pi} + \cos 2\varphi\,\sqrt{3M^2-4}\,\frac{9M^2-16}{8\pi}\right] + \frac{3}{2\pi}\sqrt{3M^2-4} - \frac{3}{\pi}\mathrm{acos}\left(\frac{2}{\sqrt{3}M}\right) \quad (27)$$

for $M > 2/\sqrt{3}$. Notably, unfolder PWM yields the same RMS current stress as in the two-level inverter case (i.e., for $M \le 2/\sqrt{3}$) [24]. The two $I_{\mathrm{C_{dc},RMS}}$ expressions are illustrated in normalized form (i.e., divided by the peak phase current $I$) in Fig. 7 as functions of $M$ and $\varphi$. The worst-case value of (25)

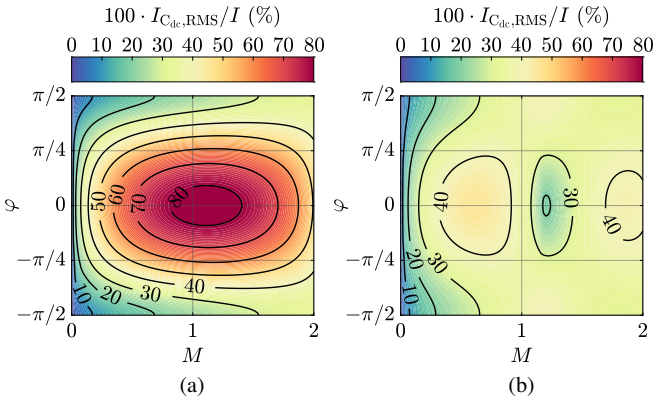


Fig. 7. Normalized DBI DC-link capacitor RMS current $I_{\mathrm{C_{dc},RMS}}$ as function of the inverter modulation index $M$ and the load power factor angle $\varphi$ for (a) unipolar PWM and (b) unfolder PWM. The normalization factor is the peak phase current $I$.

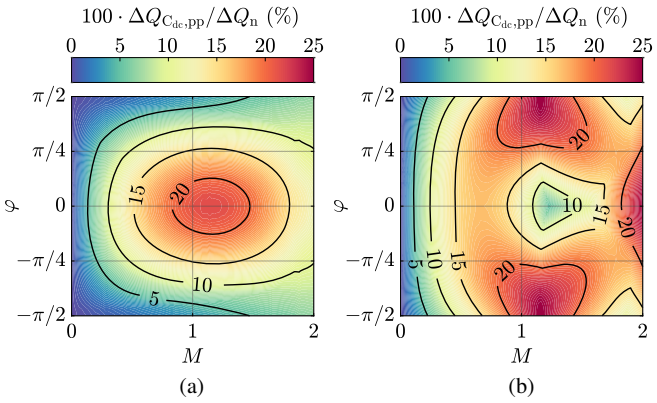


Fig. 8. Normalized DBI DC-link capacitor peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{dc},pp}}$ as function of the inverter modulation index $M$ and the load power factor angle $\varphi$ for (a) unipolar PWM and (b) unfolder PWM. The normalization factor is $\Delta Q_{\mathrm{n}} = I/f_{\mathrm{sw}}$.

(unipolar PWM) is found for $\varphi = 0$ and $M = {}^{(10\sqrt{3}+14)}/_{9\pi}$, as

$$I_{\mathrm{C_{dc},RMS,max}} = \frac{5\sqrt{3}+7}{6\pi}\, I \approx 0.83\, I, \tag{28}$$

whereas the worst-case value of (26) (unfolder PWM) is found for $\varphi = 0$ and $M = {}^{10\sqrt{3}}/_{9\pi}$, as

$$I_{\mathrm{C_{dc},RMS,max}} = \frac{5\sqrt{3}}{6\pi}\, I \approx 0.46\, I. \tag{29}$$

The capacitor charge ripple $\Delta q_{\mathrm{C_{dc}}}$ (i.e., the high-frequency current-time area) can be directly obtained by integrating the DC-link current $i_{\mathrm{C_{dc}}}$, as

$$\Delta q_{\mathrm{C_{dc}}} = \int_0^t i_{\mathrm{C_{dc}}}\, \mathrm{d}t, \tag{30}$$

which features a ${}^{T}/_{6}$ periodicity. However, since the analytical expression of $\Delta q_{\mathrm{C_{dc}}}$ and the location of its maximum both change with $M$ and $\varphi$, the expression of $\Delta Q_{\mathrm{C_{dc},pp}}$ is a complicated piecewise-defined function [26], which is not reported here for reasons of simplicity. Therefore, $\Delta Q_{\mathrm{C_{dc},pp}}$ is calculated numerically and is illustrated in normalized form in Fig. 8 for both unipolar PWM and unfolder PWM, where $\Delta Q_{\mathrm{n}} = I/f_{\mathrm{sw}}$ is the normalization factor. The worst-case value of $\Delta Q_{\mathrm{C_{dc},pp}}$ for unipolar PWM is obtained for $\varphi = 0$ and $M = {}^{2}/_{\sqrt{3}}$, as

$$\Delta Q_{\mathrm{C_{dc},pp,max}} = \frac{\sqrt{3}}{8}\, \Delta Q_{\mathrm{n}} \approx 0.216\, \Delta Q_{\mathrm{n}}, \tag{31}$$

whereas the worst-case $\Delta Q_{\mathrm{C_{dc},pp}}$ value for unfolder PWM is found for $\varphi = \pm{}^{\pi}/_{2}$ and $M = {}^{2}/_{\sqrt{3}}$ (i.e., as in the two-level inverter [26]), as

$$\Delta Q_{\mathrm{C_{dc},pp,max}} = \frac{1}{4}\, \Delta Q_{\mathrm{n}} = 0.25\, \Delta Q_{\mathrm{n}}. \tag{32}$$

Comparing the two considered modulation strategies, it is observed that unipolar PWM requires a significantly higher DC-link RMS current capability (i.e., $\approx 80\,\%$ higher) with respect to unfolder PWM, meanwhile allowing for a slightly lower peak-to-peak charge ripple (i.e., $\approx 16\,\%$ lower). Therefore, when the DC-link capacitor sizing is limited by the RMS current capability (i.e., typical for film capacitors and/or for high-frequency operation), unfolder PWM can provide a substantial reduction in the overall DC-link capacitance requirement.

## IV. Converter Design

In this section, the complete design of the converter is carried out, describing the selection of the semiconductor devices, the selection/sizing of the DC-link capacitors, the sizing of the thermal dissipation system and the estimation of the semiconductor losses and efficiency. Furthermore, a component disposition and PCB layout are proposed, leading to a three-phase full-GaN 100 kVA 400 V DBI design concept. The design specifications and the nominal operating conditions of the considered drive inverter are reported in Table I.

TABLE I. DBI specifications and nominal operating conditions.

| Parameter | Description | Value |
|---|---|---|
| $S$ | Apparent Power | 100 kVA |
| $V_{\mathrm{dc}}$ | DC-Link Voltage | 400 V |
| $I$ | Peak Phase Current | 167 A |
| $f$ | Fundamental Frequency | 1000 Hz |

### A. Semiconductor Devices

The most suitable semiconductor device for the application is identified by comparing the performance of all commercially available 600/650 V GaN devices and technologies, including e-mode HEMTs, cascode d-mode HEMTs and direct-drive d-mode HEMTs [27]. The VisIC V08TC65S2A direct-drive d-mode HEMT is selected due to its excellent conduction/switching performance trade-off, its absolute on-state resistance value (i.e., 7.8 mΩ at 25 °C) and its unparalleled cooling effectiveness (i.e., 0.1 K/W junction-to-case thermal resistance, further enhanced by an embedded electrically insulated cooling pad) [28]. An overview of the device package is provided in Fig. 9(a).

Leveraging the conduction and switching characteristics shown in Fig. 9(b)–(c), assuming a case-to-heatsink specific thermal resistance $r_{\mathrm{th,c\text{-}hs}} = 70\,\mathrm{mm^2\,{}^{\circ}C/W}$ (cf. Section IV-C), and considering a typical cooling fluid (i.e., ≈heatsink) temperature $T_{\mathrm{f}} = 75\,{}^{\circ}\mathrm{C}$, the DBI semiconductor loss and efficiency in nominal operating conditions are estimated as functions of the switching frequency using a coupled electro-thermal model (i.e., $R_{\mathrm{ds,on}}$ is temperature-dependent). The results are reported in Fig. 10(a)–(b).

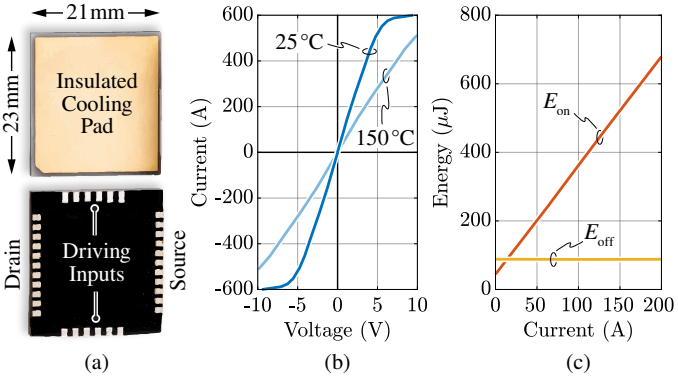


Fig. 9. (a) top and bottom view of the selected VisIC V08TC65S2A direct-drive d-mode HEMT [28], (b) conduction characteristics ($R_{\mathrm{ds,on}} = 7.8\,\mathrm{m\Omega}$ at 25 °C, $R_{\mathrm{ds,on}} = 16\,\mathrm{m\Omega}$ at 150 °C), and (c) switching energies ($k_{0,\mathrm{on}} = 44.3\,\mu\mathrm{J}$, $k_{0,\mathrm{off}} = 86.5\,\mu\mathrm{J}$, $k_{1,\mathrm{on}} = 3.18\,\mu\mathrm{J/A}$, $k_{1,\mathrm{off}} \approx 0\,\mu\mathrm{J/A}$).

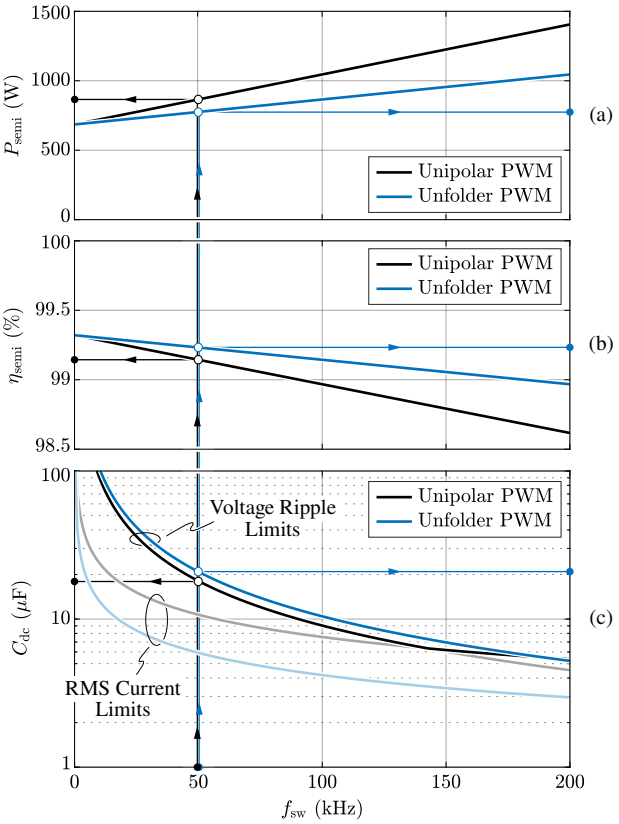


Fig. 10. (a) semiconductor loss and (b) semiconductor efficiency for unipolar and unfolder PWM as functions of $f_{\text{sw}}$ in nominal operating conditions (i.e., $V_{\text{dc}} = 400\,\text{V}$, $I = 167\,\text{A}$, $M = 2$) and assuming a cooling fluid temperature $T_{\text{f}} = 75\,^{\circ}\text{C}$. (c) DC-link capacitance $C_{\text{dc}}$ worst-case requirement as function of $f_{\text{sw}}$. The selected design frequency is $f_{\text{sw}} = 50\,\text{kHz}$.

### B. DC-Link Capacitor

In typical three-phase drive inverter systems, the DC-link capacitor determines the converter size and weight and is thus a crucial component. To maximize the DBI performance, PLZT ceramic capacitor technology is considered, since it features high RMS current capability, high temperature operation, excellent volumetric/gravimetric capacitance density and improved characteristics with increased switching frequency [29], [30]. In particular, the CeraLink® LP series from TDK (i.e., 500 V 0.6 µF capacitors [31]) is selected to size the DC-link capacitor according to the approach outlined in [30].

Fig. 10(b) shows the DC-link capacitance $C_{\text{dc}}$ worst-case requirement as function of $f_{\text{sw}}$, either determined by the maximum peak-to-peak voltage ripple (i.e., $\Delta V_{\text{pp,max}} = 10\,\% \cdot V_{\text{dc}} = 40\,\text{V}$) or by the maximum RMS current carrying capability (i.e., assuming an ambient temperature of 85 °C) [30]. To best exploit the PCB space available for the placing of the capacitors (i.e., defined by the width of the semiconductor driving and power loops, cf. Section IV-E) and aiming to satisfy the capacitance requirement of both unipolar PWM and unfolder PWM, $f_{\text{sw}} = 50\,\text{kHz}$ is selected as design value, leading to excellent semiconductor efficiency in nominal operating conditions (i.e., 99.1 % for unipolar PWM, 99.2 % for unfolder PWM) and a total capacitance requirement $C_{\text{dc}} \geq 20.8\,\mu\text{F}$ (i.e., determined by unfolder PWM). In worst-case conditions, the DC-link capacitor must withstand $\approx 139\,\text{A}$ for unipolar PWM and $\approx 77\,\text{A}$ for unfolder PWM.

### C. Heatsink and Thermal Dissipation System

A schematic overview of the considered thermal dissipation system is reported in Fig. 11, where the two three-phase inverter

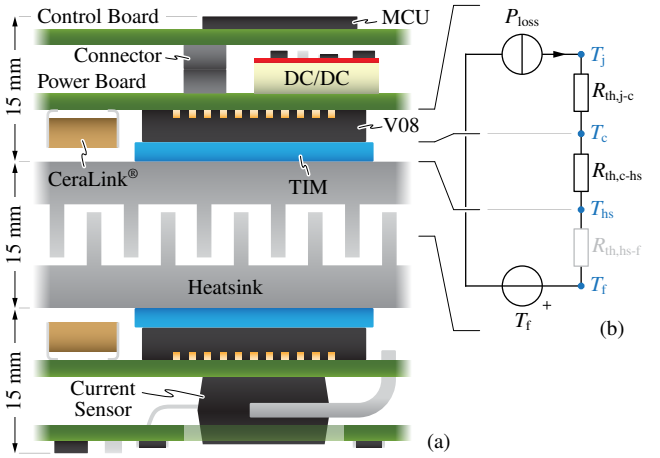


Fig. 11. (a) schematic cross-section of the proposed DBI design concept and (b) steady-state equivalent circuit of the thermal dissipation system. The heatsink-to-fluid thermal resistance $R_{\text{th,hs-f}}$ is greyed out since it can be neglected (i.e., $T_{\text{hs}} \approx T_{\text{f}}$).

units (cf. Section IV-E) are mechanically connected to the opposite sides of the liquid-cooled heatsink (i.e., to reduce the converter volume). Since the top surface of the VisIC V08TC65S2A is electrically insulated [28], a 2 mm-thick graphite-based thermal interface material (TIM) is used to thermally connect the semiconductor devices to the heatsink, achieving a case-to-heatsink thermal resistance $R_{\text{th,c-hs}} \approx 0.15\,^{\circ}\text{C/W}$ at $\approx 100\,\text{kPa}$ (15 psi) of contact pressure (i.e., to be added to $R_{\text{th,j-c}} \approx 0.1\,^{\circ}\text{C/W}$). Furthermore, a high-performance 15 mm-thick pin-fin liquid cooled heatsink is considered, providing negligible temperature rise (i.e., $T_{\text{hs}} \approx T_{\text{f}}$) due to its excellent specific thermal performance (i.e., $< 100\,\text{mm}^2\,^{\circ}\text{C/W}$), the large available surface (i.e., 145 x 80 mm, cf. Section IV-E) and the relatively low semiconductor loss (i.e., $P_{\text{semi,max}} \approx 865\,\text{W}$ for unipolar PWM, cf. Fig. 10(a)).

### D. Performance Estimation

Since the semiconductor devices, the DC-link capacitors, the thermal dissipation system and the operating switching frequency have been defined, an estimation of the inverter semiconductor loss and efficiency is carried out. Fig. 12 shows the semiconductor efficiency of the designed DBI as function of the modulation index $M$ and the AC-side peak phase current $I$ for both unipolar PWM and unfolder PWM. As expected, unfolder PWM achieves the best performance, with an estimated peak efficiency of $\approx 99.7\,\%$ at $\approx 1/4$ of the rated current.

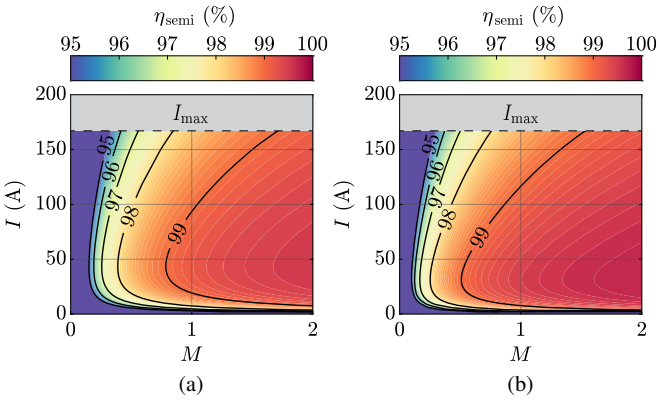


Fig. 12. Estimated semiconductor efficiency of the designed DBI as function of the modulation index $M$ and the peak phase current $I$, assuming $V_{\text{dc}} = 400\,\text{V}$, $f_{\text{sw}} = 50\,\text{kHz}$ and $T_{\text{f}} = 75\,^{\circ}\text{C}$ for (a) unipolar PWM and (b) unfolder PWM.

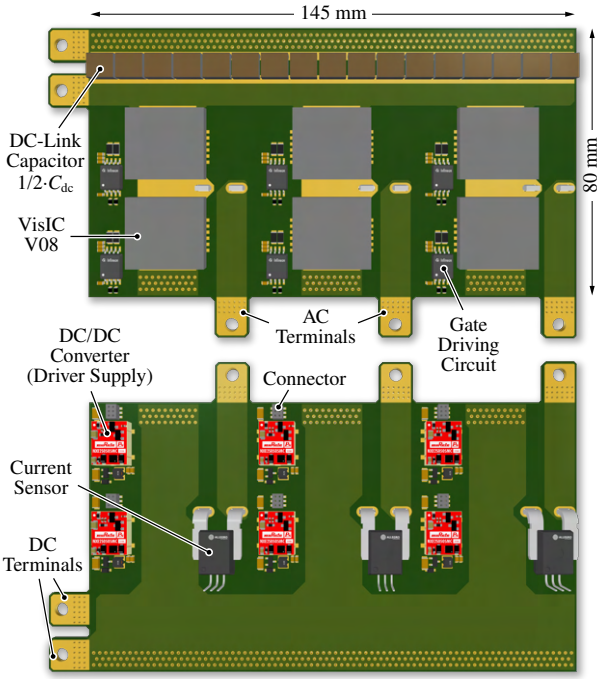


Fig. 13. Top and bottom view of one three-phase power board (i.e., first inverter unit) of the proposed full-GaN 400 V 100 kVA DBI design concept.

### *E. Design and Layout*

The proposed DBI design concept consists of two separate three-phase inverter units mechanically connected to the opposite sides of a common heatsink (cf. Fig. 11). The power board of the first inverter unit, which includes power semiconductors, capacitors, driving circuits and current sensors, is illustrated in Fig. 13. The PCB features 300 µm thick copper tracks to withstand the current stress in rated conditions and the DC-link capacitor (i.e., $C_{\mathrm{dc}}/2$) consists of 17 CeraLink® 500 V 0.6 µF units (i.e., $C_{\mathrm{dc}} = 20.4\,\mu\mathrm{F}$). The power board of the second inverter unit (not shown in Fig. 13) does not include the current sensors and features the DC terminals on the opposite side, to ensure a compact DC-link connection between the two boards. To best exploit the available PCB area and minimize the converter height, only low-profile components are selected, obtaining a total height of $\approx 45\,\mathrm{mm}$ (i.e., including the thermal dissipation system and the control boards, cf. Fig. 11). Therefore the proposed DBI concept achieves a total volume of $145 \times 80 \times 45\,\mathrm{mm} \approx 0.52\,\mathrm{dm}^3$ and an estimated volumetric power density of $\approx 192\,\mathrm{kVA/dm^3}$.

## V. Conclusion

This paper has proposed the analysis and the conceptualization of a full-GaN 100 kVA 400 V three-phase double bridge inverter (DBI) for next-generation EV drives. A comprehensive theoretical assessment of all active and passive component stresses has been carried out, providing useful tools for the converter sizing. Two modulation strategies have been compared, demonstrating a trade-off among machine phase flux ripple, DC-link capacitor stress and semiconductor losses. While unipolar PWM ensures minimum PWM-induced losses and lower DC-link voltage ripple, unfolder PWM enables higher inverter efficiency and reduced DC-link RMS current. Remarkably, unfolder PWM also unlocks hybrid DBI implementations, i.e. adopting different (optimized) semiconductor technologies for the two three-phase inverter units. Finally, a DBI design concept has been developed, achieving an estimated 99.7 % peak semiconductor efficiency (unfolder PWM) and a $192\,\mathrm{kVA/dm^3}$ power density.

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