A readout chip for spectroscopic X-ray imaging in photon-counting pixel detector

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***Abstract*—A pixel detector readout chip with multiple energy bins was designed for X-ray imaging applications. This chip was developed in a 0.11 μm CMOS technology.The active area on this chip consists of a matrix of 8 $\times$ 112 square pixels with 110 μm side. Each pixel unit was implemented with four programmable digital energy thresholds, which permits spectroscopic imaging in photon-counting pixel detectors. The deposited energy is measured with Time-over-Threshold method and a 5-bit clock cycle counter in the digital domain. Each energy bin has a 12 binary bit counter for recording the number of incident photons. Imaging quality degradation caused by charge sharing effect has been addressed by means of a digital in-pixel correction algorithm, which allows inter-pixel communication and can allocate the hit to the pixel with largest charge deposit. The design of this readout chip is presented in this paper.**

I. Introduction

SPECTRAL Computed Tomography (CT) based on photon counting detector is available for clinical research and has the potential to dramatically change the clinical CT industry in the near future. Photon counting CT can reduce the X-ray dose delivered to the patient, reconstruct the images at a higher resolution and contrast-to-noise ratio (CNR) [1]. In the photon counting detector system, the induced signal is compared with a number of energy thresholds, a counter associated to an energy bin is incremented if the signal falls within this bin [2]. In some semiconductor detectors, e.g., silicon and cadmium telluride, charge sharing happens if the photon is absorbed close to the border between two detector elements. As a result, distortion is introduced to the measured energy spectrum, increasing image noise and decreasing the image CNR [3]. Some chips have been proved capable of mitigating the effects of charge sharing [3]–[6].

A readout chip with multiple energy bins was designed to permit spectroscopic imaging in photon counting pixel detector. This project is embedded within ARCADIA (Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays) research that aims to develop and test monolithic chips with scalable architecture for particle detection [7]–[9]. The energy bins are defined by 4 thresholds, which provide the possibility to sample the different sections of incoming energy spectrum simultaneously. An in-pixel charge sharing correction algorithm is implemented by means of comparing Time-over-Threshold (ToT) signal with neighboring pixels. This chip was submitted to be manufactured in June 2022, before the submission it was verified by a serious of post-layout simulations.

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II. Chip Overview

The chip was designed in a commercial 0.11 μm CMOS technology. The chip electronics can be divided into two regions, as shown in Fig. 1, the sensitive pixel matrix and the peripheral circuits. The peripheral circuits at the bottom of the chip contain a duplex serial peripheral interface block for the pixel configuration and chip control, 7 data serializers, 7 I/O LVDS transceivers, 1 LVDS receiver, various analog blocks and a large number of power pads, analog pads and digital pads. All pads are placed at the bottom and therefore the chip can be tiled on three sides.

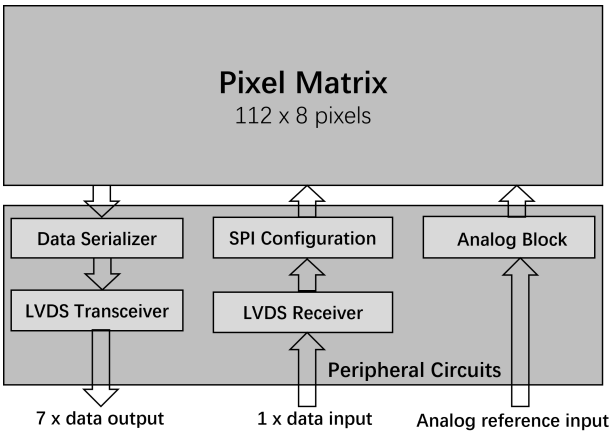

Fig. 1. Block diagram of the chip.

The chip works in two modes, the independent mode and the summing mode,

1) In the summing working mode, the charge sharing effect is addressed. In each single readout channel the collected charge is processed by two stages of amplifiers, one of the second-stage amplifier has four inputs to acquire the output signals from the first-stage amplifiers in the local and adjacent pixels, which works as a summing node to collect all the deposited charge in a cluster of 2 $\times$ 2 pixels, and to reconstruct the whole deposited energy. In order to find the pixel which has the largest portion of the generated charge, one pixel communicates with its 8 neighboring pixels by means of exchanging ToT signals. An on-pixel correction logic compares the ToTs to determine if the local pixel was hit and then allocate all collected charge to it.
2) In the independent working mode, the communication between neighboring pixels is closed, every pixel works independently and the on-pixel charge sharing correction algorithm is disabled.

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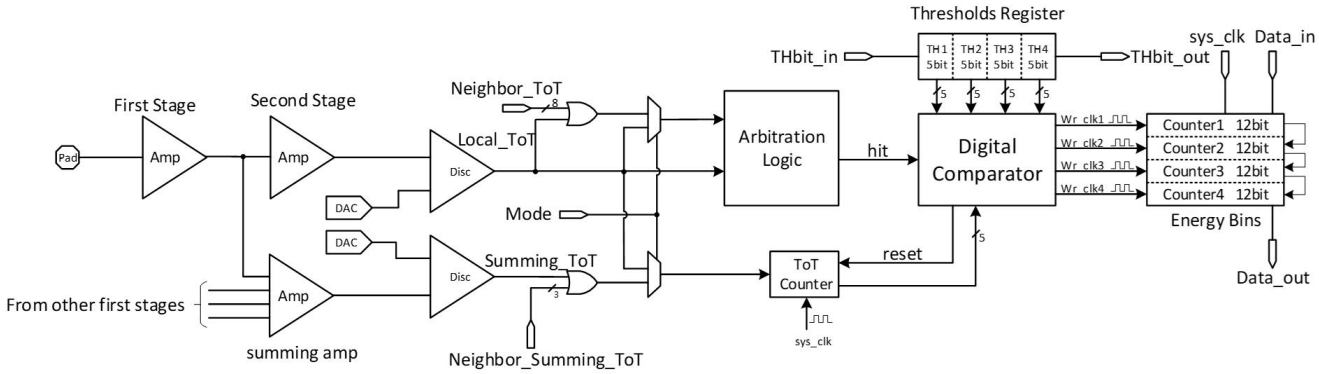

Fig. 2. Block diagram of a single signal processing channel architecture containing both analog and digital parts.

The analog part was designed to be able to handle a counting rate of 350 kHz per pixel. The power consumption is around 0.021 mW and 0.12 mW per pixel for analog and digital circuits working with a 100 MHz clock respectively.

III. Pixel Architecture

The block diagram of one readout channel architecture is shown in Fig. 2., every pixel consists of three parts, charge collection electrodes, analog circuits and digital circuits. The analog circuits employ two stages amplifiers with Krummenacher feedback [10], [11]. After the second stages two asynchronous discriminators are developed for generating digital ToT pulses. The output of the summing node is sent to a ToT counter by which the summing ToT signal is sampled at the rising edges of system clock in the digital domain. In the independent working mode, the output of summing node is cut off by a multiplexer that is controlled by the mode selection.

The arbitration logic module in the digital domain is responsible for eliminating the effects of charge sharing. The arbitration logic compares the local ToT with ToT signals from its 8 neighbors, if the local ToT is longer than others, e.g., the local pixel has the largest charge deposition with respect to its neighbors, as a result, an index signal named Hit is generated to enable the digital comparator.

In the digital comparator module, the content from ToT counter is compared with these four digital thresholds. Every digital threshold in each pixel is configured independently, which makes it possible to calibrate the dispersion. Depending on their energy, the X-ray photons are sorted into four energy bins whether they are above or blow the different thresholds. Four 12-bit linear feedback shift register (LFSR) are implemented, they can be configured as standard binary counters during the data recording or chained together with other registers in the same column of pixels for the readout.

A. Charge sharing correction algorithm

The charge generated from an interaction in the sensor may spread among a group of pixels. The goal of the charge sharing calibration algorithm is to assign an individual hit to the right pixel where the interaction happened. The generated charge

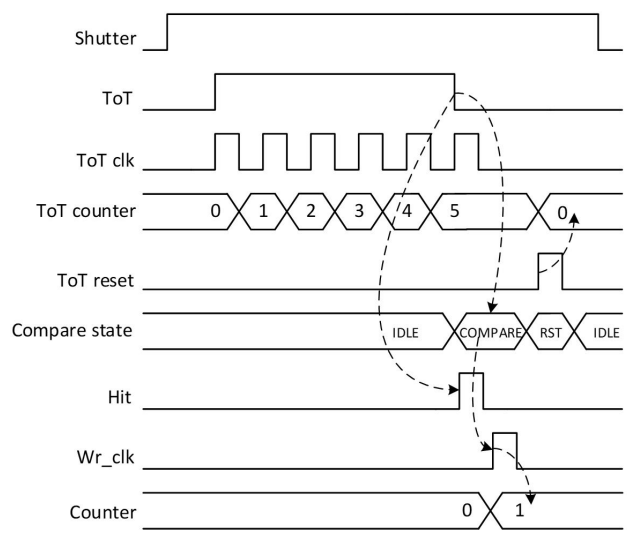

Fig. 3. The generated charge by a incident photon may spread over a group of pixels and be collected by more than one electrodes. The charge sharing effect causes the loss of energy information.

spreads from the center of the photon impact, therefore, it is obvious that the pixel which is hit by the incident photon has the largest proportion of the generated charge. In order to find the pixel was hit, the algorithm must compare the signals between pixels. The comparisons of such signals were performed between their respective ToT.

Before the comparison logic, two OR gate units are implemented and each of which is constructed with several standard two-inputs OR cells that are selected from the PDK library provided by the technology vendor. The function of the OR gate is selecting the maximum one of these 9 input ToT signals based on the functionality of the standard or logic gate. The output is high as long as at least one input is high. In other words, the output rises to high with the arrival of the ToT signals, falls to low with the end of maximum ToT input. Therefore, the duration time the output signal always equals to that of the maximum ToT. Consequently, the comparison logic only needs to compare two signals, the local ToT and the output of OR gate, rather than comparing the local ToT with

8 neighboring ToT directly. The complexity of the comparison logic was reduced significantly and the amount of required circuit resources was saved a lot as well. The delay for each or gate and for interconnects between these gates are only several tens of picoseconds, thus the cell delay and interconnect delay can be ignored with respect to the duration of the ToT signal is several tens of nanoseconds or hundreds of nanoseconds.

A simplified timing diagram as shown in Fig. 3. presents how the digital logic works. The ToT counter records the number of the rising edge of ToT clock in a certain time window that as long as the duration time of ToT signal. The falling edge of ToT ends the counting process and then the state machine enters to the comparison state where the logic compares the local ToT with adjacent ToTs. After the comparison in reset state a ToT reset signal is generated to clear the content of ToT counter. If the comparison shows a positive result a hit signal will be sent the digital comparator unit where the digitized energy is compared with 4 digital thresholds and the event is allocated to an appropriate energy bin.

B. Energy bins

Each pixel contains four 12-bit energy bin registers which are implemented in LFSR structure. They can operate in two modes by controlling the selection input of the multiplexers,

1) Counting mode.
2) Serial shift out mode.

The energy bin register is one of the more common forms of LFSR is formed from a simple shift register with feedback from a number of XOR gates [12], [13]. If the control signal shutter is low the energy bin register works in the counting mode, the input of the register is the output of the feedback circuit. The input is a series of pseudo-random values with a certain sequence which is determined by the feedback function defined by the XOR feedback circuit. Therefore, the stored pseudo-random data in the energy bin register is required to be decoded off-chip.

During the readout process, all these four energy bin registers in a pixel as well as other registers in the same column are chained together and shifted out serially. The input is switched from the output of feedback circuits to the output of preceding D flip-flop by setting the shutter to high.

IV. Layout and Simulation Results

The full chip layout that includes active circuits and padframes is shown in Fig. 4.. Three regions, a) active pixel matrix, b) peripheral circuits and c) padframes are marked.

Fig. 5. shows the layout of a single pixel. As can be seen, the analog island is placed at the center. In order to increase the charge collection efficiency, four square electrodes with the dimension of 20 $\times$ 20 μm^2 are at the corners of analog part.

There are 2 versions of the pixel, one with only the electrodes and one with a pad for connection to an external sensor. Since the charge sharing correction algorithm requires inter-pixel communications, gaps between pixels were reserved intentionally as the routing channels for inter-pixel wire connections. The technology we used has 6 metals, metal 6, the top metal in vertical direction, is used for analog bias routing, analog and digital power supplies. The digital clock distributions are realized on metal 5.

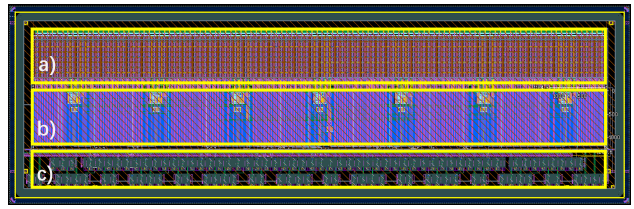

Fig. 4. Layout of the full chip. a) is the pixel matrix that contains 112 columns and each column has 8 pixels. b) is the peripheral circuits by which the SPI configuration, data transmission and receiving and analog bias blocks are implemented. c) is the double-rows padframes that are used for power supplies, analog bias input and digital I/Os.

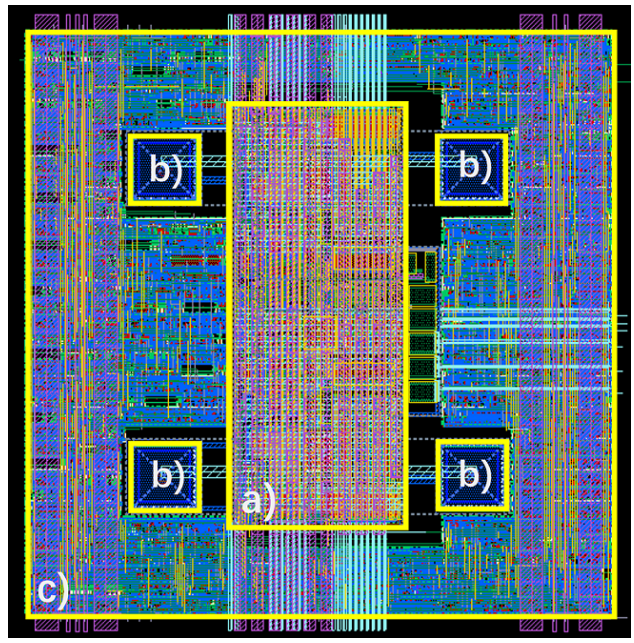

Fig. 5. Layout of a single pixel with a size of 110 μm $\times$ 110 μm. a) is the analog circuits placed at the center. b) are the 4 electrodes that are adopted for bump bonding connection to the sensor and for charge collection. The left area that excludes analog part and electrodes in c) is occupied by digital circuits. Gaps with width of 6 μm, black part outside the active area c), are reserved for inter-pixel communications.

To optimize the connection resistance between the electrodes the digital electronics were inserted between the 4 electrodes, this choice resulted in analog islands between digital electronics. Consequently, the following precautions were taken: special attention was paid to the placement of the components, created guard rings to isolate the analog electronics, separate power grids, and general attention to the placement of the more sensitive bias lines.

A. Charge sharing correction logic simulation

The charge sharing correction algorithm is one of the main goals of this chip. It was mainly realized by the digital circuits, thus for the full examination of the algorithm, 9 ToTs were generated randomly from 0 ns to 320 ns (the maximum can be measured) as the input of arbitration unit in the digital domain

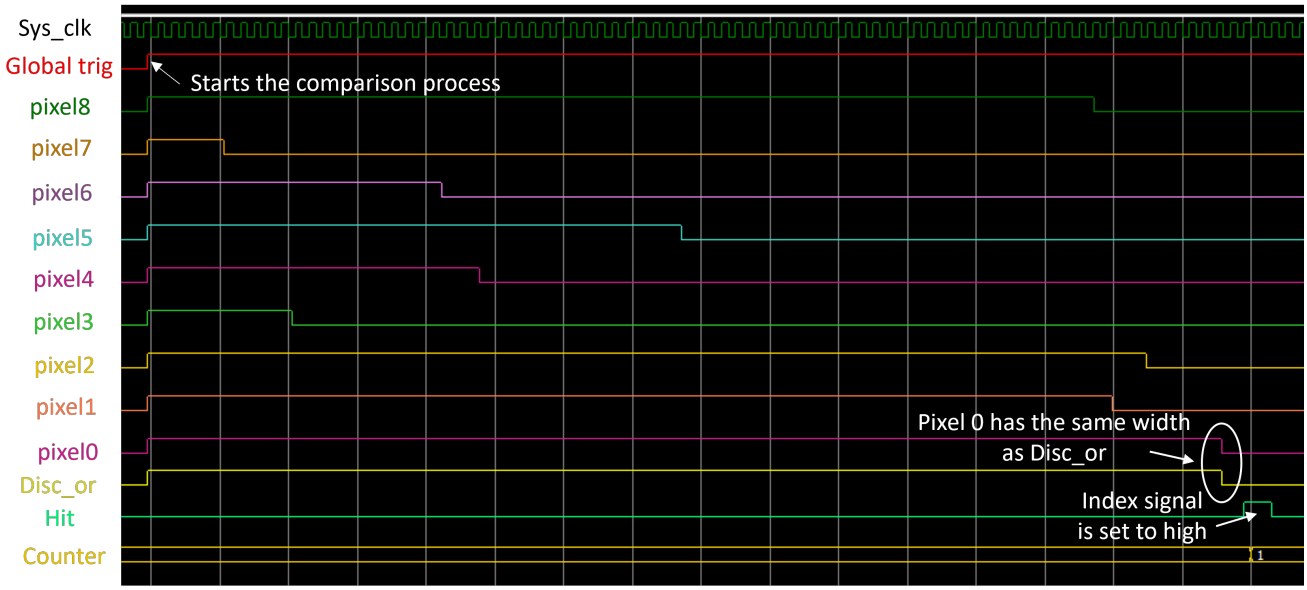

Fig. 6. A simulation example for the charge sharing correction algorithm.

(see in the Fig. 2.). Fig. 6. shows a simulation example in which the local ToT (from pixel 0) is the largest one and thus a hit signal is pulled to high to indicate the positive comparison result. The correction algorithm worked well with post-layout simulations.

V. Conclusion

The photon counting pixel detector readout chip was designed with four energy bins which provides the possibility of being applied in spectroscopic X-ray imaging. This chip was fabricated in a commercial 110nm CMOS technology. The active area of the chip consists of 112 $\times$ 8 pixels with size of 110 μm $\times$ 110 μm. An in-pixel correction algorithm has been developed for mitigating the effects of charge sharing. The key features of the chip, e.g., charge sharing correction algorithm, and two working modes have been verified by post-layout simulations.

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