Forum on specification & Design Languages

Hybrid digital-neuromorphic architecture integration for low-power applications

Politecnico di Torino
Dipartimento di Automatica e Informatica
DAUIN

Challenges

The presented ongoing research aims to study the integration between traditional processors and neuromorphic devices in edge applications, where power budgets and computational resources are often limited. The co-existence of the two domains will allow on one hand to perform artificial intelligence and machine learning tasks by exploiting Spiking Neural Networks (SNNs), and on the other hand to manage data handling and communications.

The first open-source architectures that were explored are:

- PULPissimo [1]: a single-core digital microcontroller architecture based on the RISC-V ISA, aimed at low-power IoT applications (Fig. **1**)
- ReckOn [3], a digital neuromorphic processor capable of implementing Spiking Recurrent Neural Networks with online learning capabilities. (Fig. **2**)

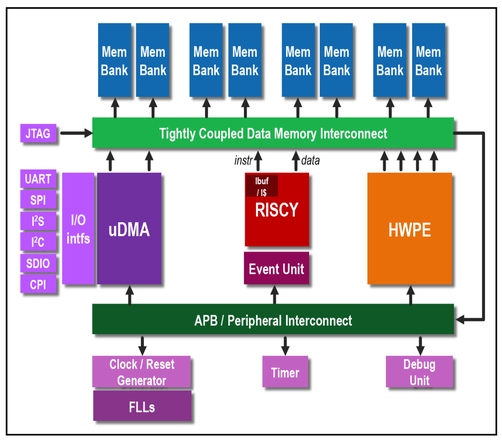

Fig. **1**: Architecture of PULPissimo SoC – Adapted from [2]

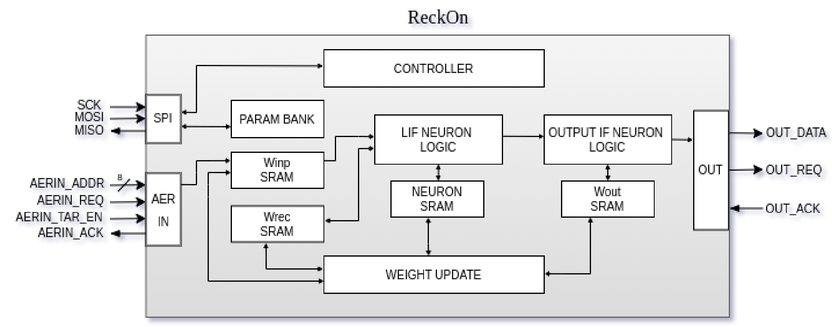

Fig. **2**: Architecture of ReckOn

Implementation

The neuromorphic processor ReckOn is equipped with a SPI peripheral that can be used to access its SRAM blocks and the SNN configuration parameters. In our first configuration, PULPissimo's µDMA [4] was programmed to drive the SPI channel and gain access to ReckOn's network configuration and SRAM blocks (Fig. **4**) [4].

In Fig. **3** it's possible to see the SPI transmission between PULPissimo and ReckOn: the communication protocol asks for packets of 64 bit sent to ReckOn, including a 32-bit command and a 32-bit data packet. The outcome of the transmission can be seen from the updates of the different registers at the respective timesteps.

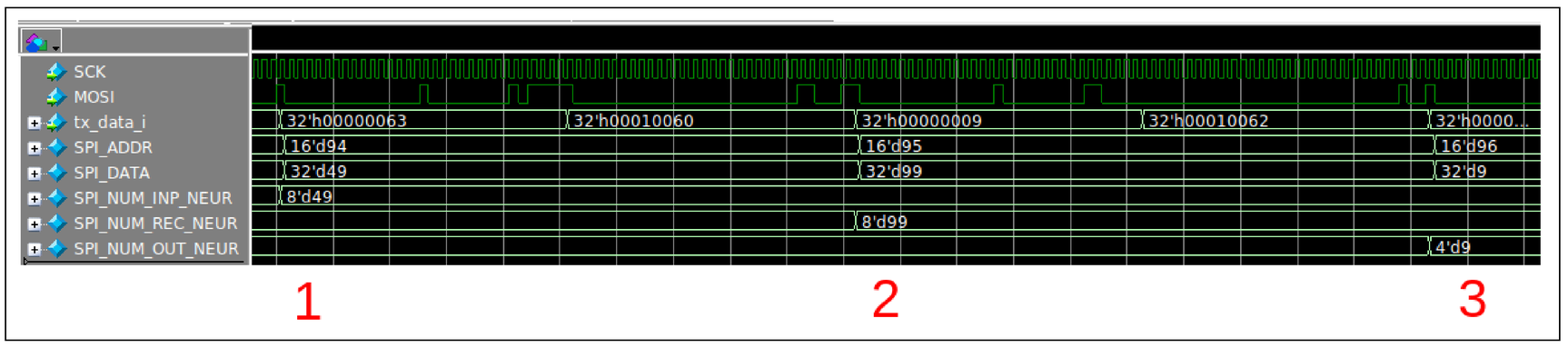

Fig. **3**: ReckOn's registers update driven by PULPissimo: at timesteps 1, 2 and 3 the registers that describe the number of neurons in the Spiking RNN's input, recurrent and output layers are updated.

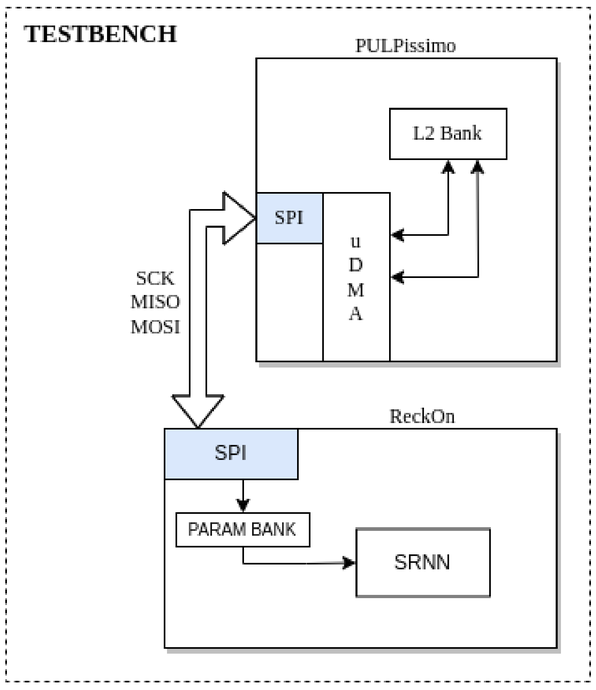

Fig. **4**: Schematic representation of the SPI interface between PULPissimo and ReckOn

Future Developments

HWPE (HardWare Processing Elements)

In this study, PULPissimo performs ReckOn's configuration through its SPI port.

For the future, the integration between the two domains will be further explored by making use of PULPissimo's HWPE compatibility and having ReckOn as a co-processor inside the main SoC. This will allow the neuromorphic processor to access its network's parameters directly from the dedicated allocations in the L2 memory inside PULPissimo, thus avoiding long configuration times imposed by the SPI protocol (Fig. **5**).

The final goal will be to build a complete hybrid architecture and deploy it on FPGAs to study and support use-cases that make use of sparse data and event-driven computing.

High Performance Computing

To exploit the full computational power of neuromorphic architectures it's necessary to change the computing philosophy, hence by approaching the HPC paradigm. This will be done by adopting different architectures both neuromorphic, such as commercial products or other multi-core, digital processors that can be deployed on FPGAs, and more performing CPUs such as the 64-bit RISC-V core CVA6, which can run Linux kernels [5].

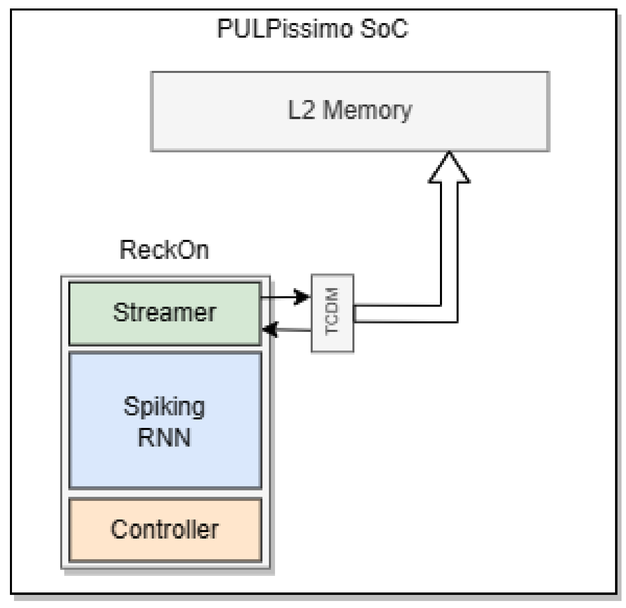

Fig **5**: HWPE interface inside PULPissimo with ReckOn as the main neuromorphic co-processor

Michelangelo Barocci, Department of Computer and Control Engineering, Politecnico di Torino – michelangelo.barocci@polito.it

[1] P. D. Schiavone et al., IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, p 1-3, 2018
[2] github.com/pulp-platform/pulpissimo
[3] C. Frenkel et al., IEEE International Solid- State Circuits Conference, p 1-3, 2022
[4] M. Barocci et al., under publication
[5] F. Zaruba et al., IEEE Transactions on Very Large Scale Integration (VLSI) Systems, pp 2629-2640, 2019

EBRAINS Italy
Italiadomani
PIANO NAZIONALE DI RIPRESA E RESILIENZA
Finanziato dall'Unione europea
NextGenerationEU