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Dead Time Constraints in Gallium Nitride Devices for Inverter Applications

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Keywords

Power electronics, Gallium Nitride transistors, HEMT, Inverter, Dead time, Reverse conduction.

Abstract

The paper deals with investigating the dead time constraints for Gallium Nitride (GaN) devices in inverter switching leg applications. The power devices considered are the low-voltage enhancement GaN FETs. The variable current (typical of inverter applications) influencing the dead time impact is analysed through several simulation results and experimental tests. Furthermore, device temperature measurements support the dead time effect. The proposed survey allows for obtaining a procedure for correctly selecting the length of the dead time to avoid cross-conduction and lower the device losses.

Introduction

In power converter applications with switching legs, such as half-bridge or full-bridge DC-DC converters or in DC-AC inverter applications, the dead time is necessary to avoid possible cross-conduction due to the actual device's transients. In inverter applications, the dead time features a negative effect on converter operation. From the point of view of the quality of the output waveforms, the dead time duration influences the output voltage and current distortion, increasing the level of the fifth and seventh harmonics [1]. The harmonic distortion in the AC motor inverters can result in additional torque ripple. Furthermore, the dead time impacts the reliability and efficiency of the converters. The reduction of the dead time length is crucial to optimize the efficiency and dynamic performances of the inverter. Gallium Nitride Field Effect Transistors (GaN FETs) devices are recently introduced in the power electronic switches arena; they belong to the high mobility electron transistors (HMET) featuring high switching frequency and noticeable temperature reachable. Currently, they are widely used at low voltage (<200V) to replace silicon (Si) MOSFETs in converters with high switching frequencies (up to tens of MHz) and power ratings in the mid-range (<100kW). While they are being developed and used with some interest for applications with voltages around 600 V as an alternative to SiC MOSFETs [2]. In recent years the use of GaN FETs for low voltages features remarkable development in applications for inverter drives for AC motors (for voltages <200V) [3]. The increasing use of these devices is correlated to the high energy density and the capability of reaching high switching frequencies (≥ 100 kHz), reducing the overall dimensions of the inverter and therefore allowing the integration of motor, inverter, and control in a single compact system obtaining an integrated modular motor drive (IMMD) [4]. In a half-bridge configuration, dead time leads the devices to operate in reverse conduction, causing power losses that are related to the structure technology of the antiparallel diode. Enhancement GaN FET devices have higher equivalent reverse diode forward voltage compared to other anti-parallel diodes connected to the switching devices, which produces more reverse conduction energy losses. Consequently, in GaN FETs, the reverse power losses are a drawback compared to those of Silicon (Si) MOSFETs [5]. The capability of bidirectional

operation of GaN FET can be used to reduce the reverse diode operation [6]. In the proposed paper, the dead time issue and the GaN FET technology impact on the device reverse conduction are investigated. The main dead time design constraints for inverter applications are explored through several simulation results and experimental tests. Finally, temperature measurements are carried out to characterize the behaviour of the device at different dead time lengths.

GaN FET Dead Time Evaluation in Inverter Application

GaN FET for low voltage application is a lateral enhancement normally-off structure. It is a bidirectional switching device. The symmetric bidirectional operation occurs with the gate-source voltage V_{GS} higher than the threshold voltage V_{GSth} when the two-dimensional electron gas (2DEG) appears. 2DEG phenomena allow high electron mobility peculiar to the GaN FET operation [7]. In the case of reverse conduction, when $V_{GS} > V_{GSth}$ enough to fully reach 2DEG operation, the GaN FET operates in an ohmic region with R_{SDon} quite similar to the resistance in direct conduction.

The inverter leg dead-time t_{dt} selection must consider the device's dynamic characteristics features, the parasitic effects introduced by the PCB, and the load connection [8]. However, the t_{dt} must be chosen long enough to avoid switching leg cross conduction but not too long to reduce the waveforms distortion effect. For evaluating the t_{dt} in a switching inverter leg typical operative condition, two cases must be considered [9].

- Reverse conduction of the switching leg turn-off device;
- Capacitance charge dynamic between the device turn-off and the reverse conduction.

In the first case, the turning-off device moves its conducted current directly to its equivalent diode, and reverse conduction appears. The reverse conduction time does not depend on the current value. Considering the switching leg in Fig. 1 is composed of the same power devices, and supposing the Q_H is the turning-on device (while Q_L is the turned-off device). Considering the positive current I_{load} from V_{DC} to the load, theoretically, Q_H can start conducting immediately when the V_{GSL} falls to V_{GSLth}. Theoretical node voltage V_S waveforms at positive load current are reported in Fig. 1b for positive voltage slope, where t_{RC} is the reverse conduction time. In the second case with positive I_{load} (Q_H is turned off, and Q_L is turned on after), the commutation time depends on the load current amplitude [7]. An additional time due to the output equivalent capacitance charging must be added. Where C_{eq} is the equivalent capacitance related to the half-bridge switching node. The theoretical node voltage V_S waveforms at positive load current are reported in Fig. 1c for negative voltage slope. From Fig. 1c arise the slope variation at increasing load current amplitude, t_f is the time related to the maximum voltage slope. The dead time evaluation is carried out by several simulation results in LT Spice, using a GaN FET model validated in [10]. The gate driver is also modelled in LT Spice to achieve very close to the actual application results in the switching leg operation for the dead time investigation. The electric schematic used for the simulation tests is depicted in Fig. 1. The inverter has a V_{DC}=48 V of the bus voltage and supplies an I_{Load}=10 A to the inductive load.

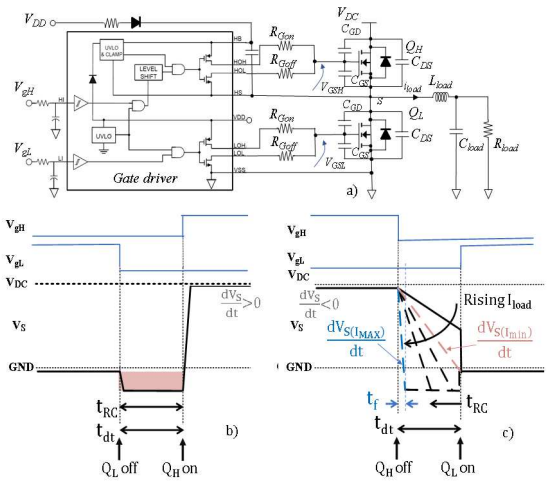

Fig. 1: a) Electric schematic of the gate driver, H-bridge, and load used in the simulation tests. Theoretical node voltage V_S waveforms at positive load current I_{load}. b) positive dV_S/dt is constant at variable I_{load}. c) negative dV_S/dt slope depending on the current magnitude

The gate command voltages are V_{gH}=V_{gL}=5 V for GaN FET. A gate driver featuring an inner turn-on resistance of 2.1 Ω; turn-off resistance of 0.6 Ω; turn-on and turn-off signal delay of 30 ns, and an 8 ns of the delay matching tolerance (t_{dm}) between the two output signals (V_{gH} for the high

side Q_H device; V_{gL} for the low side Q_L device) is used to drive the devices.

In the electric schematic of Fig. 1a, the gate driver circuit features a turn-on gate resistance of R_{Gon}=1Ω, a turn-off gate resistance of R_{Goff}=0.47 Ω, and the gate-drive command voltage of V_{gH}=V_{gL}=5 V. From the simulation results, the transient times during the commutations can be easily highlighted. Thus, the correlation with the dead time duration can be shown.

Low-Side (Q_L) Device Turn-Off with Positive Load Current

The switching transient when Q_L is turned off, and Q_H is turned on is considered. A dead time t_{dt} = 40 ns is chosen to easily investigate the dead time operation. I_{load} is set to 10 A positive (from the switching leg node to the load). The same event happens when Q_H is turned off while Q_L is turned on, and I_{load} flows in the opposite direction. Fig. 2a shows the waveforms when low-side Q_L is turned off and high-side Q_L is turned on. In Fig. 2a, t_0 is the time when V_{gL} is set to low, but V_{GSL} is still 5 V (Q_L is still in on-state). t_1 is the time when V_{GSL} falls to the threshold voltage V_{GSth}. t_2 is the time when V_{gH} is set high, but V_{GSH} is still 0 V (Q_H is still off-state). t_3 is the time when V_{GSH} rises to the threshold voltage V_{GSth}. Fig. 3b shows the current paths through the devices during the commutation time. As shown in Fig. 2a, before t_1, Q_L is still on, despite V_{gH} being still set low (see t_0-t_1 time interval in Fig. 2a. Since V_{GSL} = V_{GSth}, the current is deflected to the Q_L equivalent diode. The device works in reverse conduction (t_3-t_1=t_{RC} time in Fig. 3a. The voltage ringing on V_S, due to the stray inductances in the PCB layout [11], could be neglected for the dead time selection because it is after the time t_3. In this case, as shown in Fig. 1b at different I_{load} amplitude values, the reverse conduction duration behavior is the same.

The C_{OSS} capacitance of Q_L generates the negative current peak caused by the V_S variation. The switch Q_H starts conducting only at t_3, stopping the Q_L reverse conduction (from the time t_3 above, Fig. 2a. For this reason, the V_{gH} command could be set in the range t_3-t_2 when setting the dead time. Two times the gate driver delay matching time t_{dm} (e.g., 8 ns) must be considered for the minimum dead time selection. From these considerations, the minimum dead time is obtained when t_3=t_1, and it could be calculated as

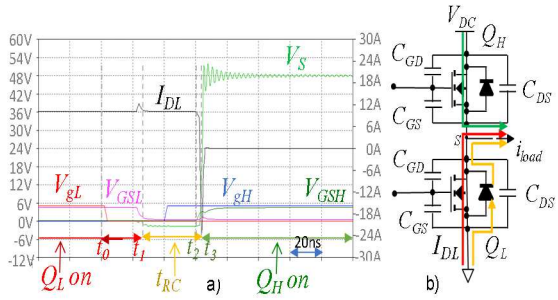

Fig. 2: GaN FET-based H-bridge. a) Waveforms during Q_H turn on with positive load current; b) current paths through the devices during the commutation time

$$t_{dt\,\min 1} = \Delta t_{0,1} - \Delta t_{2,3} + 2 \cdot t_{dm} \qquad (1).$$

Table I reports all time interval duration and the calculated t_{dtmin1} for the GaN FET-based H-bridge. The load current I_{load}=10 A is used.

Table I: Time interval duration and the calculated t_{dtmin1} for the GaN FET-based H-bridge

$\Delta t_{0,1}$ $[ns]$	$\Delta t_{2,3}$ $[ns]$	$\Delta t_{0,3}$ $[ns]$	$t_{dt\,\min 1}$ $[ns]$
26	0.9	60	17.1

High-Side (Q_H) Device Turn-Off with Positive Load Current

The switching condition when Q_H is turned off and Q_L is turned on after a dead time, t_{dt}=40 ns and I_{load}=10 A positive is considered. The same event happens when Q_L is turned off, Q_H is turned on, and I_{load} flows in the opposite direction. Fig. 3a shows the waveforms in the switching transients described above. In Fig. 4a, t_4 is the time when V_{gH} is set low, but V_{GSH} is still high (5 V). t_5 is the time when V_{GSL} falls to the plateau voltage (2 V for the chosen GaN FET). t_6 is the time when V_S falls to the reverse conduction value, and the Q_H drain current becomes zero. t_7 is the time when V_{gL} is set high, but V_{GS2} is still 0 V. t_8 is the time when V_{GSL} rises to the threshold voltage V_{GSth}. Fig. 3b shows the current path through the devices during the considered switching time. From Fig. 3a, after t_5, the Q_H drain current cannot be conducted by its equivalent diode (Fig. 3b). Still, the C_{OSSH} capacitance charges (t_6-t_5 time interval in Fig.3a). $\Delta t_{5,6}$ =t_6-t_5

depends on the current amplitude (Fig. 1c). Higher I_{load} causes a shorter $\Delta t_{5,6}$. After t_6 C_{OSSH} is charged, and the reverse conduction of the equivalent diode of Q_L starts (t_7-t_6 is the reverse conduction t_{RC} in Fig. 3a). Two times the gate driver delay matching time t_{dm} (e.g., 6 ns) must be considered for the minimum dead time selection. The minimum dead time t_{dtmin2} is obtained when t_8=t_6, and it could be calculated as:

$$t_{dt\,\min 2} = \Delta t_{4,5} + \Delta t_{5,6\,(I_{load})} - \Delta t_{7,8} + 2 \cdot \mathrm{t_{dm}} \quad (2)$$

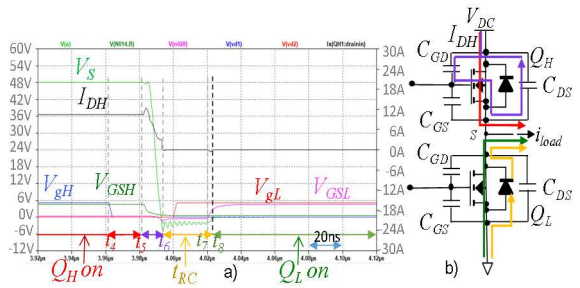

Fig. 3: GaN GaN FET-based H-bridge. a) Waveforms during Q_L turn on with positive load current; b) current paths through the devices during the commutation time.

Table II reports all the time interval duration and the $t_{dtmin2F}$ for the GaN FET-based H-bridge at I_{load}=10A.

Table II: Time interval duration and the calculated $t_{dtmin2F}$ for the GaN FET-based H-bridge

$\Delta t_{4,5}$ $[ns]$	$\Delta t_{5,6}$ $[ns]$	$\Delta t_{7,8}$ $[ns]$	$\Delta t_{4,6}$ $[ns]$	$t_{dt\,\min 2}$ $[ns]$
10	18	12	28	37

The approach to select a correct dead time in inverter leg application from motor drives arises from the above results.

GaN FET Minimum Dead Time Selection Methodology

In order to select the minimum dead time for a given operative condition (DC input rated voltage and load current peak requested), it is useful to evaluate which are the minimum dead time for different load current values. Fig. 4 shows the switching transients of the gate command voltages V_g used as input at the gate driver, the gate-source voltages V_{GS}, and the switching node voltage V_S for different load current values I_{load} (0.5 A; 1 A, 1.5 A; 2 A; 10 A; 15 A; 20 A). The dead time in the simulation test has been set to 40 ns; starting from this operative condition, the minimum dead dime can be evaluated. Fig. 4a refers to the high-side Q_H turn-on, and Fig. 4b refers to the low-side Q_L turn-on.

The gate driver time delay is of the time gap between V_g and the V_{GS} variation (30 ns). As explained, with a positive current, the minimum dead time for the Q_L turn-on does not change with the current amplitude. In this example, a minimum dead time of $t_{dtmin1F}$=15 ns has been obtained by using the formula (1).

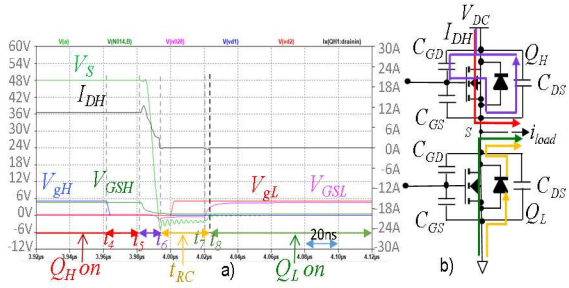

Fig. 4: (a) Waveforms during Q_H turn on; (b) Waveforms during Q_L turn on. Different load current values (0.5 A; 1 A, 1.5 A; 2 A; 10 A; 15 A; 20 A)

In the case of Q_H turning on, the load current amplitude has its influence. At I_{load} < 1.5 A, the device features a hard switching transient increasing the power loss. Furthermore, for the dead time estimation, the C_{eq} value can be computed from waveforms as

$$C_{eq} = \frac{I_{load}}{dV_S/dt} \quad (3).$$

The formula (3) is obtained empirically, by analyzing the measurements in the laboratory and finding the equivalent capacitance. C_{eq} consider the output capacitances of the low side and high side GaN FETs and the one of the motor used. C_{eq} is almost linear because the influence of the linear motor capacitance hides the non-linear trend of the GaN FET capacitances. Thus, the non-linear effect is not clearly visible in the V_S waveform. The average value obtained by the simulation for different current values is $C_{eq} = 2\,nF$. The resulting minimum dead times t_{dtmin2} calculated

by (2) for different current values are reported in Table III.

For a very low current, $t_{dtmin2F}$ is too long to achieve ZVS. But long dead time length increases the output waveforms distortion. In the Inverter leg for the motor drive, a hard-switching operation at a low current is permissible if the switching losses are maintained at a suitable level to maintain high efficiency [12]. In the case considered, a dead time shorter than $t_{dtmin2F}$ can be used (e.g., 40 ns for I_{load}<2 A).

Moreover, for high load current amplitude, $\Delta t_{5,6}$ tends to reach a minimum value. From Fig. 4b, also, t_{dtmin2} becomes a constant value for high current amplitudes (e.g., 15 ns for I_{load}>20 A). The minimum dead time values in the considered operative operation are plotted in Fig. 5 for different I_{load} values. Fig. 5a refers to the high-side Q_H turn-on commutation, while Fig. 5b refers to the low-side Q_L turn-on one.

Table III: Q_{HS} turn on. Voltage variation duration and minimum dead time calculation $t_{dt\ min2}$ for different current values

I_{load} [A]	0.5	1	1.5	2	10	15	20
$\Delta t_{5,6}$ [ns]	>40	>40	>40	36	12	10	9
$t_{dtmin2F}$ [ns]	40	40	40	40	18	16	15

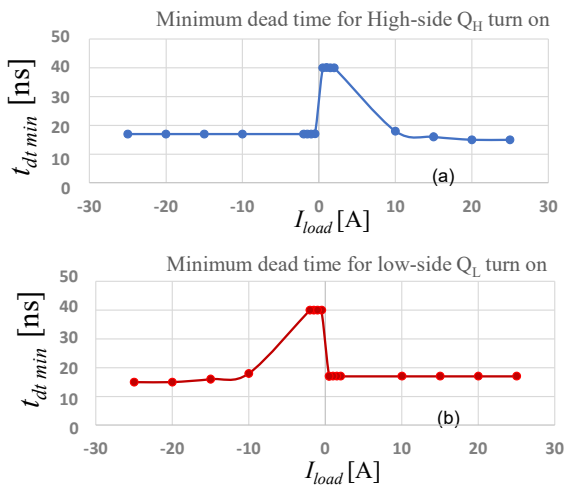

Fig. 5: Minimum dead time plot versus I_{load} value. (a) Q_L turn-off and Q_H turn-on commutation; (b) Q_H turn-off and Q_L turn-on commutation

GaN FET Minimum Dead-Time Evaluation: Experimental Results

The experimental tests are carried out to evaluate in the actual operative conditions the minimum dead time value of a GaN FET-based switching leg. A test is performed using the board EPC90137, which contains two EPC2065 GaN FETs in a Half-Bridge configuration. A switching frequency, f_{sw}=250 kHz, has been used. The dead time is t_{dt}=40 ns circa in order to completely terminate transients, such as voltage ringing, within the conduction time. The board gate driver uP1966E features a maximum delay matching time of 6 ns. Fig. 6 shows the experimental waveforms of V_{GS} and V_S for different positive load current values, I_{load} 0.5A, 1 A, 1.5 A, 2 A, 10 A, 15 A, 20 A. Fig. 6a shows the commutation in which Q_L is turned off, and Q_H is turned on. Fig. 6b shows the commutation in which Q_H is turned off and Q_L is turned on. In the case of Q_H turned off and Q_L turned on (Fig. 6a), the minimum dead time can still be calculated through (1) independently from the I_{load} amplitude. The time variation of V_{GS} from 0 V to the threshold value 1.2 V (t_{VGS} rise) is 0.51 ns, while the time t_{VGS} fall from 5 V to 1.2 V is 13.8 ns. The resulting $t_{dt\ min}$ is 7.7 ns.

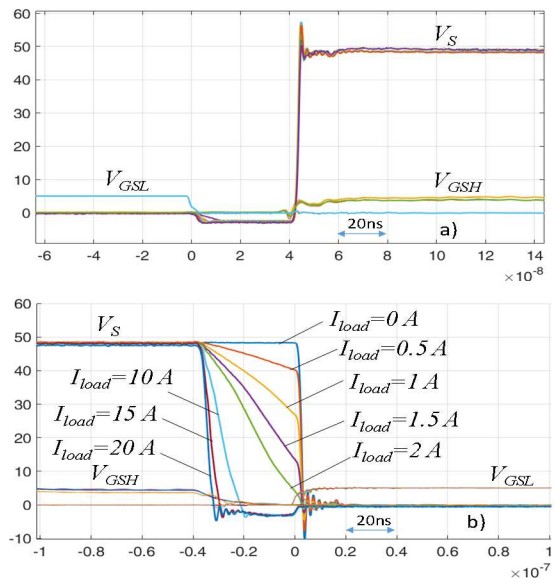

Fig. 6: Experimental gate-source voltages and switching node voltage V_S trend during dead time. (a) Waveforms during Q_H turn on; (b) Waveforms during Q_L turn on. Different load current values (0 A, 0.5 A, 1 A, 1.5 A; 2 A; 10 A; 15 A; 20 A)

In the case of Q_H turned off and Q_L turned on

(Fig. 6b), the dead time length must consider the V_S voltage variation. Also, in this case, the time variation V_{GS} from 0 V to the threshold value 1.2 V is 0.51 ns. In Fig. 6b, the time interval from V_{GS}=5 V starting variation to the time in which V_S falls to the reverse conduction value (V_{RC} - corresponding to the reverse conduction time t_{RC}), and the resulting t_{dtmin2} calculated as (2) are reported in Table IV for different current values. For I_{load}= 2 A, the ZVS condition happens and there is not the reverse conduction phenomenon. This current value is also confirmed by formula (3) when using $\Delta t = t_{dt}$ and $\Delta V_S = V_{DC}$. The hard switching operation is admitted for I_{load}< 2 A and the dead time value is saturated to the maximum of 40 ns. In this case, commutation energy loss $E_{min\ dt}$ that will be achieved by using the minimum dead time, can be calculated during the time interval $\Delta t_{4,5}$. The dead time energy losses E_{dt} is calculated during the full dead time duration. Table V reports E_{mindt} and E_{dt}.

Table IV: Q_L, turn off, and Q_H, turn on. Voltage variation duration and minimum dead time calculation t_{dtmin2} [ns] for different current values

I_{load} [A]	0A to 1.5A	2	10	15	20
$\Delta t_{5,6}$ [ns]	>40	40	20.8	11.6	9.1
t_{dtmin2} [ns]	40	40	19	9.8	7.3

Table V: Q_L, turn off, and Q_H, turn on. Commutation energy loss is achievable by using the constant dead time 40 ns, E_{dt}, and by using the minimum dead time $t_{dt\ min2}$, E_{mindt}

I_{load} [A]	0.5	1	1.5	2	10	15	20
E_{dt} [μJ]	1	1.8	2.3	2.6	7.7	*8.7*	10.5
E_{mindt} [μJ]	1	1.8	2.3	2.6	7	7.7	9.1

Dead Time Impact on the Devices Temperature

As shown in the previous paragraph, the correct dead time selection can help reduce the switching losses with a consequent lowering of the operating temperature of the power components under the same operating conditions. This aspect can be verified experimentally by monitoring the temperature of the switching devices for various load currents and dead times. Higher switching losses must reflect higher operating temperatures [13].

The two GaN FETs on the EPC90137 board are operated in buck mode at a constant duty cycle of 0.5 (i.e. both devices are in conduction for the same amount of time) at 500 kHz to maximize the impact of the switching losses. A second switching converter interfaced via an LCL filter is used to impose the load current. Given the target value of dead time and load current, the switching leg is kept working in steady state conditions for 10 minutes so that all the thermal transients are over. Next, the temperature of the hottest device is measured using a thermal IR camera, as shown in Fig. 7. The test is then repeated for different load currents and dead times. The results are summarized in Fig. 8. It is possible to notice that for each load current, there is an optimal dead time that minimizes the temperature of the hottest switch, as indicated by the black arrow. Remarkably the optimal dead time found with the thermal analysis matches the one obtained from the electrical measurements. E.g.

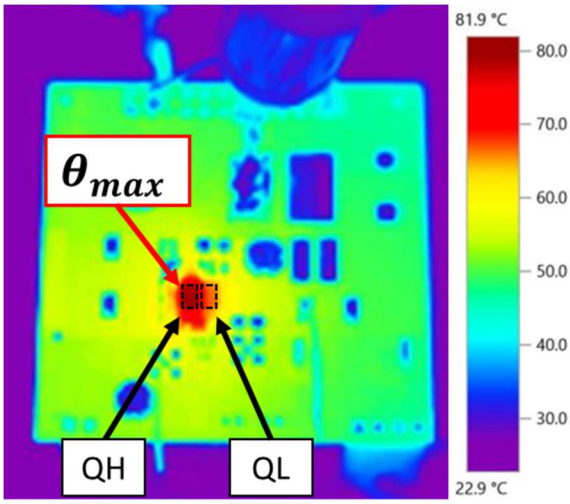

Fig. 7: High and Low side GaN FETs thermal image @I_{load}=10 A

For a load current of 2 A, the optimal dead time is 40 ns, and this value matches the one found by the previous measurements shown in Fig. 6. It must be noted that symmetrical dead times were used during the tests. A further reduction in the losses can be obtained by using asymmetrical dead times.

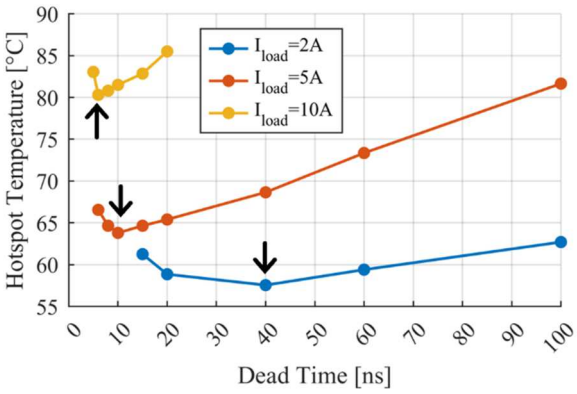

Fig. 8: Case temperature of the hottest GaN FET at different load currents and dead times

Conclusion

This paper investigates the dead time constraints in inverter legs based on GaN FET. Several simulation results are carried out to analyze in detail the reverse conduction at variable load current during the dead time duration. The switching leg node voltage slope behaviour is explored at different load conditions. An optimal dead time selection methodology is proposed. Experimental results are carried out to evaluate the actual operative condition and the dead time impact on the energy losses to demonstrate the methodology. Furthermore, thermal measurement tests are carried out. In the thermal tests, optimal dead time is selected so to minimize the temperature of the hottest switch. Remarkably the optimal dead time found with the thermal analysis matches the one obtained from the electrical measurements.

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