Synthesis

The work that has been carried out producing this thesis is a result of an industrial PhD activity, and it is made in collaboration with the Institute for Microelectronics and Microsystems of the National Research Council (CNR-IMM) and, as an employee of the company, STMicroelectronics, focused on the development of solutions to improve quality and reliability of electronic devices for industry.

The general area that I faced during the whole 3-years activity can be split in 2 main topics:

- to model physical defects and evaluate the effectiveness of different fault models for testing low-power static random-access memories (SRAMs), especially what concerns particular issues inside the memory cells cluster.
- to analyze automatic test pattern generation (ATPG) algorithms that use the cell-aware testing (CAT) approach to target together both common and cell-aware fault models and obtain the best tradeoff between fault coverage and testing time; furthermore, to evaluate and understand which flow may get more advantages in terms of fault coverage, test pattern sets have been fault simulated with fault lists belonging to common fault models, including CAT and delay fault models.

The first research topic has focused on the effect of particular resistive defects that may produce a fault in the device, especially when the SRAM switches stand-by low-power state to the normal operating state and vice versa. The second research activity has included a testing methodology and ATPG flows that have been presented to combine different fault models and increase the fault detection figures coming from different fault lists. Lastly, different fault models and designs have been used to generate different sets of defect-oriented test patterns to increase the overall quality of the test.

The first contribution of the PhD career is about the evaluation of the effect of each resistive defect in the low-power SRAM cell with back-bias circuitry. The most suitable fault model has been identified for each of the analyzed defects (depending on the resistance value) and then, the corresponding test aiming at identifying and detecting the fault has been evaluated. The study done has identified the key issues about which type of effect the analyzed defects change the resistance value until the cut-off values are produced. This has been useful to ensure a more reliable and efficient testing of low-power SRAMs.

Then, the second contribution includes the importance of cell-aware testing in identifying defects that are not easily detectable using traditional testing methods. By resorting to the research study done, it may be possibly demonstrated that cell-aware testing can significantly improve the accuracy and reliability of digital testing. At last, different fault models and designs have been used to generate different sets of defect-oriented test patterns. The obtained fault coverages derived from the fault simulation process of the generated patterns with different fault lists belonging to different fault models have been evaluated. The results have shown the different behavior of the analyzed circuits and the obtained fault coverage using the ATPG tool targeting a specific fault model is generally higher than the one obtained by using patterns generated for other fault models.

The study has also demonstrated that there are cases where the patterns generated for a given fault model achieve very good fault coverage when fault simulated with different fault lists. As a result, the presented observations may pave the way to develop optimized test generation strategies, able to reduce the test generation time and reduce the number of required test patterns while still achieving the same fault coverage.