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Wideband GaN digital class-E Doherty PA for sub-6 GHz 5G applications

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Research Paper

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Abstract

This work presents a GaN-based digital class-E Doherty power amplifier module for the 5G FR1 frequency band. The design integrates two identical class-E MMICs, driven by digital pulse-width-modulated signals, in a two-way wideband Doherty configuration. This configuration is co-optimized together with the class-E components of the amplifiers to achieve high efficiency over an extended output back-off range of up to 9 dB. At 7.5 dB back-off, the measured final-stage drain efficiency reaches 68% with a 3.4 GHz single-tone input. Across the (3.2–3.6) GHz band, the prototype maintains a minimum efficiency of 52% at 9 dB output power back-off, with a maximum saturated output power of 32.8 dBm. At 3.3 GHz, the module achieves efficiencies of 60% and 59% for 20 and 100 MHz digital OFDM signals with 9 dB peak-to-average power ratio, respectively.

Introduction

The power amplifier (PA) is a key component of the RF transmitter front-end, where high efficiency is critical for effective data transmission. The class-E PA [1] is a widely used switching-mode amplifier, capable in principle of achieving 100% efficiency at maximum saturated output power (P_{out}), with practical efficiencies of 80% in the sub-6 GHz range at Watt-level power [2, 3]. With the advent of 5G and 6G wireless systems, higher data rates and more complex modulation schemes with high peak-to-average power ratios (PAPRs) have emerged. This trend underscores the need for energy-efficient PAs capable of maintaining strong performance over a wide output power back-off (OBO) range of up to 9–12 dB.

Various combinations of class-E PAs have been explored in GaN technologies in the past to achieve high efficiency under back-off conditions. Configurations such as outphasing strategies [4, 5] have exhibited deep OBO up to 10 dB and OBO efficiency in the order of 50%, while Doherty configurations [6–8] have achieved back-off levels up to 8 dB OBO and OBO efficiency up to 60%. It is therefore of significant interest to continue the research in the field of power-combined class-E PA to achieve even higher efficiency at even higher back-off ranges.

The majority of the solutions reported in the literature employ analog RF signals at the input, while only a limited number utilize a digital input approach [4, 5]. Digital implementations offer greater flexibility and compactness, driving increased interest in fully digital transmitter and PA architectures [9]. The integration of Doherty back-off efficiency enhancement strategy [10] with the high-efficiency performance of class-E PAs with digital pulse-width-modulated (PWM) input driving remains largely unexplored in the literature. To the authors' knowledge, the PA presented here is the first example of a GaN-based digital class-E Doherty PA.

Preliminary results of this work were reported at EuMW 2025 and published in the conference proceedings [11].

Design process

Two identical digital class-E MMICs (monolithic microwave integrated circuit) [5], fabricated in the Ferdinand-Braun-Institut (FBH) 250 nm GaN-HEMT process, are combined off-chip in a two-way Doherty microstrip combiner to leverage class-E efficiency. A photograph of the fabricated module is shown in Figure 1.

Class-E MMIC

Figure 2 shows the photograph and corresponding schematic of the digital class-E PA chip used in this work, previously presented in [5], with an area of 1.71 × 1.18 mm^2.

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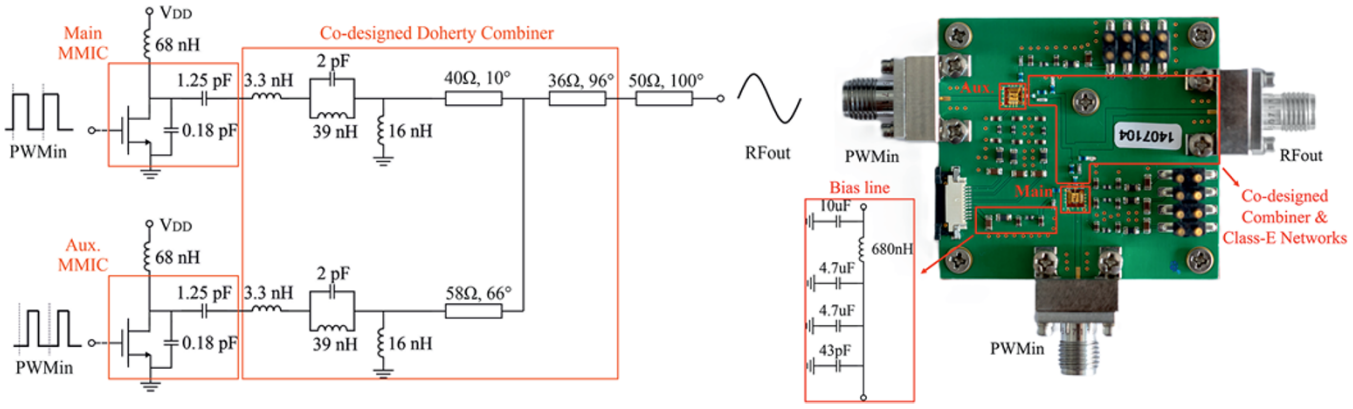


Figure 1. Fabricated digital class-E Doherty module: schematic (left) and photograph (right), showing two GaN PA MMICs and two class-E output networks with the co-designed Doherty combiner. Module size: 39×42 mm^2.

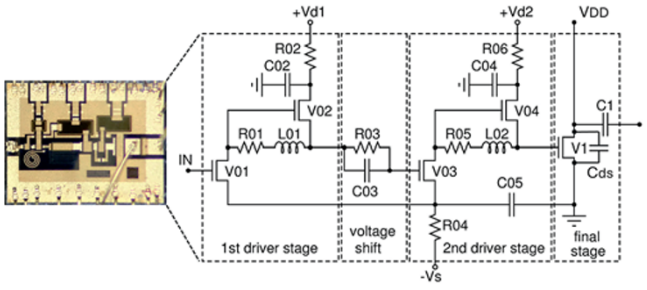


Figure 2. Photograph and corresponding schematic of the digital class-E GaN PA MMIC, area 1.71×1.18 mm^2 [5].

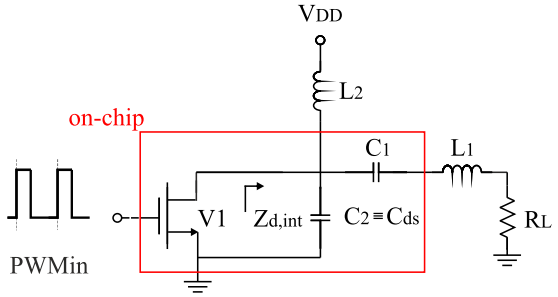


Figure 3. Ideal class-E PA with output matching network: MMIC on-chip components are highlighted.

The final stage employs a common-source GaN-HEMT device with dimensions of 8×62.5 μm (V1), preceded by two on-chip driver transistors (V01 and V03 in Figure 2). The drain-source capacitance (C_{ds}) of the final device is estimated to be 0.18 pF and provides the required class-E shunt capacitance. At the circuit output, a 1.25 pF series capacitor (C1) is integrated to form part of the class-E output matching network, whose remaining elements are implemented off-chip. The chip operates with three drain supply voltages: a 10 V supply for the final stage (V_{DD}) and two 5 V supplies for the driver stages (Vd1 and Vd2). To minimize the number of external supply lines, a voltage-shifting network composed of R03 and C03 is used. C05 provides RF blocking, while R04 damps the resonance formed by C05 and the bias bond wire. Likewise, R02 and R06 damp the resonances associated with C02 and C04 on the drivers' drain bias lines.

The nominal driving of the digital class-E chip is a PWM signal, which is applied directly to the gate of the first driver transistor (V01). This input controls the switching of V01 and consequently that of the following stages. The chip is switched ON by setting duty cycles different from 0%. In addition, a DC bias voltage of −10 V is applied at the input to set the gate operating point of V01. A shared negative bias (−Vs), typically set to −9 V, is applied to the sources of the driver transistors, ensuring that V03 has a sufficiently negative gate resting voltage. This biasing enables large gate swing excursions while maintaining the gate-source voltage (V_{gs}) within safe operating limits.

Figure 3 shows the ideal schematic of the class-E output network for the chip's final-stage transistor (V1 in Figure 1). After the initial component values are derived from Sokal's design equations [1], the maximum performance of the individual class-E MMIC is evaluated using load-pull simulations in a computer-aided design environment.

An input PWM excitation with variable duty cycle is used to analyze the optimum loads to be presented at the transistor intrinsic plane ($Z_{d,int}$) to achieve the desired power and the highest efficiency at full power and in back-off. In the next section, the selected loads for achieving Doherty load modulation are presented.

The on-chip driver stages (V01 and V03) consume approximately 2 W per chip, significantly affecting the overall efficiency. Since this work aims to demonstrate the effectiveness of the Doherty combining strategy rather than the absolute performance of the standalone digital class-E PA, the reported efficiency values exclude the driver-stage contribution. A chip redesign is underway to address this limitation.

Combiner design strategy

While the switching action of the class-E devices generates multiple harmonics at their drains, in the ideal class-E output network presented in Figure 3, C1 together with part of the inductance L1 forms a resonator tuned to the fundamental frequency [12], thereby attenuating the harmonics. As a first approximation, only the fundamental frequency reaches the load, thus allowing the application of the Doherty theory developed for linear amplifiers, namely based on the assumption that at the combiner's plane the current stimulus is sinusoidal and does not contain significant harmonic content [13]. Each PA and the output class-E section formed by (C1–C2, L1–L2) is modeled as an ideal single-frequency current

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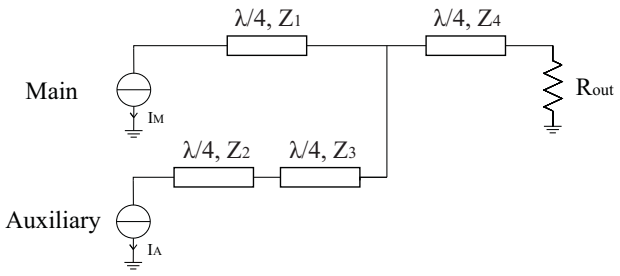


Figure 4. Generalized Doherty topology from [14].

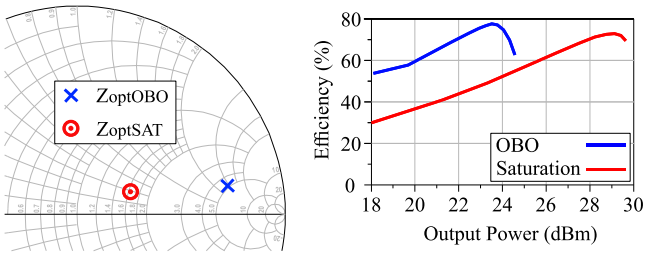


Figure 5. Chip-level circuit model simulated power-sweep performance at saturation (red) and OBO (blue). $Z_{opt,SAT}$ and $Z_{opt,OBO}$ are highlighted.

source, and the Doherty theory is applied at the "RL" plane. This section presents the combiner strategy and the selection of the required load impedances, based on ideal single-frequency driving currents (Figure 8(b)). The following section will describe how these driving currents are generated from PWM input signals with varying duty cycles.

The output combiner strategy from [14], shown in Figure 4, is adopted. To achieve OBO greater than 6 dB with devices of equal size and identical saturation currents, the generalized Doherty topology incorporates one quarter-wavelength transformer (QWT) in the Main branch, two QWTs with different characteristic impedances on the Auxiliary branch, and one QWT for post-matching. The lines' characteristic impedances Z_1, Z_2, Z_3, and Z_4 constitute the design space. The input variables for the design include the current ratio of the Main amplifier to the Auxiliary amplifier at saturation, defined as $\alpha = I_{aux,max}/I_{main,max}$, which is set to 1 in this study for equal maximum currents. The OBO level in linear units, denoted as β and defined in (1), is 0.35 for the 9 dB OBO case.

$$\beta = 10^{-\mathrm{OBO}/20} \tag{1}$$

The resulting design parameters are expressed in (2) as a function of R_{opt}, the optimum impedance of the Main amplifier at saturation:

$$\begin{aligned} Z_1 &= 1.8\,R_{opt}, \qquad Z_2 = 1.6\,R_{opt}, \\ Z_3 &= 1.5\,R_{opt}, \qquad Z_4 = 1.5\,R_{opt}. \end{aligned} \tag{2}$$

For the Main amplifier, given the impedance relation at OBO versus saturation (3), the estimation for the output power level at OBO versus saturation (4) can be derived. For the 9 dB OBO target, it results in a reduction of 4.5 dB in power level.

$$R_{opt,OBO} = \frac{1}{\beta} R_{opt} \tag{3}$$

$$P_{out,OBO} = \beta P_{out,sat} \tag{4}$$

Here, $R_{opt,OBO}$ is the optimum load impedance of the Main amplifier at OBO, while $P_{out,OBO}$ and $P_{out,sat}$ represent the output power of the Main amplifier at OBO and saturation, respectively.

Since the output power of a class-E PA reduces with the duty cycle [12, 15], the reduced output power levels and back-off behavior of the PA are investigated by applying reduced duty cycles at the input. The resulting optimum load at back-off is then verified to satisfy the relationship in (4). At the nominal V_{DD} of 10 V, the chip achieves a saturation power of 29 dBm with 70% efficiency on a (77 + j25) Ω load, using a 60% input duty cycle. The optimum load for OBO conditions is evaluated by applying duty cycles below 50%. With a 30% input duty cycle, the load-pull simulations indicate that 75% efficiency can be reached at 24 dBm output power, corresponding to 5 dB back-off, on a (230 + j150) Ω load.

Figure 5 shows the simulated performance of the chip under a swept duty cycle on the optimum loads obtained from load-pull, $Z_{opt,SAT} = (77 + j25)\,\Omega$ and $Z_{opt,OBO} = (230 + j150)\,\Omega$, at saturation and OBO, respectively. The resulting back-off power of 5 dB is sufficiently close to the required 4.5 dB value to satisfy (4).

Figure 5 shows that a single class-E PA can achieve a certain degree of back-off efficiency enhancement through load modulation. This work aims to demonstrate that a Doherty combination of class-E PAs enables larger back-off levels, on the order of 9 dB, which are more suitable for modern high-PAPR modulation schemes, while also being driven with digital PWM signals.

Figure 1 (left) shows the final implemented combiner together with the class-E output matching networks of each chip. The class-E output network configuration composed by (C1–C2, L1–L2) of Figure 3 is enhanced with the integration on-board of the SMD components (L3, C3) to form a resonator tuned to the second harmonic, in order to reduce the peak voltage across the transistor as demonstrated in [16]. The shunt SMD inductor L4 is introduced to enhance the design space for complex load synthesis.

The combiner strategy presented in [14] assumes purely real optimum load impedances, whereas the selected optimum loads for class-E operation at saturation and back-off are complex. The combiner lines' widths and lengths and the values of the off-chip SMD components (C3, L1–L4 in Figure 1) that constitute the class-E output matching networks for each chip have been co-optimized at circuit level. The co-optimization is performed to obtain the optimum loads at the intrinsic drain of the transistors as previously discussed. The final combiner layout deviates from the initial topology shown in Figure 4, with the two transmission lines in the Auxiliary branch merging into a single line and both the Auxiliary and Main branches being implemented with shorter transmission lines. An additional 50 Ω transmission line is inserted after the combiner solely to enable physical connection to the RF output launcher.

Figure 6 shows the load modulation performance over the (3.2–3.6) GHz bandwidth for the overall simulated module. The target saturation and back-off loads are effectively synthesized. The load modulation trajectories remain well-centered around the target loads across the entire bandwidth.

Figure 7 shows the 1-tone simulated output of the full digital class-E module across the (3.2–3.6) GHz bandwidth. The saturated output power (P_{sat}) exceeds 31.5 dBm with a variation within 0.5 dB.

The simulated gain exhibits an increasing behavior with output power, consistent with that reported in [5], due to the nearly constant input power of the pulse-driven-wave signal. Efficiency is above 65% at 7.5 dB OBO and above 62% at 9 dB OBO across the bandwidth, peaking at 68% at 9 dB OBO at the center frequency of 3.4 GHz.

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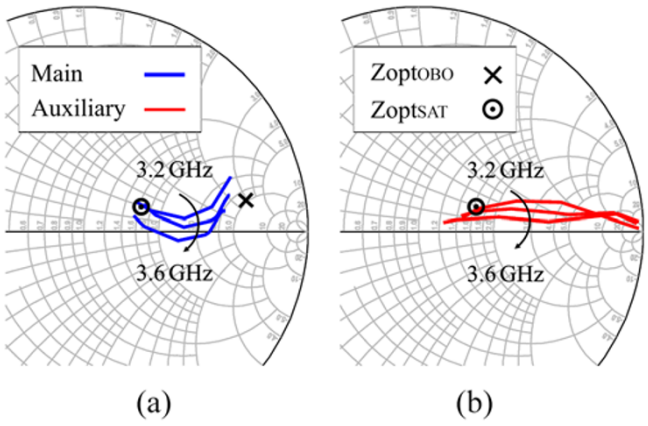


Figure 6. Load modulation trajectories for the Main (a) and Auxiliary (b) amplifiers over the (3.2–3.6) GHz bandwidth. Simulation of the full digital class-E module.

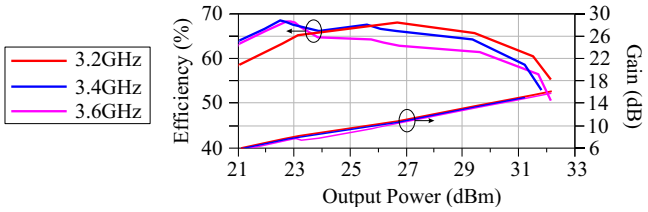


Figure 7. 1-Tone simulated output performance over the (3.2–3.6) GHz bandwidth of the full digital class-E module.

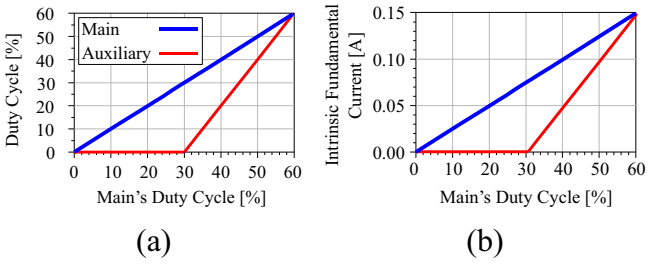


Figure 8. Driving duty cycles (a) and intrinsic fundamental currents (b) ideal target performance for the Main (blue) and Auxiliary (red) PAs.

Digital driving

In digital class-E amplifiers, varying the input duty cycle allows control of the drain current and output power [12, 15]. In this application, we assume that the fundamental component of the drain current increases linearly with the input duty cycle, analogous to the linear relationship observed in analog-driven PAs between the fundamental drain current and the input drive [17]. Furthermore, we assume that, in the ideal class-E configuration of Figure 3, the fundamental component of the drain current corresponds to the magnitude of the previously assumed single-frequency signal at the load RL, where the Doherty combination theory is applied.

For the implemented digital Doherty, the input duty cycles of the Main and Auxiliary PAs are adjusted to obtain the drain current profiles shown in Figure 8(b). The digital implementation allows precise control of the PA's turn-on and current ramp by adjusting the input duty cycle. As shown in Figure 8(a), the Main's duty cycle is set to increase from 0 to 60%. For the Auxiliary device, the duty cycle remains at 0% until the break point, which is located where the duty cycle of the Main reaches 30%, turning the chip on just after this point. It is then increased until the Auxiliary current matches the Main maximum current, as illustrated in Figure 8(b). Digital driving using PWM signals faces inherent limitations, as the minimum achievable duty cycle directly affects the output power dynamic range. Arbitrary waveform generators (AWGs) exhibit a finite time resolution of approximately 10 ps for the M8195A used in this work, limiting the generation of very narrow pulses. This corresponds to a practical duty-cycle resolution of approximately 5% at the design center frequency of 3.4 GHz. Further discussion of these limitations and possible solutions is provided in the following section.

Board integration

The module shown in Figure 1 (right) is fabricated on a 0.305 mm Rogers 4003C laminate. The board is mounted on a copper heatsink, and the complete demonstrator measures 39 × 42 mm^2. The two class-E MMICs are mounted in dedicated cutouts on the board, soldered to the copper carrier for common ground and improved heat spreading, and wire-bonded to the DC and RF lines on the PCB. Two RF connectors provide the digital PWM inputs (PWMin), one for the Main chip and one for the Auxiliary chip, each routed to its respective MMIC input via a 50 Ω transmission line.

As described in the "Class-E MMIC" section, each MMIC requires four bias lines: three for the drains of the two drivers and final-stage devices, and one for the negative source. The topology of one MMIC bias line is included in Figure 1. It features four decoupling capacitors, ranging from 43 pF to 10 µF, and a feeding inductor. The bias lines are connected to the DC supply via flat-top and pin-header connectors. At the chip outputs, the class-E output network is implemented as described in the "Combiner design strategy" section. The components C1 and C2 are integrated on-chip; L1 and L2 are partially implemented by the gold bond wires necessary to connect the chip to the board; where large values are necessary, high-precision SMD inductors are added on board. Following the class-E networks, the Doherty combiner, realized using microstrip lines, is connected to the RF output (RFout).

Characterization

The measurement setup uses a Keysight M8195A AWG to produce the two digital input signals. Two external broadband preamplifiers generate the minimum peak-to-peak input swing of 6 V required to drive the MMICs' final-stage transistors. Two bias-Ts are used to supply the gate bias for the first driver transistor, whose gate is directly connected to the PWM input, as shown in Figure 2. At the output, a 20 dB attenuator limits the power delivered to the Tektronix DPO70000SX real-time oscilloscope. All results presented in the following section are derived from the captured real-time waveform data, with power measurements validated using a Keysight UXA spectrum analyzer.

The following biasing conditions are applied: the final-stage device V_{DD} is set to 10 V, to match the load-pull simulation performance, while the driver's drain voltage is set to 5 V. The input gate bias, provided by the bias-Ts, is set to −10 V to allow large gate swing excursions as described in the "Class-E MMIC" section.

The system was calibrated to equalize the Main and Auxiliary input channels in both amplitude and phase. Nevertheless, a residual phase mismatch may remain at GHz operating frequencies. For

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this reason, a phase sweep was performed to identify the optimum phase shift between the Main and Auxiliary branches, resulting in an optimal phase difference of 40° for the co-optimized final circuit shown in Figure 1.

Because the effective gate bias varies with the input duty cycle, the DC level applied through the bias-Ts is dynamically adjusted during single-tone measurements via the remote PC controller to maintain a consistent operating point. This adjustment could not be implemented during modulated signal measurements, since the power supply is controlled via SCPI commands and cannot update the voltage setting on the required time scale. Future work will focus on integrating a GaN-based broadband driver PA with a dynamically adjustable voltage offset like [18] into the digital PA transmitter chain.

The module gain could not be measured due to setup limitations. All reported efficiency values correspond to the drain efficiency of the class-E final-stage transistor only, as the goal of this work is to illustrate the maximum potential of the back-off efficiency enhancement strategy achievable with optimized drivers. The efficiency calculations also exclude the power consumed by the preamplifiers.

1-Tone characterization

The digital Doherty PA has been first evaluated using single-tone PWM input signals to demonstrate the effectiveness of the proposed Doherty combining strategy. The back-off behavior is examined by applying reduced duty-cycle values to the input signals of the Main and Auxiliary chips, following the profiles illustrated in Figure 8.

Figure 9 compares the measured and simulated final-stage drain efficiency (η_{drain}) versus P_{out} at the center frequency of 3.4 GHz. The measured P_{sat} reaches 31.6 dBm, while efficiencies of 68% at 7.5 dB OBO and 61% at 9 dB OBO are achieved.

Comparing the original simulated results (Sim. no. 1) with the measured results (Meas.), a good agreement in the efficiency level is achieved at the back-off peak, while differences appear in the efficiency values throughout the OBO range up to saturation and in the achieved power back-off range. To address this discrepancy, an additional simulation (Sim. no. 2) is performed using a more accurate model of the MMIC output stage, adjusting the simulated values of the output series capacitor C1 and the bond wire connecting it to the board, simulated as L1. In particular, the exact inductance of the bond wires is difficult to determine, introducing some uncertainty in the model; based on measurements, the inductance per unit length is estimated to be approximately 1 nH/mm. The updated simulation provides a better estimate of the OBO efficiency peak, shifting it from 9 to 7.5 dB, while maintaining agreement with the measured OBO efficiency level of 68%.

Despite the improved agreement, a drop in the measured performance is still observed from medium output powers up to saturation. This discrepancy is partly attributed to the simulation approach: the results combine time-domain circuit-level simulations with Doherty combiner losses estimated from electromagnetic simulations. Direct time-domain simulations of the full electromagnetic circuit could be more accurate, but they have shown convergence problems. Furthermore, the board implementation faced grounding issues, which may have affected the measured performance. Overall, the results show that the proposed topology is capable of achieving high efficiency in simulations at 9 dB OBO, as demonstrated by Sim. no. 1 (Figure 9). Updated simulations and measurements confirm the effective achievement of the

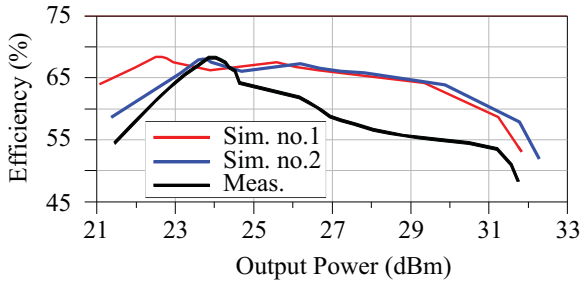


Figure 9. η_{drain} vs. output power performance @f_s=3.4 GHz with V_{DD} = 10 V: 1-tone measured (black) and simulated results with original (red) and improved (blue) MMIC's output section model.

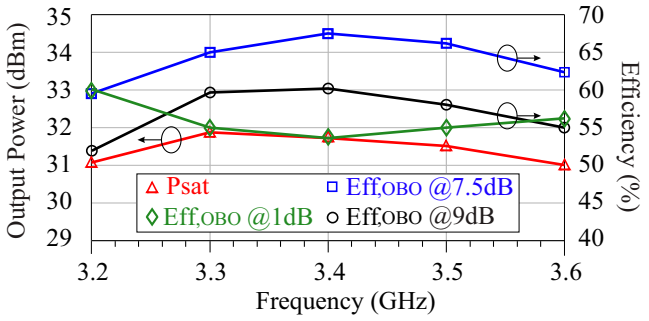


Figure 10. 1-Tone measured P_{sat} and η_{drain} at 1, 7.5, and 9 dB OBO performance with V_{DD}=10 V over the (3.2–3.6) GHz band.

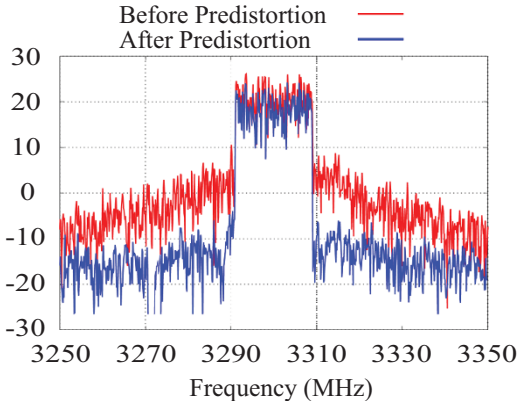


Figure 11. System-level characterization of 20 MHz, 9 dB PAPR OFDM signal @3.3 GHz before (red) and after (blue) DPD. After DPD, −31 dBc ACPR and 4.2% EVM were achieved, with 47% and 19 dBm average efficiency and average power, respectively.

Doherty efficiency enhancement in back-off, with characterized efficiencies of 68% at 7.5 dB OBO and 61% at 9 dB OBO.

The measured P_{sat} has also been characterized for higher V_{DD} values. At a V_{DD} of 12 V, the output power peaks at 32.8 dBm. Nevertheless, according to class-E theory, the maximum voltage swing across the transistor can reach 3.6 $\times V_{DD}$ at a 50% duty cycle [12]. To ensure the robustness of the module during testing, all measurements presented are performed at a V_{DD} of 10 V.

In the measurement setup used, the AWG has a finite time resolution of 16 ps that leads to the minimum duty cycle that was producing output power of about 5%. This corresponded to a characterized minimum output power of 21.5 dBm and 10 dB of output power dynamic range.

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Table 1. Comparison with state-of-the-art GaN class-E PAs

Ref.	Freq. (GHz)	BW (%)	P_{sat} (dBm)	η_{sat} (%)	η_{obo} (%)	OBO (dB)	A/D input	Impl.
[6]	2.14	/	46	75	61	6	A	DPA
[7]	2.9	14	43	73	50	6	A	DPA
[8]	3.6	11	48	50	54	7.5	A	DPA
[22]	2.0	10	33	60	40	6	D	PA
T.W.	**3.4**	**12**	**33**	**48**	**52**	**9**	**D**	**DPA**

One possible approach to overcoming these limitations in digital PWM-driven PAs is currently under investigation and is based on the subharmonic principle [19], already used in CMOS-based transmitters. In this approach, at low output power levels, the power devices are switched at a submultiple of the target center frequency, while the desired frequency is generated as a harmonic component of the switching waveform and selected by the filtering behavior of the class-E output network. Since the output is obtained from a higher-order harmonic of the switching signal, lower output power levels can be achieved.

The performance over the (3.2–3.6) GHz frequency range is also investigated using single-tone PWM input signals. Figure 10 shows the maximum output power and peak efficiencies for 1 dB, 7.5 dB and 9 dB OBO levels, across the bandwidth at a V_{DD} of 10 V. The saturated output power remains above 31 dBm with less than 1 dB variation over the bandwidth, while the minimum efficiencies achieved at 1, 7.5, and 9 dB OBO, respectively, are 54%, 59% and 52%. Overall, a minimum efficiency of 52% is maintained over the 9 dB OBO range and over a 400 MHz bandwidth, representing a record performance for a digital Doherty amplifier.

System-level characterization

Finally, the PA module is tested across the (3.2–3.6) GHz bandwidth using OFDM input signals with 9 dB PAPR. All input signals are generated using the digital modulator concept presented in [20], which employs an inline linearization technique that requires no additional power for digital predistortion (DPD). The best results are obtained at 3.3 GHz with a 20 MHz signal bandwidth, achieving 60% average efficiency and 21.6 dBm average power with −20 dBc ACPR. As shown in Figure 11, after linearization, the 20 MHz signal reaches −31 dBc ACPR and 4.2% EVM, though with reduced efficiency of 47% and output power of 19 dBm. At 3.3 GHz, also the 100 MHz bandwidth has been characterized, achieving 59% average efficiency and 21.4 dBm average power with −15 dBc ACPR, before DPD.

The linearity performance of −31 dBc achieved by the design remains below the −45 dBc 5G requirements for the targeted base-station application. In this design, Doherty back-off efficiency enhancement was prioritized over linearity, resulting in low selectivity of the class-E output resonator and degraded linearity. However, literature reports on both analog-driven Doherty [8] and digitally driven class-E PAs [21] demonstrating ACPR values of −45 dBc or better after linearization. This indicates that the observed linearity limitations stem from the specific implementation and that the presented architecture has potential to fulfill 5G linearity requirements.

From the system-level campaign, a drop in performance of over 10% in average efficiency and 2 dBm in power is apparent. The discrepancy is attributed to the physical limitations of the measurement test bench when used with the nominal digital input drive. Specifically, due to the limited time resolution (16 ps) of the AWG, some short pulses may be lost, and some may be incorrectly generated with reduced amplitude, reducing the total output power and affecting the efficiency. The application of the subharmonic principle [19] introduced in the "1-Tone characterization" section, by operating at a lower switching frequency, appears promising for mitigating the loss of short pulses and preventing the performance degradation observed when applying modulated signals. The application of this revised driving approach is planned for future work. Overall, the results nevertheless demonstrate the significant potential of the proposed digital class-E Doherty architecture for future 5G base station applications.

State-of-the-art comparison

The achieved performances are compared to the state-of-the-art of GaN class-E PA in Table 1. Both analog (A) and digital (D) input solutions are considered. Works [6–8] present Doherty implementations (Impl.) with analog input signals and microstrip combination techniques implemented on-board. Ref. [22] constitutes the only example of a digitally driven class-E PA, where a single class-E MMIC is wire-bonded to an off-chip tunable load matching network implemented with a varactor diode, achieving analogous power levels in the order of 33 dBm.

This work presents the largest OBO range of 9 dB, with 52% efficiency achieved on a comparable fractional bandwidth in the order of 10%. The comparison shows that the presented implementation is, to the best of our knowledge, the first digitally driven class-E Doherty PA and achieves the highest OBO performance among reported analog- and digital-driven class-E implementations.

Conclusion

This work proposes a GaN-based digital class-E Doherty PA designed for 5G sub-6 GHz applications, achieving peak single-tone performance of 68% drain efficiency at 7.5 dB OBO at 3.4 GHz and maintaining 52% drain efficiency across the (3.2–3.6) GHz band at 9 dB OBO. The compact module demonstrates significant potential for 5G base-station use, delivering efficiencies near 60% when driven with modulated OFDM signals up to 100 MHz bandwidth.

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