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Transitions in Multilayer PCB Technology for mmWave Low Loss Transmission Lines / Ballaera, S.G., Daniel Martinez Perez, J.. - ELETTRONICO. - (2025). (International Conference on Electromagnetics in Advanced Applications ICEAA 2025 Palermo (Ita) 08-12 September 2025) [10.1109/ICEAA65662.2025.11306048].

Publisher:
IEEE

Published
DOI:10.1109/ICEAA65662.2025.11306048

Transitions in Multilayer PCB Technology for mmWave Low Loss Transmission Lines

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***Abstract*—This paper presents a transition from coplanar waveguide to stripline capable of operating over the DC–67 GHz frequency range. The proposed structure is a vertical through-via transition, fabricated using PCB technology and designed for on-wafer probe measurements. Full-wave electromagnetic simulations have been performed to evaluate the S-parameters of both the single transition and a back-to-back configuration including a 30 mm stripline section. In the back-to-back configuration, the measured insertion loss is less than $2.2\,\mathrm{dB}$, while the return loss exceeds $20\,\mathrm{dB}$ across the entire frequency band of interest.**

***Index Terms*—Low-loss transmission lines, PCB, Coplanar Waveguide, Stripline, RF circuits, Transitions, Full-wave simulations, millimeter-wave**

I. INTRODUCTION

Nowadays, coplanar waveguide-to-stripline transitions in Printed Circuit Board (PCB) technology can be easily designed from DC up to 30 GHz. However, emerging microwave and millimeter-wave circuits require increasingly advanced transitions capable of functioning at higher frequencies. In addition, these transition should be fully compatible with standard PCB manufacturing technologies to avoid expensive fabrication costs.

The goal of this paper is to investigate and design a through-via transition from coplanar waveguide (CPW) to stripline in the DC-67 GHz frequency band. In this study, the following key objectives are addressed:

- Explore impedance matching techniques and vias design considerations to minimise signal reflections and impedance mismatches;
- Carry out electromagnetic simulations to verify the validity of the structure designed and perform optimisations.

To this end, an experimental design was developed to investigate the through-via transition from a coplanar waveguide to a stripline in a multilayer PCB. The stack-up was carefully configured with alternating signal and ground layers to minimize crosstalk and prevent unwanted resonances, ensuring stable signal integrity. The dimensions and spacing of the traces were meticulously determined based on the target impedance values for both the coplanar waveguide and the stripline, optimizing signal propagation. To further enhance performance, vias were strategically placed to minimize impedance mismatches and reduce parasitic effects. Additionally, via stub was optimized to mitigate signal degradation at higher frequencies. Grounded via fences were also considered to improve isolation. These design considerations are crucial for achieving efficient transitions in high-frequency PCB layouts, enabling seamless integration into advanced microwave and millimeter-wave circuits.

II. METHODOLOGY AND DESIGN

The electromagnetic simulation software Ansys HFSS was utilized to analyze the electrical characteristics of the CPW-to-stripline transition. The simulation model incorporates the PCB geometry, material properties, and transmission line configurations. The simulation employs the finite element method (FEM) to obtain impedance, insertion loss, return loss, and other relevant parameters. The stackup includes 8 layers planning to implement two different transitions on two different layers for a total width of 860 $\mu\mathrm{m}$, but only one of the two will be analyzed. Tachyon 100G was chosen as substrate material, which has a dielectric constant $\epsilon_r \simeq 3.02$ and a loss tangent $\delta = 0.0021$, which are very constant over the entire band and a wide temperature range of -55°C to +125°C. When working with laminates at high frequencies, it is essential to consider their similarities to a parallel plate waveguide loaded with dielectric material and open walls. We can assess its natural resonant frequencies to ensure that a high-frequency laminate is suitable for a particular frequency range. Such resonances arise between the upper and lower copper planes when the laminate is $\lambda/2$ thick at the operating frequency. It is best to avoid this resonance and weaker resonances at fractions of the 1/2 wavelength, such as 1/4 or 1/8 wavelength. A laminate thickness of 1/10 of the wavelength is a safe choice to prevent unwanted resonances. Considering a material with a dielectric constant of $\epsilon_r = 3.24$ at the frequency of $\mathrm{f_{MAX}}$= 67 GHz, the worst case for the chosen material, we obtain a maximum laminate thickness given by:

$$t = \frac{\lambda}{10} = \frac{c}{10\sqrt{\epsilon_r} f_{MAX}} = 249\mu m \qquad (1)$$

Moreover, following some preliminary tests with different sizes, a thin stack-up performs better and allows the creation of circuits with a smaller volume, so the thinnest possible stack-up was chosen. Once the stack-up has been determined, the next step is the realisation within it of the transmission lines of interest, i.e. CPW and stripline (Fig. 1). The two transmission lines are designed in order to have a characteristic impedance of 50Ω.

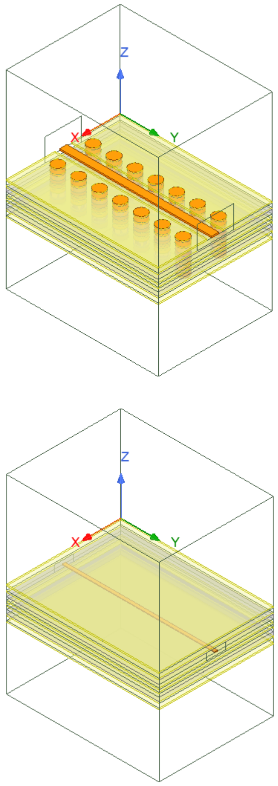

Fig. 1. CPW (top) and stripline (bottom) structures

Looking at the CPW structure, the presence of vias surrounding the signal line is evident, which connect the ground planes and provide enhanced isolation. The same technique can be applied to the stripline, and it will later be implemented for the stripline as well. These shielding vias also make it possible to reduce crosstalk, but they must be positioned appropriately. In fact, they create a kind of semi-closed resonant cavity that can also lead to a worsening of high-frequency cross-talk.

As observed in the resonance frequency analysis of the laminates within the stack-up, here we also calculate, as a first approximation, the half-wavelength value. This calculation accounts for the distance between the vias and the signal line, as well as the pitch between the vias.

To connect the two transmission lines, a through-hole via was chosen. This type of via penetrates the entire substrate, is easier and cheaper to fabricate, but terminates in an open-ended stub. The insertion of a via causes a discontinuity in the characteristic impedance, leading to signal reflection. This discontinuity is mainly due to the via's structure, which includes pads, anti-pads, and non-functional pads, introducing parasitic capacitances and inductances that significantly impact performance at high frequencies. To minimize these discontinuities, Time Domain Reflectometry (TDR) simulations were conducted, varying the catchpad, stub, and anti-pad sizes, as illustrated in Fig.2. Through TDR analysis, the optimal dimensions of the various parameters were determined.

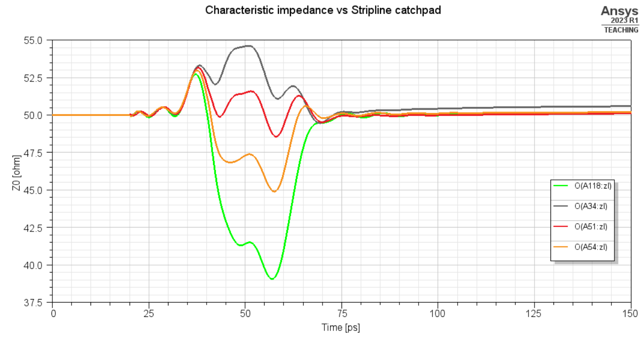

Fig. 2. Caracteristic impedance vs Stripline catchpad radius (grey = 200um, red = 250um, orange = 300um, green = 350um)

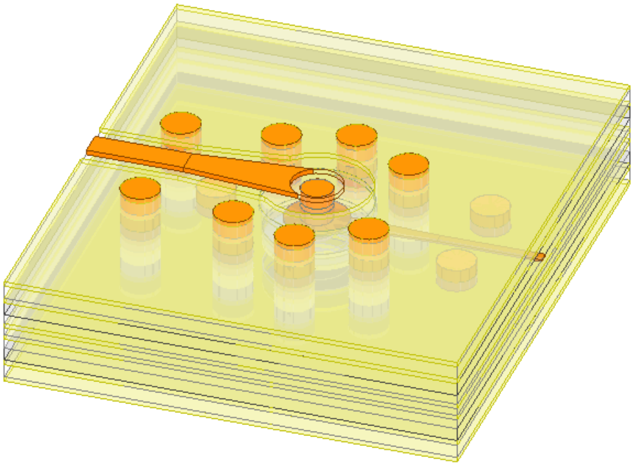

Fig. 3. Transition structure

The radius of all the vias is set to $125\,\mu\mathrm{m}$, the radius of the catchpad on the outer face is $200\,\mu\mathrm{m}$, while the one in the inner layer has a $250\mu m$ radius, finally the radius of the antipad is $400\,\mu\mathrm{m}$.

III. RESULTS

The final design of the CPW-to-stripline transition, highlighting the signal traces as well as the grounding and shielding vias, is shown in Fig. 3. The S parameters of the final transition are presented in Fig. 4. It can be observed that the return loss exceeds 24 dB across the entire band of interest, while the insertion loss remains below 0.3 dB.

A back-to-back configuration was then implemented in preparation for future fabrication, enabling experimental measurements. This configuration features a 30 mm long stripline and its S parameters are provided in Fig. 5. In this case, a return loss exceeding approximately 20 dB is observed across the entire band, while the insertion loss remains below 2.2 dB.

Table I presents a comparison between the state of the art and the proposed work. Various transitions have been reported, mainly through-via, realised on ceramic substrates (LTCC) or with classical PCB technologies. This comparison demonstrates that the transition introduced in this study performs quite well, despite its wide bandwidth.

TABLE I

COMPARISON OF STATE OF THE ART TRANSITIONS

	BW (GHz)	Structure	Technology	IL (dB)	RL (dB)
[1]	DC-9.8	Through-Via	PCB	<1.2	>8.7
[2]	76-81	Through-Via	PCB	<2.1	>10
[3]	2-18	Through-Via	PCB	<0.2	>19
[4]	57-67	Through-Via	LTCC	<1.72	>20
[5]	DC-100	Through-Via	LTCC	<2.49	>9.8
[6]	60-110	No Vias	LCP	<2	>13
This work	DC-67	Through-Via	PCB	<2.2	>20

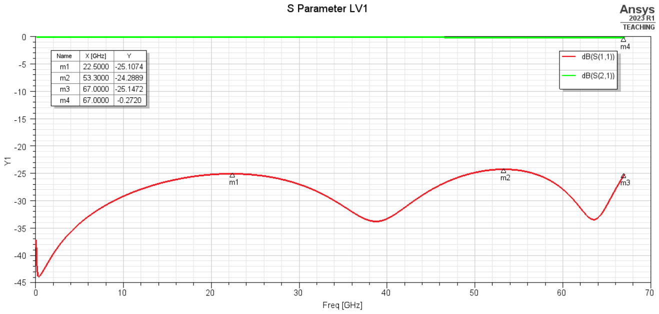

Fig. 4. Transition S parameters

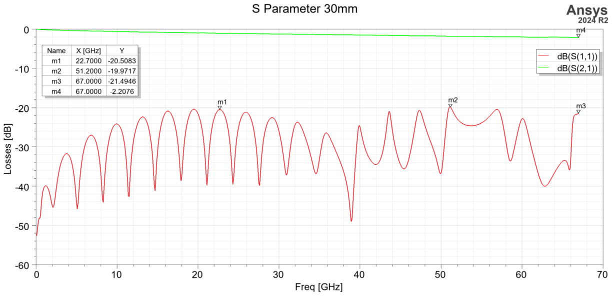

Fig. 5. S parameters B-to-B configuration with 30mm stripline

IV. CONCLUSIONS

A vertical through-via transition from coplanar waveguide to stripline capable of operating over the DC–67 GHz frequency range is designed. Full-wave electromagnetic simulations have been performed to evaluate the S-parameters

All the geometry requirements of the PCB elements, like the minimum vias diameter, the minimum spacing between signal lines and ground planes and the dimensions of pads and anti-pads are satisfied. The operating frequency band is DC-67 GHz as required with a return loss greater than 24 dB and an insertion loss less than 0.3 dB for the highest frequency.

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