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(Article begins on next page)

01 July 2026

Simulation study on the impact of miniaturization in 3 nm node 3D junctionless transistors

Luca Scognamiglio, Fabrizio Mo, Chiara Elfi Spano, Marco Vacca, Gianluca Piccinini

***Abstract*—Junctionless Nanosheet gate-all-around Field Effect Transistor (JL-NSGAAFET) is a promising technology characterized by the absence of any junctions between source-channel-drain. This absence allows to further scale down transistors while limiting short-channel effects. In this article, JL-NSGAAFET is explored as a potential candidate for the next 3 nm technology node through 3D TCAD simulations. First, we propose and simulate, through fabrication process simulations, a fabrication strategy for the JL-NSGAAFET compatible with the current manufacturing technology and based on the inversion mode NSGAAFET fabrication process. The high-k gate dielectric (HfO_2) and metal-gate technology (TiN) are also adopted in the fabrication process to enhance the electrostatic gate control over the channel for the n-type and p-type transistors. Then, we perform electrical simulations of the device by also including drift-diffusion model and quantum density gradient correction. We characterize the device in terms of electrical performance and compare with the conventional NSGAAFET. Furthermore, to investigate the impact of the device scaling on the unwanted short channel effects, we simulate and analyze the devices while varying the gate length (L_G) from 20 nm to 12 nm. Our reported simulation results prove that JL-NSGAAFET exhibits near-ideal subthreshold slope, low drain-induced barrier lowering (DIBL) and high on-to-off current ratio (I_{ON}/I_{OFF}) with superior advantages of greater drive currents and a simpler fabrication process because of the absence of junctions.**

***Index Terms*—density gradient, gate-all-around, junctionless, N3 logic technology, nanosheet, TCAD simulations, transistor, vertical stacked.**

I. Introduction

Nowadays, semiconductor devices play a huge role in digital and telecommunication technology. The shrinking of transistors becomes more difficult since more heat and power consumption indirectly increases while trying to achieve better performance [1]. The increasing demand for high integration density, high performance, and low power consumption can be achieved with 3D multigate structures such as FinFET and Nanosheet gate-all-around FET (NSGAAFET), thanks to better electrostatic control of the channel transport via fully surrounding the gate [2]–[7]. However, further challenges are emerging during fabrication processes in the next technology nodes when decreasing the size of the transistors. Moreover, as the channel length gets shorter, the electric field near the drain increases, thus reducing the gate electrostatic control. Because of the diffusion of dopants in silicon, the inversion-mode transistors are subjected to effective channel length variation. Difficulties arise in transistors when developing ultra-sharp source and drain junctions at the nanoscale due to the requirement of extremely high gradients in doping concentration [1]–[6], [8]. Junctionless transistor (JLT) is a promising technology since it has uniform doping concentration along source-channel-drain. Therefore, the effective channel length is equal to the physical gate length (L_G), when the transistor is turned on. By combining the JLT with the electrostatic gate control of multigate structures like gate-all-around (GAA), it is possible to obtain devices with improved short channel effects (SCEs) immunity and high performance in terms of ON/OFF current ratio (I_{ON}/I_{OFF}), while reducing SCEs, e.g., drain-induced barrier lowering (DIBL) [9].

In this paper, we investigate, through fabrication process simulations in Sentaurus TCAD suite [10], a novel fabrication strategy for junctionless NSGAAFET (JL-NSGAAFET) at the 3 nm technological node (N3) dimensions. The proposed fabrication process is fully compatible with the current manufacturing technology and presents significantly less complexity w.r.t. conventional ones. The obtained JL-NSGAAFET devices are then studied and characterized in terms of electrical performance. The simulations are validated through experimental results. Finally, we compare the performance of the JL-NSGAAFET with the one of the inversion mode NSGAAFET, to get a direct indication of performance w.r.t. the most recent and currently on-market technology. Our outcomes suggest further experimental studies based on the fabrication and testing of the proposed JL-NSGAAFET, to confirm the expected advantages of the proposed device.

II. Junctionless working principle

The JLT is essentially a gate-controlled resistor since there is no junction in the semiconductor material. The channel can be fully depleted when in off-state, due to the workfunction difference between the gate and the silicon channel. A gate voltage is required to modulate the carrier concentration inside the semiconductor channel, thus its conductivity [11]. When the JLT is turned off, the distance between the non-depleted source and drain regions can be larger than the physical gate length across the entire section of the device [12] - Fig.1 shows an example of n-type JL-NSGAAFET in OFF state. This is the feature that enables the reduction of the short-channel effects. The designer can control the depleted region

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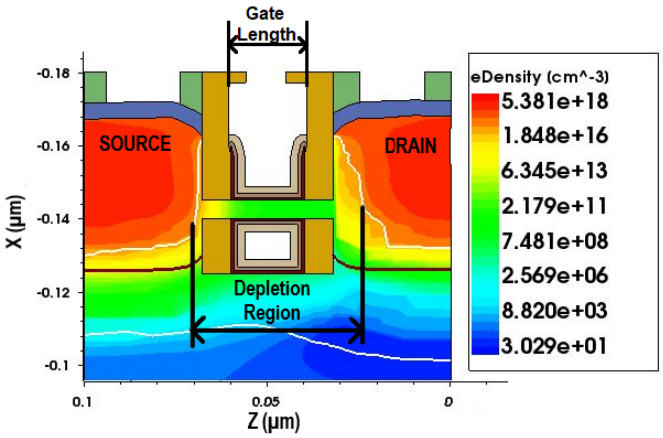

Fig. 1. Electron concentration along the channel of the n-type JL-NSGAAFET when V_{GS}=0 V and V_{DS}=0.75 V.

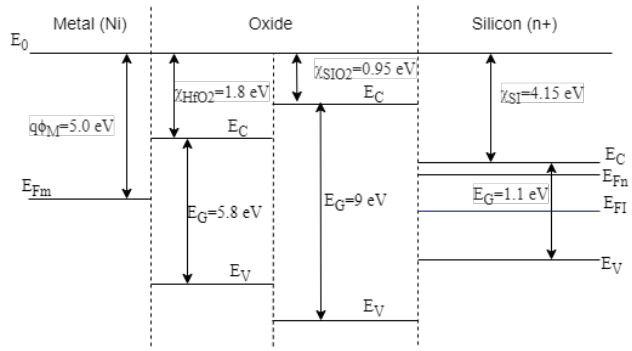

Fig. 2. Energy band diagrams of isolated materials n-type JLT.

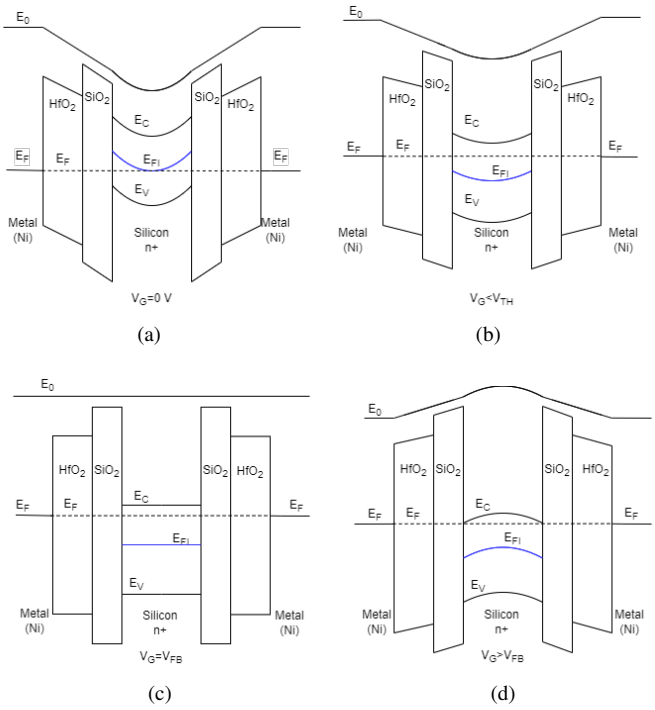

Fig. 3. Energy band diagrams for n-type JLT under different bias, for the conditions of: a) full-depletion (OFF state), b) partial depletion, c) flat-band (ON state) and d) accumulation.

extension by setting the width of the spacers (L_{SP}). Also, the stacked gate-all-around (GAA) structure enhances the electrostatic gate control over the channel, thus improving I_{ON}/I_{OFF}, subthreshold slope (SS), and DIBL [2], [13]. To understand how the channel is depleted of carriers when no gate voltage is applied, the energy band diagram of isolated materials for the n-type JLT is reported in Fig.2. The energy band diagrams include: E_F (Fermi energy), E_{Fm} (Fermi energy of the metal), $q\phi_M$ (metal workfunction), E_0 (vacuum level), χ_{Si} (electron affinity of silicon), χ_{SiO_2} (electron affinity of silicon dioxide), χ_{HfO_2} (electron affinity of hafnium dioxide), E_G (band-gap energy), E_{FI} (intrinsic Fermi energy), E_{Fn} (Fermi energy of n-type silicon), E_V (valence energy) and E_C (conduction energy).

At equilibrium, when contact is formed, a depletion region is formed in the channel region, due to the thin channel and the workfunction difference between the gate and the channel - Fig.3a. Moreover, the majority carriers (electrons) are pushed away from the surfaces, and the channel is depleted with the peak concentration in the center of the device [14], [15]. The region may be fully depleted or partially depleted, depending on the device parameters, such as doping and thickness of the silicon channel and the Fermi energy of the gate material. Since the source-channel-drain is uniformly doped n-type, a p-type metal workfunction is required. Instead, if the transistor is p-type, a n-type metal workfunction is needed.

When a positive voltage is applied to the gate electrode, the band bending declines and depletion width tends to decrease - Fig.3b. Therefore, current starts to flow through the bulk of the channel. If the voltage is further increased, the flat band condition is reached, and a completely neutral channel is created - Fig.3c. When the applied voltage crosses flat-band voltage (V_{FB}) - Fig.3d, charges accumulate in the surface of the channel. The current is governed by accumulation charges at the outer region of the channel [11], [16], [17]. As a result, the channel conduction for JLT goes from depletion to accumulation, differently from conventional MOSFETs, in which the conduction progress from depletion to inversion.

The band diagram along the source-channel-drain of the simulated JL-NSGAAFET structure has been extracted to show that the structure does not conduct when either no voltage is applied at contacts (Fig.4a) or when V_{GS}=0.75 V (Fig.4b). Once the gate voltage starts raising, charge carriers begin to flow from source to drain (Fig.4c).

The junctionless transistor behaves like a resistor when flat-band condition is met. Hence, at first approximation, the current for JLT is directly proportional to silicon thickness T_{si} and inversely proportional to gate length L_G when the onset of conduction is reached [11]. On the other hand, the current of inversion-mode transistors in saturation region is directly proportional to the gate oxide capacitance, carrier mobility μ, effective channel width and inversely proportional to L_G.

III. Device Structure and Simulation Model

We conceive and simulate the proposed stacked-NS JL structures in TCAD Sentaurus Process. The fabrication process is reported in Fig.6. We only rely on manufacturing processes that are currently employed for commercial inversion-mode

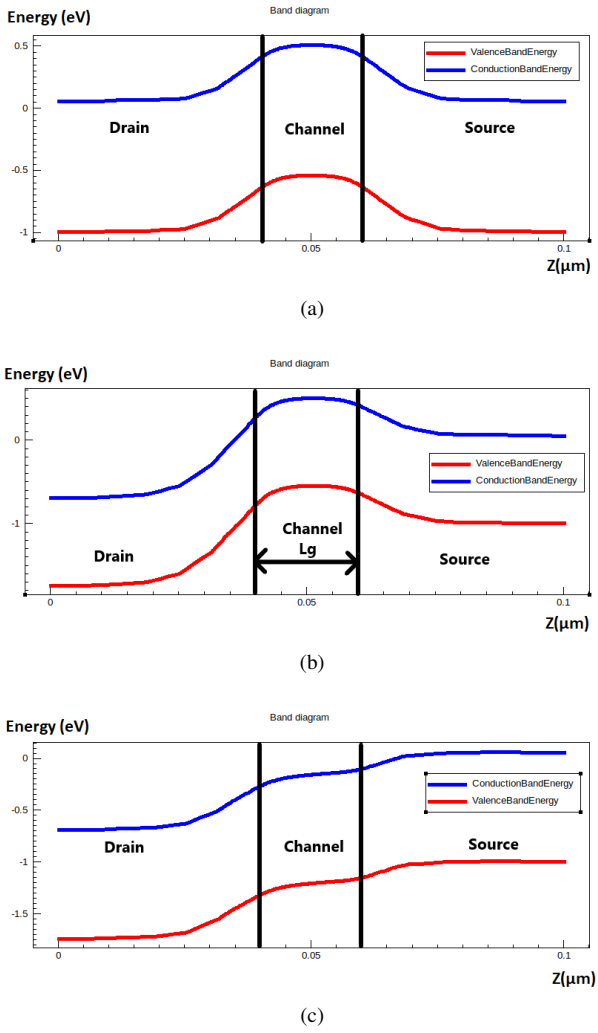

Fig. 4. Energy band diagrams along source-channel-drain of simulated n-type JL-NSGAAFET: a) V_{GS}=V_{DS}=0 V (OFF state), b) V_{GS}=0 V, V_{DS}=0.75 V (OFF state) and c) V_{GS}=0.75 V, V_{DS}=0.75 V (ON state).

stacked-NS, thus constituting an established technological framework [10], [18], [19]. The JL-NSGAAFET is built on a bulk substrate to keep the cost lower than what it would be with silicon-on-insulator (SOI) substrates. This enables to pursue large-scale production and further scalability, and corresponds to the approach of current commercial devices. The JL-NSGAAFET fabrication begins with the epitaxial growth of SiGe/Si multilayers. The fin is patterned using the Sidewall Image Transfer (SIT) technique to define the nanosheet width on the basis of the etching process parameters. After the fin formation, the well implantation is performed to block unwanted leakage current flowing along the silicon substrate, then shallow trench isolation (STI) process is performed. The exposed fin is doped with phosphorus (boron) to build the n-type (p-type) doped channel by ion implantation. The implantation is performed with a tilt angle of +10 degrees and -10 degrees to ensure adequate coverage of tall fins. Annealing is performed to activate the implanted dopants. However, the dopant redistribution caused by annealing will affect the doping concentration within the silicon channels. Dummy gates and spacers are then defined by etching the

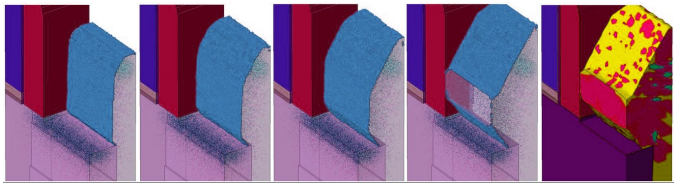

Fig. 5. Atomistic representation of the surface of the epitaxially source/drain growth simulated by LKMC [10].

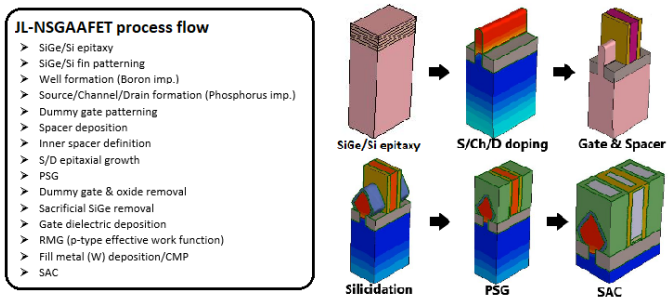

Fig. 6. JL-NSGAAFET (n-type) fabrication process simulation.

SiGe/Si layers. Contrary to what usually done, we build spacers to prevent short circuits between gate and source/drain regions. The inner spacers are formed to isolate the channels and further reduce parasitic. Source and drain regions are then epitaxially grown with an higher dopant concentration to exploit strain technology, thus enhancing the carrier mobility. Diamond-shaped source/drain contact are built using the fully atomistic model uses a lattice kinetic Monte Carlo (LKMC) method to simulate the silicon growth rate - Fig.5. This model includes orientation dependent solid phase epitaxial regrowth (SPER) and facet formation [10], [20], [21]. To improve the drive current without affecting the channel doping, an additional source and drain implantation is performed to limit the resistance of the contacts as reported in [22], [23]. Then, silicidation is performed to reduce contact resistivity. Furthermore, the phosphosilicate glass (PSG) is deposited on the structure as insulating layer. During the Replacement Metal Gate (RMG) process step, sacrificial layers (SiGe) located between channels are selectively removed. Gate stack is formed by a conformal SiO_2/HfO_2/TiN/W deposition. At last self-aligned contacts (SAC) are formed by isolating the top gate electrode with Si_3N_4, so that if any misalignment occurs during contact formation, short-circuits between gate and source/drain are prevented. The detail parameters for the device structure obtained with process simulation by tuning technological parameters are reported in Table I. Fig.7a and Fig.7c respectively presents a bird eye's view and cross-section of the resulting JL-NSGAAFET. The physical modeling of the 3D JL-NSGAAFET comprehends the silicon bandgap narrowing model that determines the intrinsic carrier concentration, and the density gradient model. The mobility model specifications take into account the carrier mobility degradation due to carrier scattering on ionized impurities, the carrier velocity saturation in high electric field, and the mobility degradation due to surface roughness scattering. The

bandgap narrowing model is activated due to the presence of doping according to the Slotboom model. Shockley-Read-Hall recombination with doping-dependent lifetime and band-to-band tunnelling are also included in the simulation [22], [24]. The current-voltage characteristics are obtained by solving a non-linear system of equations [10], [25], based on the joint solution of the Poisson equation (for the system electrostatics) and the continuity equations (electrons and holes, for the carrier transport):

$$\begin{cases} \nabla \cdot (\varepsilon \nabla \phi) = -q\,(p - n + N_D - N_A) \\ \nabla \cdot \overrightarrow{J}_n = qR_{net,n} + q\frac{\partial n}{\partial t} \\ -\nabla \cdot \overrightarrow{J}_p = qR_{net,p} + q\frac{\partial p}{\partial t} \end{cases} \tag{1}$$

where ε is the electrical permittivity, q is the elementary electronic charge, N_D is the concentration of ionized donors, N_A is the concentration of ionized acceptors, $R_{net,n}$ and $R_{net,p}$ are the electron and hole net recombination rate, respectively, $\overrightarrow{J}_n$ is the electron current density, $\overrightarrow{J}_p$ is the hole current density and n and p are the electron and hole density, respectively. Quantum-mechanical corrections are considered through the density gradient model for the specified carrier concentrations related to the type of the transistor [26]:

$$\begin{cases} n = N_C\ exp(\frac{-E_C + E_{Fn} + q\Lambda_n}{k_B T}) \\ \\ n = N_V\ exp(\frac{E_V - E_{Fp} + q\Lambda_p}{k_B T}) \end{cases} \tag{2}$$

where $\Lambda_i = \frac{\hbar^2}{6qm_i^*}\frac{\nabla^2\sqrt{i}}{\sqrt{i}}$, $i = n, p$, is the quantum potential (or Bohm's potential), accounting for the quantum-mechanical non-locality of carriers [27], $N_{C,V}$ are the conduction/valence band density of states, $E_{C,V}$ the conduction/valence band edges, $E_{Fn,p}$ the electron/hole quasi Fermi levels, k_B is the Boltzmann's constant, T the temperature. The model exploits the gradients of the carrier densities to describe carrier confinement by locally modifying the electrostatic potential through a non-local correction potential [27]. Since the quantum potential is a function of the carrier density gradients, it requires a self-consistent solution [10]. Thanks to this computational approach purely quantum mechanical features are naturally included in the solution of the system (1) when n and p are derived through (2).

TABLE I
JL-NSGAAFET DEVICE PARAMETERS

Parameters	Parameter Value	unit
Nanosheet height, H_{NS}	5	nm
Nanosheet channel gap, gap	5	nm
Nanosheet width, W_{NS}	18	nm
STI thickness	22	nm
Spacer length, L_{SP}	8	nm
Gate length, L_G	20	nm
Gate Stack		
Gate oxide (SiO_2)	0.7	nm
High-k dielectric (HfO_2)	1	nm
TiN	5.0	nm

We characterize the studied technology by extracting the most commonly used figures of merit: V_{TH}, SS and DIBL. I_{ON} is extracted to be the drain current (I_D) at gate voltage

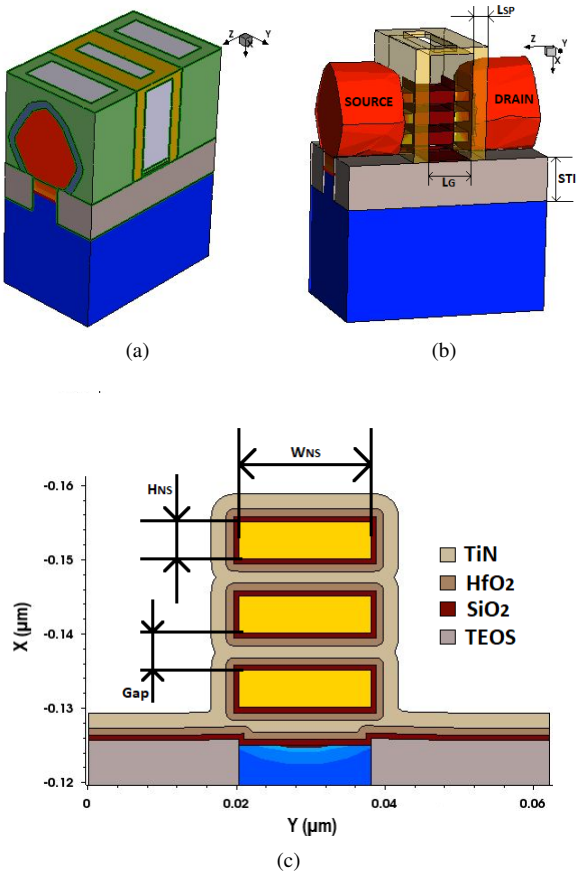

Fig. 7. (a) Bird's eye view of n-type JL-NSGAAFET structure. (b) Schematic view of the 3D structure. (c) Cross-section of JL-NSGAAFET with three-stacked channels.

$|V_{GS}|$=0.75 V and I_{OFF} is evaluated at V_{GS}=0 V [28]. Drain-induced barrier lowering (DIBL) is calculated according to the following equation as reported in [29]:

$$DIBL\left(\frac{mV}{V}\right) = -\frac{V_{TH(V_{D2})} - V_{TH(V_{D1})}}{V_{D2} - V_{D1}} \tag{3}$$

where $V_{TH(V_{D1})}$ is the threshold voltage estimated at low drain voltage (V_{D1}); $V_{TH(V_{D2})}$ is the threshold voltage when the drain voltage is equal to the supply voltage (V_{D2}=V_{DD}).
Subthreshold slope (SS) is defined as the inverse of logarithmic slope of the drain current versus gate voltage below threshold, as reported in [29]:

$$SS = \left(\frac{d\log_{10}(I_D)}{dV_{GS}}\right)^{-1} \tag{4}$$

Finally, we compare the proposed junctionless technology with the existing NSGAAFET one. To do that the main figures of merit of the two different technologies with the other papers available in the literature, the I_{ON} and I_{OFF} are reported in µA/µm and nA/µm, respectively. The transistor width considered are the effective width W_{eff}=3×(2H_{NS}+2W_{NS}) and the total width W_{si}=W_{NS} for the inversion mode and junctionless transistors, respectively. This is done because in conventional transistors, current flows at the outer region of the channel, whereas in junctionless devices, carriers populate the entire

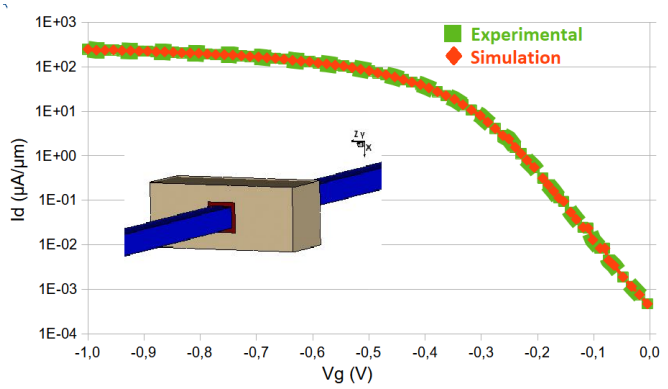

Fig. 8. Calibration of TCAD simulation models with the experimental results of thin film transistors [32].

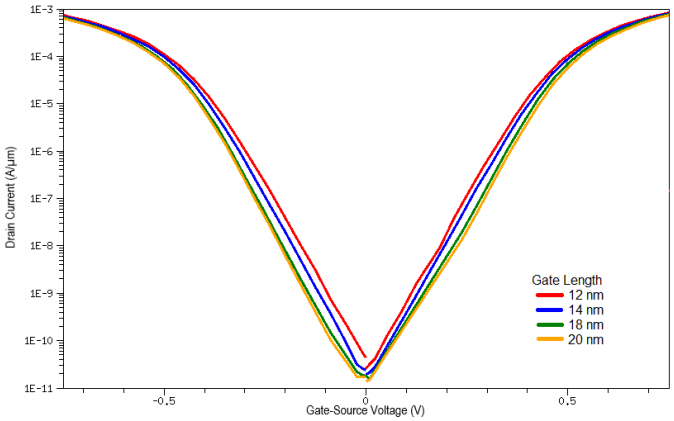

Fig. 9. I_D/V_{GS} of three-stacked channels JL-NSGAAFET at V_{DS}=$|0.75|V$ with different channel L_G=[20, 18, 14, 12] nm.

section of the silicon channel. Therefore, for fair comparison, the I_D/V_{GS} characteristics for JL-NSGAAFETs are expected to be divided by the width of each silicon channel to be reported in μA/μm, while the transcharacteristic of NSGAAFETs are divided by the perimeter of each nanosheet.

IV. Simulation Results and Discussion

To validate the modeling approach and the methodology presented in section III, the simulations are calibrated using experimental data from the literature. The single fabrication process steps were implemented to reproduce the literature and experimental results in [4]–[6], [30], [31]. The proposed fabrication process is thus composed by a sequence of validated process simulations. Furthermore, the electrical performance are calibrated to match the on reported in [32] (thin-film JLT). Fig.8 reports the comparison between the simulated and experimental characteristics. The simulation framework can accurately predict the device behavior, with a maximum error of 7.37%, thus we assume the proposed methodology is validated. In the following subsections, we present and discuss the obtained simulation outcomes.

A. JL-NSGAAFET

Fig.9 and 10 report the electrical characteristics of the investigated JL-NSGAAFETs, for different gate length values. Table II and III report the figures of merit extracted from the plots in Fig.9 and Fig.10. The studied JL-NSGAAFET presents good n-type and p-type transcharacteristics symmetry, with a competitive I_{ON}/I_{OFF} ratio of the order of 10^6-10^7. The n-type JL-NSGAAFET shows a drain current of 256.44 μA/μm, while the p-type one has the I_{ON}=-183.45 μA/μm at V_{GS}=$|0.75|V$ for the L_G=12 nm. To obtain the aforementioned values of I_{ON}, the channel concentration is set to 5×10^{18}cm^{-3}, to lower the semiconductor resistance at conduction onset. The n-type transistors have better on-state performance w.r.t. the p-type for all devices since the electron mobility is higher than the hole one. However, the formation of a semiconductor layer that is thin and narrow is needed to allow for full depletion of carriers to turn off the device [11]. Since the metal gate workfunction is $q\phi_{TiN}$=4.66 eV, the depletion of carriers for the p-type JL-NSGAAFET is worsened. Indeed, the n-type and p-type V_{TH} at L_G=12 nm is 0.45 V and -0.35 V, respectively. Therefore, the leakage current (I_{OFF}) extracted from the plots for the p-type device is higher.

B. Three stacked channels JL-NSGAAFET

The feasibility and the I_D/V_{GS} of three vertical stacked nanosheets in junctionless mode is analyzed in Fig.9. The saturation current is improved by setting the dopant concentration within the junctionless devices to better control the dopant redistribution, while adjusting the total width W_{si}=$3W_{NS}$. The channel concentration is set up to 5×10^{18}cm^{-3} to allow the depletion of the three-stacked channels when the transistor is switched off. The raised source and drain contacts have an active doping concentration of 1×10^{21}cm^{-3} to limit the resistance and provide higher I_{ON} and avoid the spreading of dopants during diffusion. The dopant implantation is tuned to have a carrier concentration of 2×10^{18}cm^{-3} in the channel. The I_{ON} is improved by 69% and 75% for n-type and p-type JL-NSGAAFET (L_G=12 nm), respectively - table III.

The three-stacked JL-NSGAAFET can achieve on/off current ratios of 10^7 for gate length of 12 nm, with a supply voltage of $|0.75|$ V. For all the considered channel lengths, the JL-NSGAAFET threshold voltage varies of about 30 mV. A symmetric V_{TH} is obtained because of the controlled dopant concentration employed for the n-type and p-type transistors, combined with the TiN gate workfunction ($q\phi_{TiN}$=4.66 eV). Moreover, the threshold voltage difference for the p-type JL-NSGAAFET between the single channel and the three-stacked one due to the diffusivity difference between boron and phosphorus. Dose, implantation and annealing are kept constant during process fabrication steps to have a comparable concentration within the structure throughout the simulations. The three-stacked devices result in more robust w.r.t. doping profile variations and threshold voltage differences between p-type and n-type. To decrease the I_{OFF}, the dose implanted in the simulated structure has been decreased, so that the channel concentration is about $7\times10^{17}-3\times10^{18}$ (table IV). Since the amount of carrier concentration is lower, a higher electrostatic gate control is achieved, hence the I_{ON}/I_{OFF} is increased. However, I_{ON} is decreased, due to channel resistance increase.

TABLE II
DC PARAMETERS EXTRACTION FOR JL-NSGAAFET HAVING DIFFERENT CHANNEL LENGTHS (SINGLE CHANNEL CASE)

Parameters	JL-NSGAAFET							
	NFET	PFET	NFET	PFET	NFET	PFET	NFET	PFET
L_G (nm)	12		14		18		20	
V_{TH} (V)	0.43	-0.35	0.43	-0.35	0.43	-0.36	0.43	-0.36
I_{ON} (μA/μm)	256.44	-183.45	228.61	-171.88	230.63	-170.14	222.26	-163.50
I_{OFF} (nA/μm)	3.80	-34.12	3.27	-22.19	2.43	-20.91	2.05	-8.81
I_{ON}/I_{OFF}	6.75×10^7	5.38×10^6	7.00×10^7	7.75×10^6	9.50×10^7	8.14×10^7	1.08×10^8	1.86×10^7
SS (mV/dec)	63.28	66.50	63.07	65.63	61.90	63.90	61.52	62.91
DIBL (mV/V)	22.01	31.70	21.35	29.41	17.71	28.85	16.62	20.60

TABLE III
DC PARAMETERS EXTRACTION FOR THREE-STACKED CHANNELS

JL-NSGAAFET having different channel lengths.

Parameters	Three-stacked channels JL-NSGAAFET							
	NFET	PFET	NFET	PFET	NFET	PFET	NFET	PFET
L_G (nm)	12		14		18		20	
V_{TH} (V)	0.45	-0.43	0.46	-0.44	0.47	-0.45	0.48	-0.45
I_{ON} (μA/μm)	835.97	-727.25	809.87	-690.06	782.62	-657.53	744.93	-640.28
I_{OFF} (nA/μm)	25.48	-43.90	19.14	-23.25	18.35	-18.18	14.24	-17.30
I_{ON}/I_{OFF}	3.28×10^7	1.66×10^7	4.23×10^7	2.97×10^7	4.27×10^7	3.62×10^7	5.23×10^7	3.70×10^7
SS (mV/dec)	67.29	68.10	63.37	65.59	62.94	63.22	62.69	62.66
DIBL (mV/V)	22.64	32.92	21.77	31.79	20.28	28.37	19.48	27.65

TABLE IV
DC PARAMETERS EXTRACTION FOR THREE-STACKED CHANNELS JL-NSGAAFET WITH LOWER DOPING CONCENTRATION.

Parameters	Three-stacked channels JL-NSGAAFET							
	NFET	PFET	NFET	PFET	NFET	PFET	NFET	PFET
L_G (nm)	12		14		18		20	
Channel doping (cm^{-3})	$1 \times 10^{18} - 3 \times 10^{18}$		$9 \times 10^{17} - 3 \times 10^{18}$		$8 \times 10^{17} - 2 \times 10^{18}$		$7 \times 10^{17} - 2 \times 10^{18}$	
V_{TH} (V)	0.44	-0.42	0.45	-0.42	0.46	-0.43	0.47	-0.44
I_{ON} (μA/μm)	238.88	-234.66	233.39	-227.84	231.90	-222.79	226.38	-217.10
I_{OFF} (nA/μm)	6.33	-7.25	4.25	-5.38	2.66	-3.45	2.25	-3.00
I_{ON}/I_{OFF}	3.77×10^7	3.23×10^7	5.50×10^7	4.24×10^7	8.72×10^7	6.46×10^7	1.00×10^8	7.24×10^7
SS (mV/dec)	64.66	67.80	63.58	64.09	62.23	63.02	61.84	61.97
DIBL (mV/V)	21.34	30.69	20.63	28.58	19.64	25.51	18.36	23.79

C. JL-NSGAAFET vs NSGAAFET

Fig.10 reports the electrical characteristics of the investigated JL-NSGAAFET, and of the inversion mode NSGAAFET, for different gate length values. Table II and V report the figures of merit extracted from the plot in Fig.10. To have a fair comparison, we keep unvaried all the other critical dimensions and processing conditions, so that the only difference lies in the channel length. As L_G gets shorter, I_{ON} increases and threshold voltage (V_{TH}) is lowered. This matches the theoretical expectations presented in [33]. The current-voltage characteristics of JL-NSGAAFET are very similar to those of a conventional MOSFET, as reported in Fig.9 and Fig.10. Moreover, the more L_G is down-scaled, the more the difference between electrical performance decreases, in terms of I_{ON}/I_{OFF} and DIBL of junctionless and inversion-mode NSGAAFETs, in agreement with the results in [34]. The junctionless devices can achieve high I_{ON}/I_{OFF}, thus demonstrating the fact that turning off the device by electrostatically depleting the channel of carriers works better than using a reverse-bias junction, as expected from [11], [34]. The JL-NSGAAFET device behaves like a resistor when the device is ON since the workfunction difference between silicon and metal gate can effectively deplete the channel, as shown in Fig.1. Although SS is slightly degraded as L_G gets shorter, it is still below 67 mV/dec at L_G=12 nm. From our results, the JL-NSGAAFETs have better SS and DIBL than the corresponding

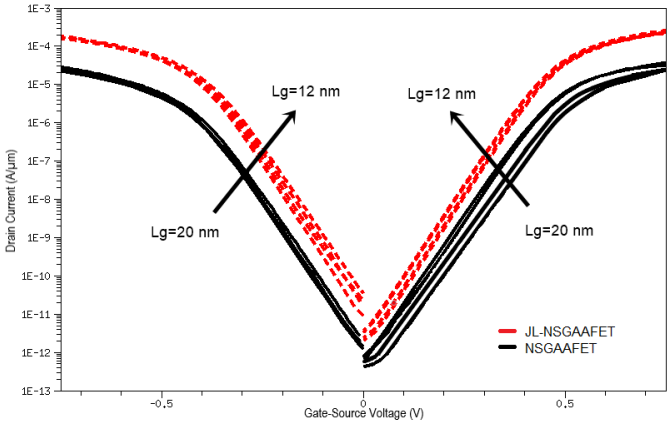

Fig. 10. I_D/V_{GS} characteristic of three-stacked channels NSGAAFET and a single channel JL-NSGAAFET at V_{DS}=|0.75|V with different channel L_G=[20, 18, 14, 12] nm.

TABLE V
DC PARAMETERS EXTRACTION FOR NSGAAFET HAVING DIFFERENT CHANNEL LENGTHS.

Parameters	Three-stacked channels NSGAAFET							
	NFET	PFET	NFET	PFET	NFET	PFET	NFET	PFET
L_G (nm)	12		14		18		20	
V_{TH} (V)	0.43	-0.38	0.44	-0.38	0.45	-0.39	0.45	-0.39
I_{ON} (µA/µm)	37.59	-28.29	31.24	-24.54	24.98	-23.10	23.52	-23.01
I_{OFF} (nA/µm)	0.77	-4.98	0.73	-3.06	0.72	-1.40	0.43	-1.22
I_{ON}/I_{OFF}	4.86×10^7	5.68×10^6	4.27×10^7	8.01×10^6	3.45×10^7	1.65×10^7	5.01×10^7	1.88×10^7
SS (mV/dec)	74.60	77.09	74.45	76.18	73.90	75.59	73.38	74.04
DIBL (mV/V)	41.02	47.16	35.16	46.97	34.30	39.26	30.27	35.40

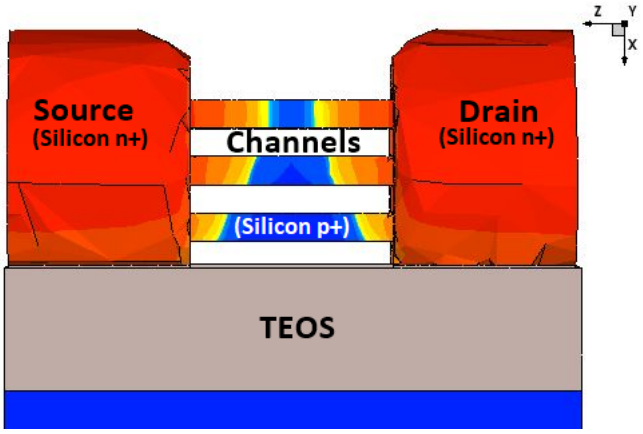

Fig. 11. Lateral view of the n-type NSGAAFET simulated.

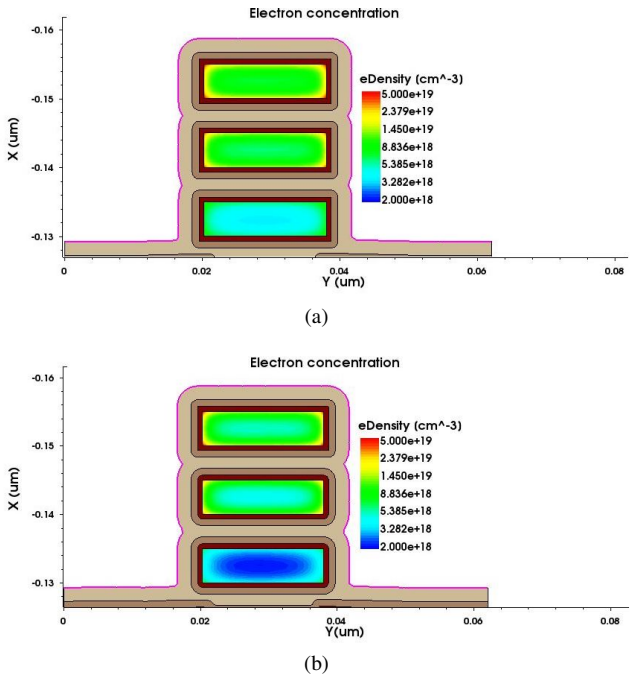

Fig. 12. Comparison of electron density of n-type (a) JL-NSGAAFET and (b) NSGAAFET. when V_{GS}=V_{DS}=$|0.75|V$.

inversion-mode FETs, thanks to the considered fabrication process. Indeed, rapid thermal annealing (RTA) is performed to electrically activate the dopants - RTA is accounted for thanks to Sentaurus process simulations. However, in junction-based FETs, the RTD leads to an uncontrolled lateral diffusion of dopants in the channel, thus affecting the effective channel length of the transistor - Fig.11. In turn, the dopant diffusion leads to relevant doping fluctuations at the nanoscale, affecting tremendously the threshold voltage and compromising its performance. In addition, as the V_{DS} is increased, the depletion region of the p-n junction between the drain and body increases in size and extends under the gate, so that the gate can control less effectively the charge in the channel, due to the reduction of the energy barrier near the drain electrode. As a toll to pay, the JL-NSGAAFETs have higher carrier concentration - Fig.12, and the carrier mobility is lower w.r.t. the inversion mode NSGAAFET - Fig. 13.

V. CONCLUSION

In this work, the JL-NSGAAFET has been analyzed through TCAD simulations, to investigate its potentiality for the future 3 nm technological node. JL-NSGAAFETs of different channel lengths were considered, designed, and characterized in terms of electrical performance. The adopted fabrication process steps for the junctionless devices are compatible with the current manufacturing technology, opening the way toward hybrid integration of inversion mode and JL technologies. The absence of junctions between channel and S/D allows to simplify the process steps required to fabricate transistors at the nanoscale, by avoiding the S/D extension implantation steps. The proposed device with uniform doping is not affected by leakage current due to lateral diffusion of dopants from source/drain contacts into the channel. The data extracted from the electrical characteristics obtained using TCAD simulations prove that the JLTs have a near-ideal subthreshold slope, low DIBL and high I_{ON}/I_{OFF}. Our outcomes motivate future research efforts in the fabrication and experimental verification of the proposed fabrication strategy and JL devices, being a promising technology to pursue the More-Moore paradigm of integration. In addition, we believe the investigation of new gate and semiconductor materials may ameliorate the junctionless transistor, enabling a more efficient channel depletion with improved performance.

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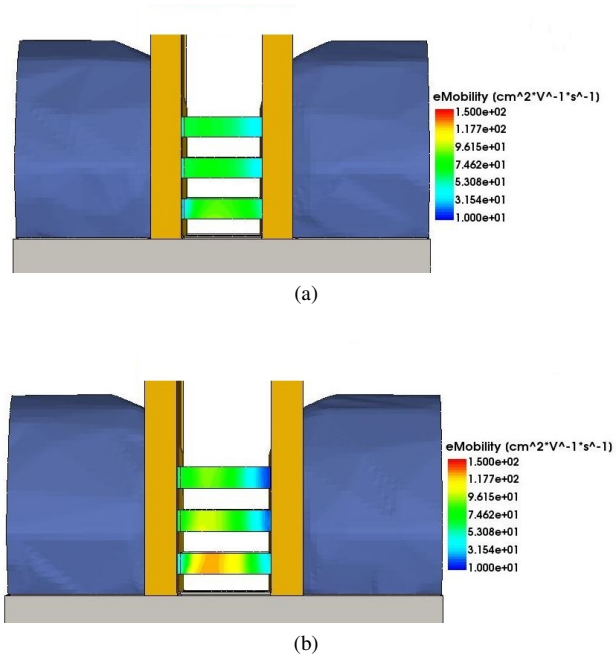

Fig. 13. Comparison of electron mobility of n-type (a) JL-NSGAAFET and (b) NSGAAFET, when V_{GS}=V_{DS}=$|0.75|V$.

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