AI-Based Optimization of a DC-DC Buck Converter Control Network Across DCM and CCM Operating Region

This is the author's version of the article that has been presented at IEEE ISCAS2025
The editorial version of the paper is available at http://dx.doi.org/10.1109/ISCAS56072.2025.11043707

AI-Based Optimization of a DC-DC Buck Converter Control Network Across DCM and CCM Operating Region

Lorenzo Nikiforos*, Giuseppe Gabriele¶, Francesco Gabriele*, Luciano Prono*,
Fabio Pareschi*,‡, Riccardo Rovatti†,‡, Gianluca Setti§,‡
* DET – Politecnico of Torino, corso Duca degli Abruzzi 24, 10129 Torino, Italy.
email: {lorenzo.nikiforos, francesco.gabriele, luciano.prono, fabio.pareschi}@polito.it
‡ ARCES – University of Bologna, via Toffano 2/2, 40125 Bologna, Italy.
¶ IDLab Ghent university – imec, Technologiepark Zwijnaarde 126, 9052, Gent, Belgium email:giuseppe.gabriele@ugent.be
† DEI – University of Bologna, viale Risorgimento 2, 40136 Bologna, Italy. email: riccardo.rovatti@unibo.it
§ CEMSE, King Abdullah University of Science and Technology (KAUST), Saudi Arabia. email: gianluca.setti@kaust.edu.sa

***Abstract*—In this paper we propose an automatic controller design methodology for DC-DC converters that comprehensively addresses both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). This methodology leverages on Artificial Intelligence (AI) techniques. Specifically, we resort on the Genetic Algorithms (GA) and Particle Swarm Optimization (PSO) methods. Both GA and PSO permit to optimally tune the component values employed in the compensation network, overcoming the limitations of traditional design methods. The latter focus indeed solely on CCM, leading to significant performance degradation in DCM operation. The proposed methodology can be seamlessly integrated into DC-DC converter design phase, and it is not restricted for specific DC-DC topologies or control architectures. As a case study, we apply the proposed approach to the design of a Type-III compensation network in a voltage-mode controlled Buck converter, aiming to improve the load-transient response. The optimization process is carried out in MATLAB. Then, a performance comparison with the conventionally designed controller is conducted via SIMPLIS simulations. An improvement in overall performance is demonstrated.**

***Index Terms*—Artificial Intelligence, Metaheuristic Algorithms, PWM DC-DC Converters, Small-Signal Models**

I. Introduction

Modern Pulse-Width Modulated (PWM) DC-DC converters must comply with the even tighter requirements of accurate output voltage level and dynamic performances regardless of the presence of exogenous disturbances. To achieve these aims ensuring system reliability, closed-loop control is thus essential. A typical scenario is shown in Fig. 1(a), representing a Voltage-Mode Controlled (VMC) Buck converter, where the controller stage is synthesized through a type-III compensation network. Its design is based on the availability of a Linear Time-Invariant (LTI) small-signal model for the converter, ensuring closed-loop system stability and adequate dynamic performances [1]–[5]. Nonetheless, the analytical structure of the model changes depending on whether the converter operates in Continuous-Conduction Mode (CCM) or Discontinuous-Conduction Mode (DCM) [5]–[7]. For standard control topologies, the design of the compensation network is usually performed only focusing on the CCM [8]–[10]. Therefore, both the stability and dynamic performances requests are well-satisfied by-design in CCM, while a performance degradation is expected in DCM due to significant changes in the converter dynamics [5], [6]. However, addressing the design of a controller employed in a DC-DC converter that operates both in CCM and DCM regions at once is not feasible in closed-form analytical solution.

The aim of this paper is to apply Artificial Intelligence (AI) techniques to assist and automate the design of a type-III compensation network employed in a VMC Buck converter. Although some studies in the literature demonstrate the usefulness of AI applications for power electronics applications [11] and, specifically, in the design of a DC-DC controller stages [12], [13], they typically leave out the converter operation in DCM and only focus on CCM. In this

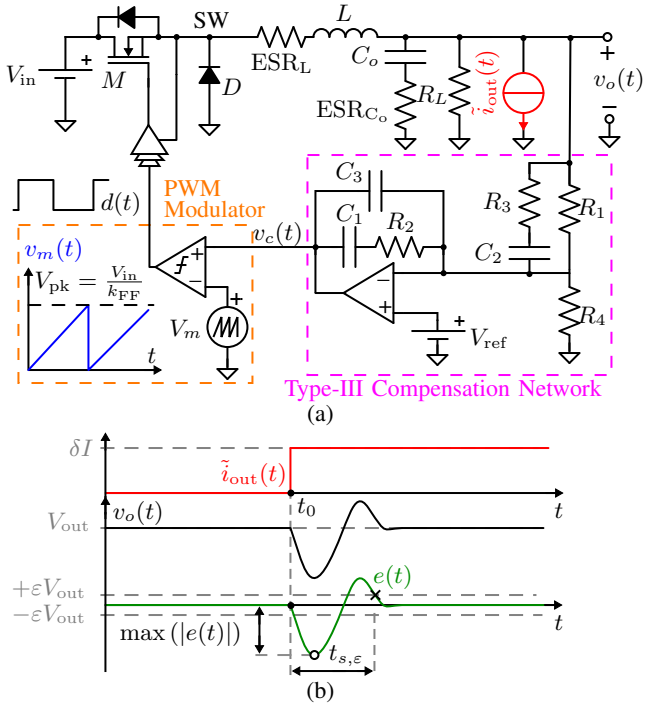

Fig. 1. Traditional VMC Buck Converter with input voltage feed-forwarding. (a) Circuital Schematic; (b) Load-Transient Response..

paper, the optimized design process is conducted by both Genetic Algorithm (GA) and Particle Swarm Optimization (PSO) methods, traversing a search space defined by a set of input voltage V_{in} and output load R_L values. These are properly defined to span both the CCM and DCM regions. The proposed methodology is adaptable to other DC-DC converter topologies (e.g., Boost, Buck-Boost) and control architectures (e.g., current mode control).

The paper is organized as follows. First, the averaged small-signal models of a VMC Buck converter and the traditional design methodologies are quickly reviewed. Then, a brief overview of the exploited optimization algorithms and the optimization procedure is carried out. The results achieved through MATLAB are validated in SIMPLIS, showing how the proposed method allows to synthesize a Buck controller with average better performances compared to traditional one. Finally, we draw the conclusions.

This is the author's version of the article that has been presented at IEEE ISCAS2025
The editorial version of the paper is available at http://dx.doi.org/10.1109/ISCAS56072.2025.11043707

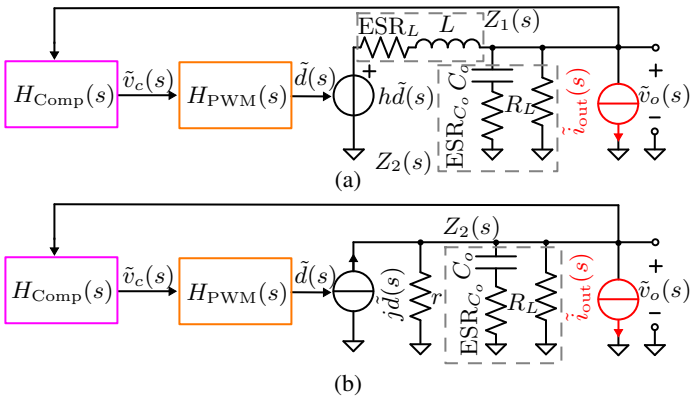

Fig. 2. Averaged Small-signal model of a VMC Buck Converter with external load disturbance operating: (a) in CCM; (b) in DCM.

TABLE I
BUCK CONVERTER SMALL-SIGNAL MODEL PARAMETER VALUES

M	$R_e[\Omega]$	D	$r[\Omega]$	j[A]	h[V]
$\frac{V_{\text{out}}}{V_{\text{in}}}$	$R_L\frac{(1-M)}{M^2}$	$\sqrt{\frac{2L}{R_e T_{\text{sw}}}}$	M^2R_e	$2\frac{(1-M)V_{\text{in}}}{DMR_e}$	V_{in}

II. SMALL-SIGNAL MODEL IN CCM/DCM AND GLIMPSES ON THE TRADITIONAL DESIGN METHODOLOGY

The VMC Buck converter shown in Fig. 1(a) is a single-loop control architecture. A type-III compensation network serves as controller sensing the output voltage $v_o(t)$ and producing a compensation signal $v_c(t)$. From the comparison between $v_c(t)$ and the sawtooth waveform $v_m(t)$, the PWM modulator generates a PWM signal $d(t)$ at a fixed frequency f_{sw}, driving the MOSFET M. A switching voltage $v_{\text{SW}}(t)$ on the SW node is thus produced by the switching action induced by M and the diode D. The output filter is made up by the L and C_o, together with the respective parasitic resistances ESR_{L} and $\text{ESR}_{\text{C}_\text{o}}$. It smooths $v_{\text{SW}}(t)$ producing the output voltage $v_o(t)$. The converter is supplied from an input source V_{in} and a resistive load R_L is placed at its output port. The values of these parameters are externally imposed and therefore, the converter can in principle operate either in CCM or in DCM.

To address the converter analysis and design, averaged small-signal models are adopted. These are represented in Fig. 2 for both CCM and DCM operating condition [6]. Hereinafter, the symbol $\tilde{\cdot}$ will denote a generic small-signal quantity and s is the complex variable in the Laplace domain. The newly defined small-signal parameters are summarized and Table I. From the closed-loop converter small-signal models in Fig. 2, the main converter transfer functions can be derived. The loop-gain of the circuit in CCM (or in DCM, respectively) is defined as

$$T_v^{\text{CCM,DCM}}(s) = -H_{\text{vd}}^{\text{CCM,DCM}}(s)H_{\text{Comp}}(s)H_{\text{PWM}}(s), \qquad (1)$$

where $H_{\text{vd}}^{\text{CCM,DCM}}(s)$ is the open-loop converter duty-to-output transfer function in CCM (DCM), $H_{\text{Comp}}(s)$ is the type-III compensation network transfer function and $H_{\text{PWM}}(s)$ is the sawtooth-based PWM modulator transfer function. The analytical expressions of $H_{\text{vd}}^{\text{CCM,DCM}}(s)$ are summarized in Table II. Regarding $H_{\text{PWM}}(s)$, it is well established [6, Ch. 7.3] that

$$H_{\text{PWM}}(s) = \frac{\tilde{d}(s)}{\tilde{v}_c(s)} = \frac{1}{V_{\text{pk}}}, \qquad (2)$$

TABLE II
MAIN BUCK CONVERTER OPEN-LOOP SMALL-SIGNAL TRANSFER FUNCTION. THE EXPRESSIONS OF $Z_1(s)$ AND $Z_2(s)$ CAN BE DERIVED FROM FIG. 2.

	x=CCM	x=DCM
$H_{\text{vd}}^x(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)}$[V]	$h\frac{Z_2(s)}{Z_1(s)+Z_1(s)}$	$j_2\,(r_2 \| Z_2(s))$
$Z_{\text{out}}^x(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)}[\Omega]$	$Z_2(s) \| Z_1(s)$	$r_2 \| Z_2(s)$

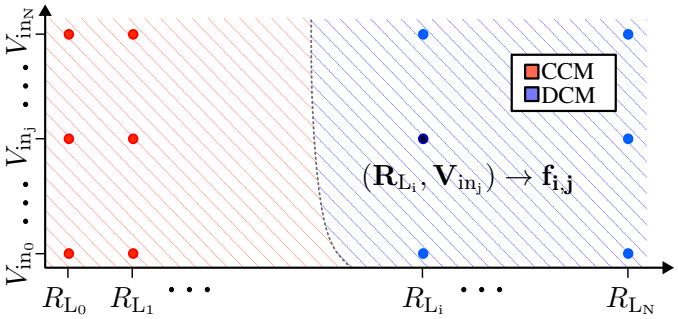

Fig. 3. Representations of some of the $(R_{L_i}, V_{\text{in}_j})$ pairs used in the calculation of the fitness function F. For each pair, the function $f_{i,j}$ is calculated as in (7) to estimate its performance. Then, the fitness function (6) estimates the overall performance of the controller across the set of all these points.

where V_{pk} is the peak value of the sawtooth waveforms employed in the PWM modulator. Furthermore, referring to Fig. 1(a), the compensation network transfer function can be computed from simple circuital analysis as

$$H_{\text{Comp}}(s) = \frac{\tilde{v}_c(s)}{\tilde{v}_o(s)} = -\frac{(1+s(R_1+R_3)C_2)(1+s\,R_2C_1)}{s\,R_1(C_2+C_3)(1+s\,R_3C_2)(1+s\,R_2\frac{C_1C_3}{C_1+C_3})}. \qquad (3)$$

Typical guidelines for the component values of the compensation network refers to the $H_{\text{vd}}^{\text{CCM}}(s)$ transfer function only. In this scenario, $T_v^{\text{CCM}}(s)$ in (1) is dependant on the static input voltage value V_{in}. To cancel out this dependency, an input voltage feed-forwarding is typically implemented in VMC Buck converter [9], [10], [14] by imposing $V_{\text{pk}} = V_{\text{in}}/k_{\text{FF}}$, where k_{FF} is a constant value. This mitigates the propagation of input voltage disturbances and therefore, they will not be considered in the following analysis. That said, the poles and zeroes in $H_{\text{Comp}}(s)$ are positioned to shape the converter loop gain, ensuring adequate stability margin at the desired crossover frequency ω_c (i.e., where $|T_v^{\text{CCM}}(s = j\omega_c)| = 1$) and disturbance rejection at the switching frequency $\omega_{\text{sw}} = 2\pi f_{\text{sw}}$. Generally, ω_c must be less than ω_{sw}, typically it is set as $\omega_c = \omega_{\text{sw}}/10$. Once the $H_{\text{Comp}}(s)$ is established, the response to external disturbances can be estimated. The closed-loop output impedance describes how variations in the load current affect the output voltage, and it is derived by inspection from Fig. 2(a) (or Fig. 2(b)) as

$$Z_{\text{out,CL}}^{\text{CCM,DCM}}(s) = -\frac{\tilde{v}_o(s)}{\tilde{i}_{\text{out}}(s)} = \frac{Z_{\text{out}}^{\text{CCM,DCM}}(s)}{1 + T_v^{\text{CCM,DCM}}(s)}, \qquad (4)$$

where $Z_{\text{out}}^{\text{CCM,DCM}}(s)$ is the open-loop output impedance in CCM (respectively, in DCM), defined in Table II. Applying a step output current excitation, i.e., $\tilde{i}_{\text{out}}(s) = \delta I/s$, the converter output voltage response in time can be computed as

This is the author's version of the article that has been presented at IEEE ISCAS2025
The editorial version of the paper is available at http://dx.doi.org/10.1109/ISCAS56072.2025.11043707

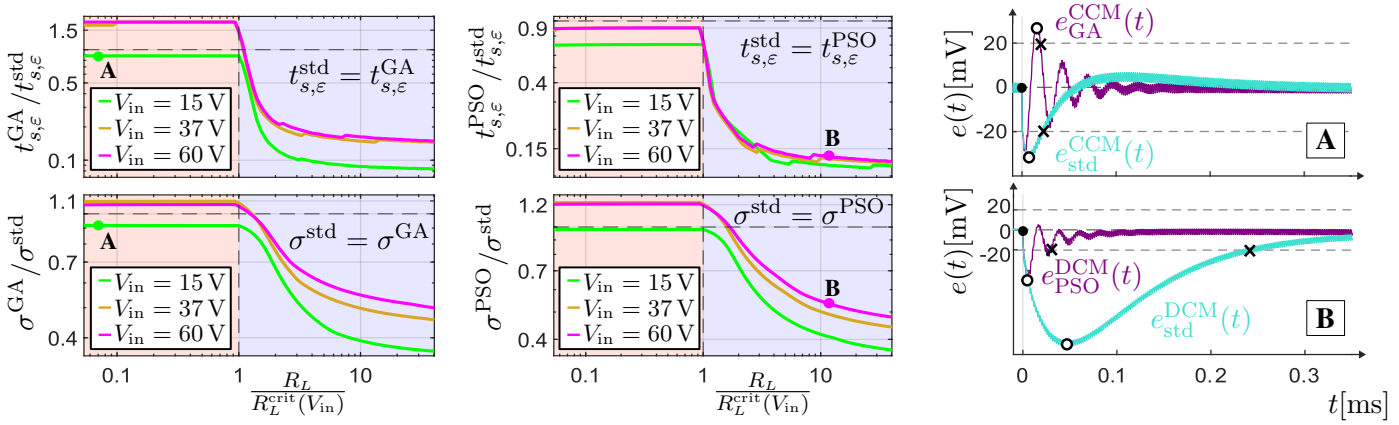

Fig. 4. Comparison of GA and PSO results. The σ and $t_{s,\varepsilon}$ ratio between the standard compensation network and ours (i.e., the optimized one) are shown in (a) and (b), where both the x and y-axis are in logarithmic scale.. The horizontal dashed line indicates equal performances, while the vertical dashed line separates the CCM and DCM domains (respectively, the transparent red area and the blue area). The points A and B are taken as references examples showing the SIMPLIS simulation waveforms in (c).

$$v_o^{CCM,DCM}(t) = V_{out} + \underbrace{\mathscr{L}^{-1}\left\{-Z_{out,CL}^{CCM,DCM}(s)\cdot \tilde{i}_{out}(s)\right\}(t)}_{\stackrel{def}{=} e^{CCM,DCM}(t)}, \quad (5)$$

where V_{out} is the steady-state converter output voltage and $\mathscr{L}\{\cdot\}$ is the Laplace-transform operator. The error signal $e^{CCM,DCM}(t)$ is defined as the time varying part, and it is represented in Fig. 1(b).

According to the traditional design methods though, the DCM operating mode is overlook. Designing the controller in CCM ensures stability in DCM, although a severe performance degradation is expected at light-loads (large R_L values) [6]. In DCM, the small-signal dynamic behaviour of the converter is intriguingly dependent on the converter operating conditions (i.e., from R_L and V_{in}). Therefore, a controller design methodology involving both CCM and DCM can not be derived in a closed-form analytical solutions. An automated numerical procedure that compute the optimal controller component values is thus required.

III. Optimization Algorithms: GA and PSO

GA and PSO are two widely used metaheuristic algorithms designed to tackle complex optimization problems and explore large search spaces efficiently.

In particular, GA [15] is an optimization method inspired by the process of natural selection. Initially, a random population is generated and each individual is evaluated using a fitness function. The best-performing individuals are more likely to be selected to reproduce, combining part of their solution representation through crossover, with occasional mutations to maintain diversity and avoid premature convergence. This process repeats until a convergence criterion, such as minimal improvement in fitness, is met.

Instead, PSO [16] draws inspiration from the collective behaviour of animals like birds and fish. A group of particles, each representing a candidate solution, moves through the search space by adjusting their velocity and position. The velocity adjustments are guided by both the best solution found by each particle so far, the best solution found by the entire group, and its current velocity, respectively scaled by the cognitive, the social and the inertia coefficient. Through this balance the particles explore and refine solutions, moving toward optimal areas until, again, a convergence condition is met.

A. Parameters Encoding and Fitness Function

Each candidate solution is encoded as a vector of floating-point numbers, where each element represents one of the controller circuital parameter, i.e., referring to Fig. 1(a), the elements $R_{1,2,3}$ and $C_{1,2,3}$. The latter can vary between an upper and a lower bound, namely, $5\,k\Omega < R_{1,2} < 5\,M\Omega$, $100\,\Omega < R_3 < 1\,M\Omega$ and $1\,pF < C_{1,2,3} < 10\,nF$, in order to obtain only realistic component values.

The optimized values are identified by minimizing a fitness function. The latter reflects how effectively the solution meets the optimization objective, which in our case is to design a controller that, on average, performs better than a conventional one when operating in both CCM and DCM. Therefore, the fitness function is defined as follow:

$$F = \sqrt{\sum_{i=1}^{N}\sum_{j=1}^{N} f_{i,j}^2} \quad (6)$$

Where $f_{i,j}$ evaluates the controller's performance under a specific operating condition of the converter, uniquely associated with the indices i, j. Specifically, based on the ranges of R_L and V_{in} a total of N^2 different pairs of points (R_{L_i}, V_{in_j}) are selected, where $(i,j) \in \{1,2,...,N\}^2$ identify each pair, as represented in Fig.3. Every of these pairs uniquely defines the converter operating mode.

To guarantee that the optimization process does not favor a controller with good performance only in specific areas, these pairs are uniformly distributed across both CCM and DCM regions, ensuring coverage of the entire range of R_L and V_{in}. The function $f_{i,j}$, for each pair (R_{L_i}, V_{in_j}) is thus defined as follow:

$$f_{i,j} = \lambda_0 ITAE_{i,j} + \lambda_1 ISE_{i,j} + \lambda_2 IAE_{i,j}, \quad (7)$$

where ITAE, IAE and ISE are typical integral performance indices quantifying the system deviation from the setpoint during the transient phase when the converter is subjected to a step-load variation as in Fig. 1(b). For further details on how these indices relates to the transient response of the system refer to [17]. In particular, they can be defined as:

- $ITAE_{i,j}$ (Integral of the Time-weighted Absolute Error) is defined as:
$$ITAE_{i,j} = \int_0^{+\infty} t\,|e_{i,j}(t)|\,dt$$
- $ISE_{i,j}$ (Integral of Square Error) is given by:
$$ISE_{i,j} = \int_0^{+\infty} e_{i,j}^2(t)\,dt$$

This is the author's version of the article that has been presented at IEEE ISCAS2025
The editorial version of the paper is available at http://dx.doi.org/10.1109/ISCAS56072.2025.11043707

- $\mathrm{IAE}_{i,j}$ (Integral of the Absolute value of Error) is defined as:

$$\mathrm{IAE}_{i,j} = \int_0^{+\infty} |e_{i,j}(t)|\, dt.$$

The signal $e_{i,j}(t)$ is defined as

$$e_{i,j}(t) = \begin{cases} e^{\mathrm{CCM}}(t), & \text{if } R_{L_i} < R_L^{\mathrm{crit}}(V_{\mathrm{in}_j}) \\ e^{\mathrm{DCM}}(t), & \text{if } R_{L_i} > R_L^{\mathrm{crit}}(V_{\mathrm{in}_j}) \end{cases} \tag{8}$$

where $R_L^{\mathrm{crit}}(V_{\mathrm{in_j}})$ is the critical load resistance [6], defined as

$$R_L^{\mathrm{crit}}(V_{\mathrm{in}_j}) = 2Lf_{\mathrm{sw}}\frac{V_{\mathrm{in}_j}}{V_{\mathrm{in}_j} - V_{\mathrm{out}}} \tag{9}$$

and $e^{\mathrm{CCM,DCM}}(t)$ are computed through (5). Employing the converter small-signal model in place of simulating the real switching converter via heavy transient analysis leads to a substantial reduction in the computational time of the optimization algorithm. The parameters λ_0, λ_1 and λ_2 act as scaling factor, making the three summation terms in (7) numerically comparable. To discard unfeasible solutions, the value of $f_{i,j}$ is set to `Inf` if any of the following constraints are violated:

- $\omega_c > \omega_{\mathrm{sw}}/10$;
- multiple ω_c are detected;
- the system is unstable, i.e., the equation $1 + T_v(s)$ has solutions lying in the right half-plane.

It is worth noting that, in principle, the small-signal models only describes the converter response to *small* perturbations around its cyclostationary operating point. However, they still provide physical insights into the system's dynamic response to external step-load perturbations, thus resulting invaluable tools in the design of DC-DC converter control-loops.

IV. Simulation Environment and Results Comparison

The GA and PSO optimization algorithms are simulated in MATLAB, each with its own settings. In particular:

- GA: The population initialization is random, with each variable uniformly distributed between its lower and upper limits. A scattered crossover with a probability of 80% and a Gaussian mutation with a probability of 20% are used. A tournament selection of size 2 is employed as the parent selection function, and additionally, elitism of 5% of the population is ensured.
- PSO: The initialization of the initial positions is random, with each variable uniformly distributed between its lower and upper limits, while the velocities are randomly chosen uniformly between -1000 and 1000. An adaptive inertia is used with values ranging from 0.1 to 1.1, while the coefficients for the cognitive and social components are both chosen as constant and equal to 1.49.

In both algorithms, an initial population of 100 individuals is used, and the stopping condition is met if the fitness function remains unchanged for 3 iterations. The parameters used for the fitness function calculation are: $\lambda_0 = 1\,\mathrm{V}^{-1}\mathrm{s}^{-2}$, $\lambda_1 = 10^{-5}\,\mathrm{V}^{-2}\mathrm{s}^{-1}$ and $\lambda_2 = 10^{-6}\,\mathrm{V}^{-1}\mathrm{s}^{-1}$. The V_{in} and R_L values are respectively selected from the ranges $[15\,\mathrm{V}, 60\,\mathrm{V}]$ and $[0.5\,\Omega, 500\,\Omega]$. Assigning $N = 10$, a total of $N^2 = 100$ pairs are selected. Specifically, N linearly spaced values are chosen from the V_{in} range, and N logarithmically spaced values are selected from the R_L range. This approach ensures that approximately half of the pairs fall within the CCM domain and the other half in the DCM domain. The fixed component and parameter values of the VMC Buck converter are: $L_f = 8.2\,\mu\mathrm{H}$, $C_o = 260\,\mu\mathrm{F}$, $\mathrm{ESR}_{L_f} = 5\,\mathrm{m}\Omega$, $\mathrm{ESR}_{C_o} = 5\,\mathrm{m}\Omega$, $k_{\mathrm{FF}} = 30$, $V_{\mathrm{ref}} = 800\,\mathrm{m}\Omega$, $f_{\mathrm{sw}} = 500\,\mathrm{kHz}$. The desired steady-state output voltage value is $V_{\mathrm{out}} = 5\,\mathrm{V}$.

TABLE III
Controller Circuital Parameters Design obtained by Standard and Optimization Methods

Strategy	R_1	R_2	R_3	C_1	C_2	C_3
Standard	13 kΩ	5.5 kΩ	144 Ω	10.5 nF	4.41 nF	115 pF
GA	5 kΩ	10 kΩ	966 Ω	423 pF	1 nF	1 pF
PSO	5 kΩ	31.6 kΩ	521 kΩ	1.39 nF	5.72 nF	1 pF

Since metaheuristic algorithms have a stochastic nature multiple runs are performed, only selecting the best results. The latter are listed in Table III, together with the component values of a controller designed following a traditional approach (e.g., refer to the methodology proposed in [10]). Note that the R_4 value is not a parameter to be optimized since, in order to regulate the desired V_{out}, it must be fixed to $R_4 = R_1/(V_{\mathrm{out}}/V_{\mathrm{ref}} - 1)$. In order to make a fair comparison and be consistent with the algorithms constraints listed at the end of Section III, the standard controller is designed to have $\omega_c = \omega_{\mathrm{sw}}/10$.

The dynamic performances of the VMC Buck converter embedding the optimized and traditional compensation networks are evaluated through SIMPLIS simulator. Standard indices are derived from a transient analysis, viz., the ε-settling time $t_{s,\varepsilon}$ and the relative over/under-shoot σ of the output voltage $v_o(t)$ in response to a step-load transient with amplitude $\delta I = 3\,\mathrm{A}$. Referring to Fig. 1(b), these are defined from $e(t)$ by the set of equations

$$\begin{aligned} t_{s,\varepsilon}: \quad & |e(t_0 + t_{s,\varepsilon})| = \varepsilon V_{\mathrm{out}} \\ \sigma := \quad & \frac{\max_{t>t_0}(|e(t)|)}{V_{\mathrm{out}}} \end{aligned} \tag{10}$$

where $t_0 = 0$ is the time at which the step-load is applied and, in line with this application scenario, $\varepsilon = 0.004$ (resulting in comparison thresholds for $e(t)$ of $\pm 20\,\mathrm{mV}$).

The results are shown in Fig. 4. In general, through the optimized component values, both the GA and PSO lead to an average performance improvement. In CCM (i.e., in the red transparent areas in Fig. 4(a) and Fig. 4(b)), both the optimized $t_{s,\varepsilon}$ and the σ values are comparable (barring slight deterioration) with the standard ones, for all the V_{in} and R_L values. Instead, significant improvements are achieved in DCM (i.e., in the blue transparent areas in Fig. 4(a) and Fig. 4(b). The $\sigma^{\mathrm{GA,PSO}}$ is reduced by almost 2.5 times at light-loads compared to σ^{std}, while the $t_{s,\varepsilon}^{\mathrm{GA,PSO}}$ values achieve a reduction of at-least 7 times compared to $t_{s,\varepsilon}^{\mathrm{std}}$. Snapshots of SIMPLIS simulation waveforms are shown in Fig. 4(c) for illustrative purposes.

V. Conclusion

In this work, an AI-based design methodology for the control network of a PWM DC-DC converter operating in CCM and DCM is proposed. In particular, the optimum component values of a type-III compensation network employed in a VMC Buck converter are derived via the GA and PSO algorithms. A validation phase is conducted through circuital simulations in SIMPLIS. The optimized controller performs comparably to the traditional one in CCM, while a significant performance improvement is achieved in DCM, substantiating the validity of the proposed approach.

Acknowledgment

This study was carried out within the FAIR - Future Artificial Intelligence Research and received funding from the European Union Next-Generation EU (Piano Nazionale di Ripresa e Resilienza (PNRR) – Missione 4 Componente 2, Investimento 1.3 – D.D. 1555 11/10/2022, PE00000013). This manuscript reflects only the authors' views and opinions, neither the European Union nor the European Commission can be considered responsible for them.

REFERENCES

[1] M. Das and V. Agarwal, "Generalized small signal modeling of coupled inductor based high gain, high efficiency dc-dc converters," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 2691–2695. doi: 10.1109/APEC.2015.7104731

[2] I. Biswas, D. Kastha, and P. Bajpai, "Small signal modeling and decoupled controller design for a triple active bridge multiport dc–dc converter," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1856–1869, 2021. doi: 10.1109/TPEL.2020.3006782

[3] K. Khatun and A. K. Rathore, "Small signal modeling, closed loop design, and transient results of snubberless naturally-clamped soft-switching current-fed half-bridge dc/dc converter," in *2019 IEEE 28th International Symposium on Industrial Electronics (ISIE)*, 2019, pp. 2571–2576. doi: 10.1109/ISIE.2019.8781406

[4] B. Bryant and M. Kazimierczuk, "Voltage loop of boost pwm dc-dc converters with peak current-mode control," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 1, pp. 99–105, 2006. doi: 10.1109/TCSI.2005.854611

[5] M. K. Kazimierczuk, *Pulse-Width Modulated DC-DC Power Converters*, 2nd ed. Hoboken, NJ: John Wiley & Sons, 2015.

[6] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 3rd ed. Cham, Switzerland: Springer, 2020.

[7] M. Hankaniemi, M. Karppanen, and T. Suntio, "Dynamical characterization of voltage-mode controlled buck converter operating in ccm and dcm," in *2006 12th International Power Electronics and Motion Control Conference*, 2006, pp. 816–821. doi: 10.1109/EPEPEMC.2006.4778500

[8] H. Venable, "The k factor: A new mathematical tool for stability analysis and synthesis," in *Proceedings of the Powercon 10 Conference*. San Diego, CA: Venable Industries, 1983, pp. 1–12.

[9] T. Instruments, "Lv5144 95-v, synchronous, buck dc/dc controller with wide duty cycle range," https://www.ti.com/lit/ds/symlink/lv5144.pdf, August 2023.

[10] STMicroelectronics, "Wide 6 v to 75 v input voltage synchronous buck controller," https://www.st.com/resource/en/datasheet/l3751.pdf, September 2024.

[11] S. Zhao, F. Blaabjerg, and H. Wang, "An overview of artificial intelligence applications for power electronics," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4633–4658, 2021. doi: 10.1109/TPEL.2020.3024914

[12] M. B. P and S. Bhat, "Steady state and transient state analysis of buck-boost converter with genetic algorithm optimized pid controller," in *2022 International Conference on Smart Generation Computing, Communication and Networking (SMART GENCON)*, 2022, pp. 1–6. doi: 10.1109/SMARTGENCON56628.2022.10084253

[13] D. Patel, Srishti, and P. K. Padhy, "Optimal tuning of fractional order pid controller with metaheuristic algorithms for high efficiency high gain dc-dc boost converter," in *2023 International Conference on Power Electronics and Energy (ICPEE)*, 2023, pp. 1–6. doi: 10.1109/ICPEE54198.2023.10059937

[14] M. Amer, A. Abuelnasr, M. Ali, A. Hassan, A. Trigui, A. Ragab, M. Sawan, and Y. Savaria, "Enhanced dynamic regulation in buck converters: Integrating input-voltage feedforward with voltage-mode feedback," *IEEE Access*, vol. 12, pp. 7310–7328, 2024. doi: 10.1109/ACCESS.2024.3351051

[15] D. E. Goldberg, *Genetic Algorithms in Search, Optimization and Machine Learning*, 1st ed. USA: Addison-Wesley Longman Publishing Co., Inc., 1989.

[16] J. Kennedy and R. Eberhart, "Particle swarm optimization," in *Proceedings of ICNN'95 - International Conference on Neural Networks*, vol. 4, 1995, pp. 1942–1948 vol.4. doi: 10.1109/ICNN.1995.488968

[17] R. Poley, *Control Theory Fundamentals*, 3rd ed. CreateSpace Independent Publishing Platform, 2015.