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Analysis and Design of ULV DIGOTAs in 16 nm CMOS FinFET / Machado, R., Toledo, P., Bica Oliveira, L., Máximo, M., Santos, M., Oliveira, J., Crovetti, P.S.. - STAMPA. - (2025). (2025 IEEE International Symposium on Circuits and Systems (ISCAS) London (UK) 25-28 May 2025) [10.1109/ISCAS56072.2025.11043594].

Availability:
This version is available at: 11583/3001350 since: 2025-06-28T11:02:57Z

Publisher:
IEEE

Published
DOI:10.1109/ISCAS56072.2025.11043594

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20 October 2026

Analysis and Design of ULV DIGOTAs in 16 nm CMOS FinFET

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[1] ***Abstract*—Three Digital Operational Transconductance Amplifier (DIGOTA) topologies, i.e. the standard DIGOTA, a Schmitt-Trigger-Based DIGOTA (ST-DIGOTA) and a DIGOTA with a Floating-Inverter input stage (FI-DIGOTA), are designed for the first time in a 16 nm CMOS FinFET technology and their performance is compared on basis of post-layout simulations. All the DIGOTAs operate at 300 mV power supply while driving a capacitive load of 350 pF. The standard DIGOTA presented the lowest silicon area (44 µm^2) and a power consumption of 99.4 nW at 59 kHz Gain-Bandwidth Product (GBW). The ST-DIGOTA achieved the highest DC gain of 43.9 dB, at the cost of a 6X increased power (609 nW) and 14% larger area, while the FI-DIGOTA achieves the highest GBW (100.3 kHz) and Slew Rate (8 mV/µs) at 36X more power (3.67 µW) and 2.5x larger are than the standard DIGOTA.**

According to these results, an area-normalized large signal figure of merit (IFOM$_{LA}$) of 117k, 19.2k and 1.8k (mV/µ s)·pF/(nA·mm^2) was accomplished along with an area-normalized small signal figure of merit (IFOM$_{SA}$) of 1.42M, 236k and 23.6k kHz ·pF/(nA· mm^2) for the DIGOTA, ST-DIGOTA and FI-DIGOTA, respectively, where the first two topologies surpass the current state of the art.

***Index Terms*—Ultra Low Voltage (ULV), Operational Transconductance Amplifier (OTA), Digital-Based Circuit, Schmitt-Trigger, Internet of Things (IoT).**

I. Introduction

The design of analog and mixed-signal cells in digital-centered nanoscale technologies is increasingly challenging due to the poor analog characteristics of nanoscale devices, reduced noise margins and large leakage currents, which hinder the applicability of traditional analog design techniques [1] and/or result in largely power- and area-inefficient solutions.

Focusing on the Operational transconductance Amplifier (OTA), an ubiquitous building block in low-frequency acquisition front-ends and analog sub-systems, gate-driven OTAs cannot operate at (Ultra Low Voltage) ULV (i.e. below 1- 0.8 V) and (Ultra Low Power) ULP, thus motivating the interest for radically different OTAs such as bulk-driven, inverter-based, subthreshold, floating-gate, and digital-based topologies [2], [3].

Digital-based OTAs [4] have been gaining plenty of attention as they do not require any DC bias current and take advantage of technology scaling, leading to decreased power consumption and improved performance/area ratio, as it happens for digital circuits [5–12].

In this paper, the DIGOTA published in [13], [14] and the Schmitt-Trigger based DIGOTA showcased in [15] are ported and post-layout simulated in a 16 nm CMOS FinFET technology for the first time. Moreover a DIGOTA that uses Floating Inverters as an input stage (FI-DIGOTA), adapted from [16], is proposed and also validated. To the best of the authors' knowledge, there aren't many comprehensive characterisations of OTAs in FinFET technology in the literature as of yet.

The paper is organized as follows: Section II overviews the circuit description of the DIGOTA, ST-DIGOTA and the FI-DIGOTA in ULV as well as some of the followed design guidelines. In Section III, simulation results are shown and a comparison with the current state-of-art is provided. Conclusions are drawn in Section IV.

II. ULV DIGOTAs Circuit Description

The standard DIGOTA, the Schmitt-Trigger-Based DIGOTA (ST-DIGOTA) and the DIGOTA with a Floating-Inverter input (FI-DIGOTA) topologies considered in this paper are introduced in this Section, and their operation is shortly revised.

A. DIGOTA Circuit and Operation

Fig.1 a) shows the schematic of the conventional DIGOTA [13], [14]. The circuit consists of two *Muller C-elements*, the inverters INV_+ and INV_-, the *MCswap tri-state buffers* (CM-Extractor), and the *output stage*.

The most remarkable feature of DIGOTA is the replacement of the differential pair with digital gates, while preserving the same functionality, i.e. amplify the differential input signal $v_d = (v_{IN+} - v_{IN-})$ while rejecting its common-mode component $v_{cm} = \frac{(v_{IN+}+v_{IN-})}{2}$. To accomplish these goals, the two Muller C-elements sense the input voltages v_{IN+} and v_{IN-}.

As detailed in [14], the circuit itself activates the *Muller C-elements* pull-up or pull-down alternately through the *MC-swap tri-state buffers* when the input differential signal is zero ($v_d = 0$). This leads to a dynamic compensation of the common-mode input voltage, making the circuit oscillate between two states, i.e., states where the output of the inverters

[1]This work was supported by FCT under CTS multiannual funding program CTS

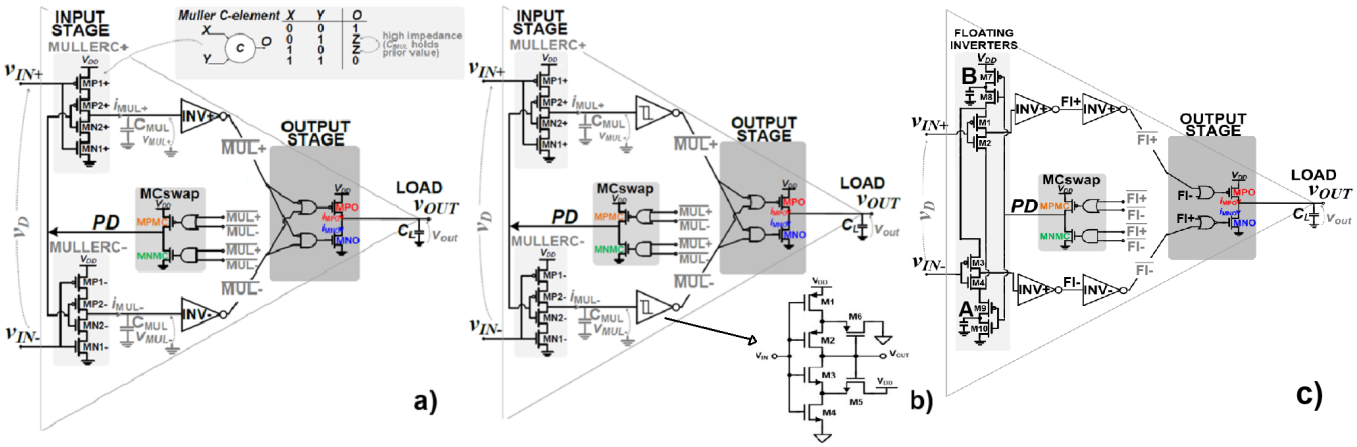

Fig. 1: Schematic of a) DIGOTA [13] ; b) ST-DIGOTA [15] ; c) the proposed FI-DIGOTA.

INV_+ and INV_- are exchanged between 0 and 1 synchronously ($(\overline{MUL_+}, \overline{MUL_-}) = (0,0),(1,1)$). On the other hand, when a differential input signal is detected ($v_d \neq 0$) the DIGOTA presents additional states, $(\overline{MUL_+}, \overline{MUL_-}) = (0,1),(1,0)$, where the output stage is triggered, therefore amplifying the input signal. The output voltage (V_{out}) is either increased or decreased through the transistors MPO and MNO in accordance with the sign of v_d.

As a result of the circuit's digital nature, a bias circuit is not necessary since all transistors operate in a digital fashion (either in the ON or in the OFF region), resulting in a zero DC bias current.

B. ST-DIGOTA Circuit

The schematic of the ST-DIGOTA circuit is illustrated in Fig. 1 b). In this topology, which was originally introduced in [15], the CMOS inverters of the standard DIGOTA are replaced by a Schmidt Trigger (ST) inverter, characterized by an intrinsic hysteretic behavior and two different switching thresholds V_{trip1} and V_{trip2} for the 0-to-1 and the 1-to-0 transitions when operated at power supply voltages above 75 mV at room temperature [17].

The adoption of ST inverters causes the ST-DIGOTA to spend more time in the states $(\overline{MUL_+}, \overline{MUL_-}) = (0,1),(1,0)$, in which the output stage is active, thus raising the overall equivalent transconductance g_m as demonstrated in [15].

C. FI-DIGOTA Description

The schematic of the proposed FI-DIGOTA is offered in Fig. 1 c). In this DIGOTA variant, the two *Muller C-elements* of the baseline DIGOTA in Fig.1 a) are replaced by *floating inverters* [18], whose positive (negative) supply rails are dynamically connected to very small capacitors (obtained in practice taking advantage of parasitics) pre-charged to the supply voltage (to ground) in the previous cycle, when the CM input voltage is below (above) the trip points of both the inverters INV_+ and INV_-, i.e. when $(\overline{FI_+}, \overline{FI_-}) = (0,0)$ $(\overline{FI_+}, \overline{FI_-}) = (1,1)$)

In this reconfiguration, the input floating inverters are dynamically baised, as required to asymmetrically discharge (charge) the input parasitic capacitances of the inverters INV_+ and INV_- and drive the output stage in the states $(\overline{FI_+}, \overline{FI_-}) = (0,1),(1,0)$ depending on the sign of v_d, as in the standard DIGOTA.

The FI-DIGOTA is supposed to enjoy the inherent efficiency of the FI cell [18] due to dynamic biasing and charge reuse.

D. Design Guidelines

The DIGOTAs described in the previous section have been designed and simulated in a 16 nm FinFET technology taking advantage of a digital standard cell design flow, using CMOS static logic for most of the gates shown in Fig 1. All the DIGOTAs have been designed to operate at 300 mV supply voltage, which is close to the Minimum Energy Point (MEP) for ultra-low power (ULP) operation [19], and their output stage has been designed to drive a maximum capacitive load of 350 pF. All the other design choices have been oriented to maximize energy efficiency and circuit performance.

III. Post-Layout Simulations Results

All DIGOTAs have been designed and simulated using 16 nm FinFET CMOS technology. The DIGOTA (43.6 μm^2) and ST-DIGOTA (49.6 μm^2) silicon areas remain under the 50 μm^2 mark while the FI-DIGOTA attained an area of 123.3 μm^2, as seen in Fig. 2. A post-layout analysis of all DIGOTAs' functionality and performance in the voltage follower configuration with a load capacitance (C_L) of 350 pF has been performed.

A. Simulated Performance

Fig. 3 displays the time-domain input and output waveforms of all topologies at V_{DD} = 300mV. These waveforms were acquired with a sine wave as the input signal at a frequency of 500 Hz and a peak amplitude of 10 mV. For this input signal, the DIGOTA, ST-DIGOTA and FI-DIGOTA power consumptions are 99.4 nW, 609 nW, and 3.6 μW, respectively. In such conditions, all DIGOTAs showcased a THD below

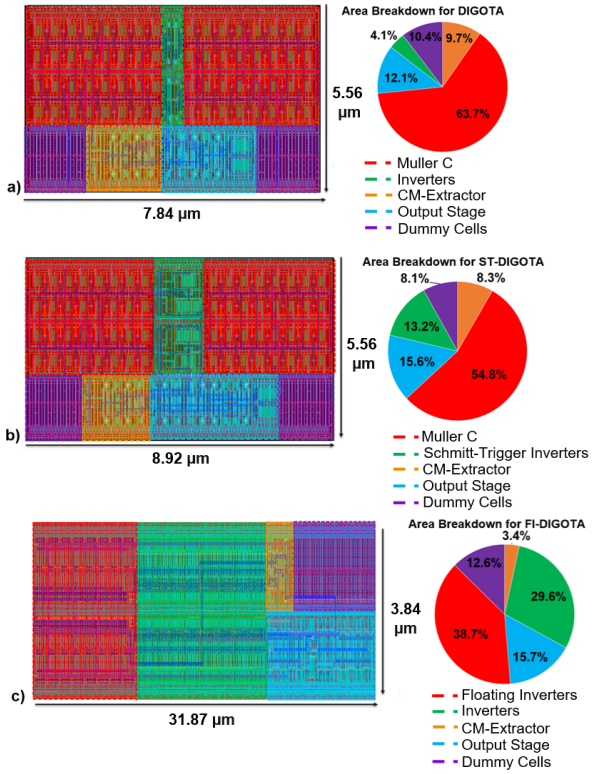

Fig. 2: Layout and Area Breakdown of the DIGOTAs.

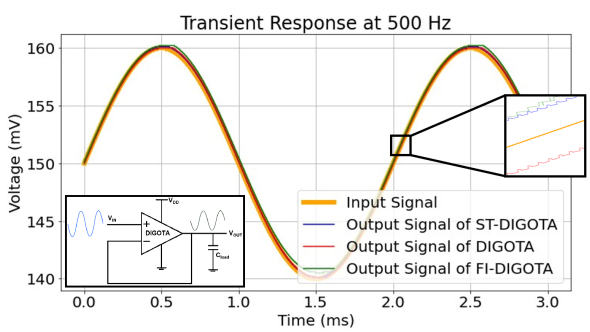

Fig. 3: Transient response of all DIGOTAs at 500 Hz and peak amplitude of 10mV.

1.2%. By examining the waveforms in greater detail (the zoomed part), it is possible to see how the digital operation (discrete change in the output voltage) in all circuits produces noticeable differences in the output voltage (v_{out}).

1) Frequency Response: The frequency response of these digital-like circuits has been tested through large-signal simulations in the time domain under different sine wave input frequency, as in [20]. The frequency response in magnitude and phase is then calculated computing the ratio of the Fast Fourier Transform (FFT) at each input test frequency for both the output and differential voltage signals [20]. The DIGOTA, ST-DIGOTA and FI-DIGOTA frequency responses reported in Fig. 4 exhibit 34.6 dB, 43.9 dB and 31.6 dB of DC gain, 59.2 kHz, 68.4 kHz and 100.3 kHz of GBW with a phase margin of 84.2°, 80.7° and 79.5°, respectively, at typical

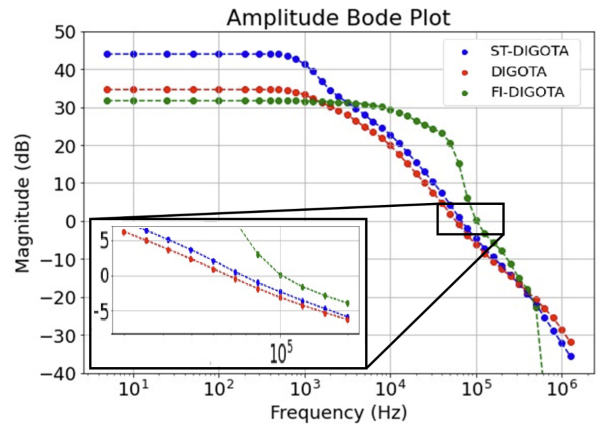

Fig. 4: Frequency response of all DIGOTAs in the typical corner.

conditions.

2) Figure of Merit (FOM): The DIGOTAs energy efficiency and performance are compared considering the Figure of Merits (FoM) [2]:

$$IFOM_{\text{S}} = \frac{GBWC_{\text{L}}}{I_{\text{DD}}} \quad \therefore \quad IFOM_{\text{L}} = \frac{SR_{\text{ave}}C_{\text{L}}}{I_{\text{DD}}} \tag{1}$$

For V_{DD} = 300 mV, at room temperature and C_L = 350 pF, DIGOTA, ST-DIGOTA and the FI-DIGOTA have achieved 62.6, 11.8 and 2.91 of $IFOM_{\text{S}}$ and 5.16, 0.96 and 0.22 of $IFOM_{\text{L}}$, respectively.

3) Process Variations and Monte Carlo (MC): Fig. 5 shows the DIGOTAs performance in the presence of process variations, considering 15 corners corresponding to -40°C, 25°C and 85°C temperatures and the five process corners for nMOS and pMOS devices (FF, FS, SF, SS and TT). These results unveil the variability of all DIGOTA topologies when implemented in more advanced technologies and working in ULV domain. The same variability is also observed in Monte Carlo simulations for the typical corner (see Table II). In Fig. 5 it can be observed that in fast corners the FI-DIGOTA does not work (DC Gain lower than 20 dB). The reason is that due to the stacked structure of input inverter generates a very small differential pulse in the time domain to trigger the output stage, making it work in its dynamic dead zone. Nonetheless, it is evident that the ST-DIGOTA achieves the highest DC Gain across all corners, except for the typical corner at -40ºC. The standard DIGOTA maintains its power consumption below the 1 μW mark, except for the fast/fast corner at 85ºC.

Table II reveals that the FI-DIGOTA is the least robust DIGOTA topology overall, with the largest standard deviation (σ) in most of the reported perfomance parameters. This arises from the distinction between the FI-DIGOTA's input stages and those of the other DIGOTAs. In such ULV domain, stacking more than four transistor has been shown problematic. The ST-DIGOTA poses itself as the more robust amongst the DIGOTAs, presenting the lowest variation in most of the performance metrics.

TABLE I: Comparison With State-of-the-Art Ultra-Low-Voltage Operational Transconductance Amplifiers

Performance	[21]$^{+}$	[13]$^{+}$	[22]*	[23]$^{+}$	[20]$^{+}$	[15]DIGOTA*	[15]ST-DIGOTA*	**DIGOTA***	**ST-DIGOTA***	**FI-DIGOTA***	Unit
Technology	65	180	180	65	180	**16**	**16**	**16**	**16**	**16**	nm
Supply Voltage	0.35	0.3	0.3	0.45	0.3	0.3	0.3	0.3	0.3	0.3	V
DC Gain	43	30	**73.52**	68	35	16.7	41.2	34.6	43.9	31.6	dB
GBW	3,600	0.25	9.63	**6,650**	0.85	15.5	26.8	59.2	68.4	100.3	kHz
Slew Rate	**5,600**	0.085	0.288	1,475	0.5	2.9	2.9	4.9	5.6	8	$\frac{mV}{\mu s}$
THD	0.6^{b}	2^{a}	-	-	3^{b}	4.3^{a}	0.75^{a}	0.75^{a}	**0.24**^{a}	1.11^{a}	%
Phase Margin	56	-	58.14	61.2	72.5	90.9	89.2	84.2	80.7	79.5	°
C_{out}	3	150	250	0.5	80	**500**	**500**	350	350	350	pF
Power	17,000	2.4	6.63	789	**2**	76	527	99.4	609	3670	nW
Die Area	5,000	982	844	20,000	1,426	54.1	75.2	**44**	50	123.3	μm^2
Normalized Area	1.18M	30.3k	**26k**	4.7M	44k	211k	293k	164k	195k	482k	-
$IFOM_S$	0.22	4.69	**108.9**	1.89	10.20	30.6	7.6	62.6	11.8	2.91	$\frac{kHz \cdot pF}{nA}$
$IFOM_L$	0.34	1.59	3.25	0.42	**6**	5.7	0.83	5.16	0.96	0.22	$\frac{pA}{(mV/\mu s) \cdot pF}$
$IFOM_{AS}$	44	4.8k	129k	95	7.2k	565k	101k	**1.42M**	236k	23.6k	$\frac{kHz \cdot pF}{nA \cdot mm^2}$
$IFOM_{AL}$	68	1.6k	3.6k	21	4.2k	105k	11k	**117k**	19.2k	1.8k	$\frac{(mV/\mu s) \cdot pF}{nA \cdot mm^2}$

$^{+}$experimental; *simulation;* **bold best result**; ^{a}Evaluated with a 10 mV input; ^{b}Evaluated with a 50 mV input

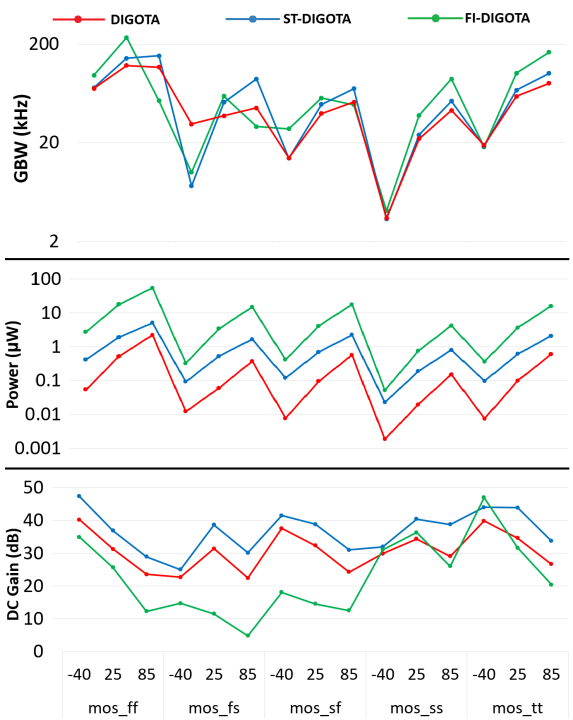

Fig. 5: GBW, Power and DC Gain Performance of all DIGOTAs across corners.

TABLE II: Typical Monte Carlos Results for all DIGOTAs.

Performance	DIGOTA (μ)	ST-DIGOTA (μ)	FI-DIGOTA (μ)	DIGOTA (σ)	ST-DIGOTA (σ)	FI-DIGOTA (σ)
Offset (mV)	4.54	4.47	4.79	1.89	1.63	1.85
DC Gain (dB)	33.21	37.03	26.29	3.09	3.35	3.26
GBW (kHz)	59.21	59.23	83.67	4.66	4.66	7.17
Slew Rate (V/ms)	5.80	6.37	14.22	3.78	3.66	13.07
THD (%)	0.74	0.43	4.43	0.33	0.21	1.37
Phase Margin (°)	84.35	84.35	82.67	1.19	1.19	2.41
Input Referred Noise (μV)	191.7	160.9	245.6	80.8	56.4	107.5
Power (nW)	133	665	5,900	10.4	34.4	257.7
PSR (dB)	47.89	48.86	49.25	9.24	4.8	8.12

331 samples with a 95% confidence interval

B. Comparison with the State of the Art

Table I shows the performance comparison between the DIGOTAs of this work and other ULV OTAs in recent literature. The presented DIGOTA topologies are the first to be simulated in post-layout using a 16 nm FinFET technology and are able to drive a lower output capacitance than the previous DIGOTAs tested in [15] (only schematic). Moreover, all of the implemented topologies present a lower area than the referred OTAs (except for the FI-DIGOTA when compared to the DIGOTA and ST-DIGOTA), specifically, the DIGOTA is the one that occupies the lowest die area, being around 20x smaller than the one proposed in [22]. Although the proposed DIGOTAs couldn't achieve the lowest power consumption amongst the referred OTAs, they still managed to reach a low power down to the nanoWatt range (4.6x lower than [21] for the DIGOTA) except for the FI-DIGOTA which revealed a higher power consumption (μW range). When taking into account the areas of the proposed DIGOTAs, the area-normalized figures of merit ($IFOM_{\mathrm{SA}}$ and $IFOM_{\mathrm{LA}}$) indicate that the DIGOTA (x25 larger than the previous 180nm DIGOTA [20]) and ST-DIGOTA achieve superior metrics due to their minimal area.

IV. Conclusion

In this work, three different ULV DIGOTA topologies, i.e. DIGOTA, ST-DIGOTA and FI-DIGOTA, have been designed in 16 nm FinFET technology and their performance has been compared based on post-layout simulations. The ST-DIGOTA presented an all-round better robustness and better performance, even if the standard DIGOTA achieves the lowest power consumption and best energy efficiency, at the cost of worse GBW and DC Gain. The FI-DIGOTA considered in this analysis showed a higher power consumption (in the µW-range and higher sensitivity to process variations. The DIGOTA and ST-DIGOTA have achieved the best simulated $IFOM_{\mathrm{SA}}$ (1.42 M and 236 k for the DIGOTA and ST-DIGOTA, respectively) and $IFOM_{\mathrm{LA}}$ (117 k and 19.2 k, for the DIGOTA and ST-DIGOTA, respectively) when compared to recent ULV OTAs, presenting a larger values than the ones obtained in the previous study of such topologies [15].

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