The Digital-Based Operational Transconductance Amplifier: Evolution and Perspective

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Pedro Toledo
Synopsys
Lisbon, Portugal
toledo@synopsys.com

Sergio Bampi
PGMICRO, Informatics Institute
Federal University of Rio Grande do Sul
Porto Alegre, Brazil
bampi@inf.ufrgs.br

Paolo Crovetti
Dept. of Electronics and Telecom. (DET)
Politecnico di Torino
Torino, Italy
paolo.crovetti@polito.it

***Abstract*—The evolution of the Digital-Based Operational Transconductance Amplifier (DB-OTA), which was initially introduced to address the challenges related to the implementation of analog functions in aggressively scaled technology nodes is reviewed in this paper, starting from the first proof-of-concept prototype up to the most recent ultra-compact area, ultra-low voltage and ultra-low power solutions. The improvement in performance and the potential of this approach in meeting the requirements of Internet of Things (IoT) sensor nodes and next-generation biosensing will be discussed.**

***Index Terms*—Digital-Based Operational Transconductance Amplifier (DB-OTA), Digital Operational Transconductance Amplifier (DigOTA), Time-Multiplexed Digital Differential Amplification (TMD^{2}A), Ultra-low Voltage (ULV), Ultra-low Power (ULP), Digital-based analog and mixed-signal, Internet of Things (IoT), Biosensors.**

I. Introduction

Analog design in nanoscale CMOS started to be more and more challenging due to the relatively poor analog characteristics of MOSFETs and of the reduction in the analog signal swing imposed by voltage scaling [1], [2]. While many research efforts have been focused on the refinement of traditional analog design techniques, different design approaches, intended to move signal processing from the amplitude to the time domain so that to take advantage as much as possible of the development of the digital-centric IC technology have been proposed [3]–[7].

In this context, the possibility to re-think analog functions in themselves and translate them into digital was suggested. This trend began with the introduction of all-digital PLL [8], synthesizable A/D converters (ADCs) [9], digital low-dropout regulators (LDOs) [10], digital-based comparators [11], voltage references [12] and buck converters [13].

In this context, the Digital-Based Operational Transconductance Amplifier (DB-OTA) was first conceptualized in 2013 with the aim of providing a systematic, scaling-friendly, fully-digital realization of the traditional analog OTA, which is a ubiquitous building block in analog ICs [14].

In the subsequent decade, the application landscape has witnessed the emergence of the Internet of Things (IoT) paradigm and of a new generation of biosensors, among the others. In both contexts, energy autonomous integrated systems with a size in the (sub)-mm are demanded so that to operated without a direct connection the power grid, relying on the tine amount of energy that can be stored in a mm-range battery or that can be retrieved from the environment small with an energy harvester of the same size. It immediately follows that such applications require ultra-low area and power consumption ICs, which need to operate under an extremely variable and often poorly controlled supply voltage.

While the requirements of energy-autonomous Internet of Things (IoT) nodes [15] and next-generation biosensing [16] are not compatible of traditional analog ICs, which draw a static power to operate transistors in their dc bias point, the digital-based approach and the DB-OTA circuit in particular, have more and more proved to be a viable solution for the implementation of analog and mixed-signal functions.

This paper provides an overview of the evolution of DB-OTA implementations, highlighting current advances and future perspectives. The paper is organized as follows. Firstly, the DB-OTA concept is introduced, and the first proof-of-concept DB-OTA prototype based on commercial off-the-shelf components is described. The paper then dives into the first DB-OTA silicon implementations, discussing both the basic topology and its passive-less evolution based on Muller C-element gates. The potential of this approach as an ultra-low voltage, ultra-low power technique for IoT applications is highlighted. Moreover, the recent adoption of the DB-OTA principle in the time-multiplexed differential amplification (TMD^{2}A) technique is described, which offers a unique way to design a Digital-Based low frequency acquisition front-end with inherent analog-to-digital conversion with high DC accuracy without using chopping and auto-zeroing. Following, the paper goes on to provide an overview of recent applications of the DB-OTA concept in the design of a charge amplifier, a potentiostat, and a biosignal amplifier targeting Body Dust applications. Additionally, the portability of this technology in emerging Indium-Gallium-Zinc-Oxide (IGZO) Flexible Thin-Film Transistor technology is discussed. Finally, the paper offers some general comments on the strengths and weaknesses of the BD-OTA and presents future perspectives of this technology.

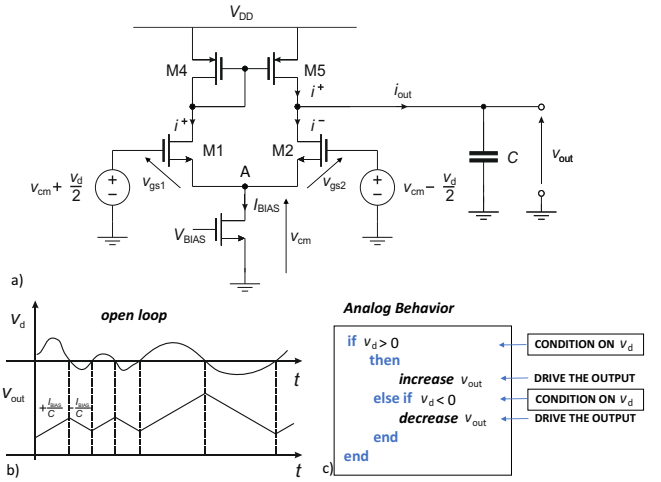

Fig. 1. A CMOS differential pair.

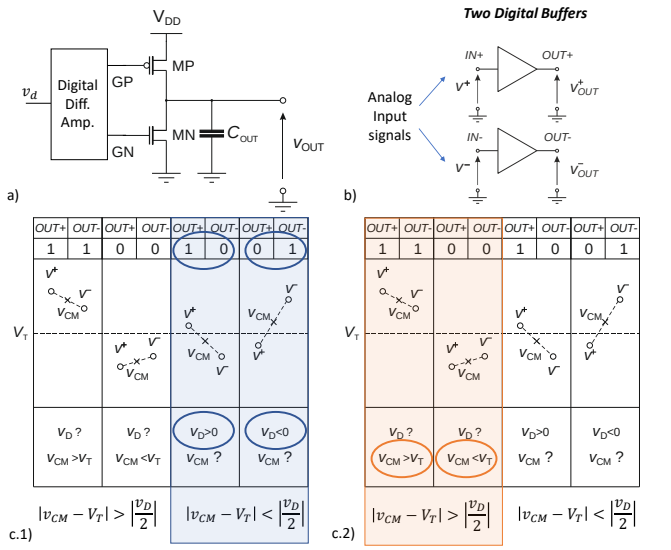

Fig. 2. a) DB-OTA output stage b) a pair of single-ended digital buffers as a digital differential stage c) digital output configurations and implications on DM and CM input signals from [14]

II. A Differential Pair as a Digital Circuit

The Digital-Based Operational Transconductance Amplifier (DB-OTA) is intended as a digital replacement of the simplest Operational Transconductance Amplifier (OTA) based on an MOS differential pair shown in Fig.1, and which could effectively mimic its analog behavior in a negative feedback configurations.

The DB-OTA design starts by abstracting the analog OTA functionality, which can be described with reference to Fig.2(a). Here, the output capacitance C is driven by a current $i_{\rm out} = g_{\rm m} v_{\rm d}$ that is proportional to the input differential signal $v_{\rm d} = v^+ - v^-$, while being independent of the common-mode input $v_{\rm cm} = (v^+ + v^-)/2$, and is converted into the output voltage

$$v_{\rm out} = \frac{g_{\rm m}}{C} \int_0^{t'} v_{\rm d}(t')dt' \qquad (1)$$

In this configuration, common-mode independence is achieved since the voltage at the common-source node A tracks the common-mode input voltage, which is then subtracted from the external input signals appearing in the gate-source voltages $v_{\rm gs1}$ and $v_{\rm gs2}$ of the input devices M1 and M2. Assuming that M1 and M2 are matched, biased in the saturation region, and neglecting the channel length modulation and the Drain-Induced Barrier Lowering (DIBL) effects, the drain currents i^+ and i^- are a function of $v_{\rm gs1}$ and $v_{\rm gs2}$ only, and therefore are insensitive to common-mode variations, resulting in an output current $i_{\rm out}$ that is purely proportional to $v_{\rm d}$.

When the OTA transconductance $g_{\rm m}$ approaches infinity, which is highly desirable to boost the loop gain in negative-feedback configurations, the differential pair bias current $I_{\rm BIAS}$ is steered with positive (negative) polarity to the output capacitance C. This causes the output voltage to increase (decrease) depending on the positive (negative) sign of $v_{\rm d}$, as shown in Fig. 1(b). As a result of this analysis, the analog behavior of an idealized OTA can be described by the pseudo-code in Fig. 1(c).

The pseudo-code in Fig. 1(c) suggests that the function of an analog OTA can be emulated by a digital circuit capable of detecting the polarity of the input differential voltage and driving the output capacitor with a positive or negative current.

In detail, to detect the polarity of the differential input voltage, a pair of digital buffers with an ideal threshold behavior and identical trip point $V_{\rm T}$ (see Fig.2(b)). Indeed, when the buffer logical outputs OUT^+ and OUT^- have different values (this condition is equivalent to $|v_{\rm cm} - V_{\rm T}| < |v_{\rm d}/2|$, see Fig.2(c1)), the sign of $v_{\rm d}$ is immediately inferred. Based on this information, a three-state buffer (see Fig.2(a)) can be driven either to charge or to discharge C thus immediately reproducing the analog OTA behavior.

On the other hand, when $OUT^+ = OUT^-$, i.e., if $|v_{\rm cm} - _{\rm T}| > |v_{\rm d}/2|$, the sign of $v_{\rm d}$ cannot be inferred (see Fig. 2(c2)). However, if OUT+ = 1 and OUT− = 1 (OUT+ = 0 and OUT− = 0), it can be concluded that $v_{\rm CM} > V_{\rm T}$ ($v_{\rm CM} < V_{\rm T}$), and this information can be utilized to drive a second three-state buffer (i.e., the CM Extractor circuit in Fig.3 (a)), so that to track the common-mode component and subtract them from the external inputs to enforce $OUT^+ \neq OUT^-$, thus implementing a common-mode compensation mechanism which closely resembles what has been described above with reference to the differential pair in Fig.1(a).

III. Early Digital-Based OTA Implementations

The DB-OTA circuit depicted in Fig.3(a) was designed in [14] based on the previous behavioral description of the analog OTA. The circuit includes digital input buffers, output and CM-Extractor stages, driven by combinational logic and a resistive summing network. Its purpose is to sum the CM-compensation voltage $v_{\rm CMP}$ to the analog external inputs. In

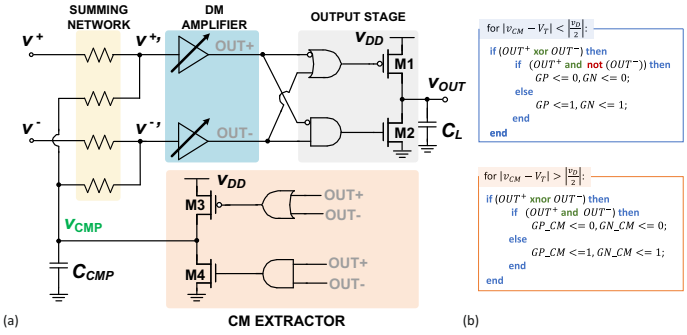

Fig. 3. a) A digital-based differential circuit. b) pseudo-code that control the amplification of the differential input signal (UP code) and pseudo-code that that controls CM tristate inverter for CM signal tracking.

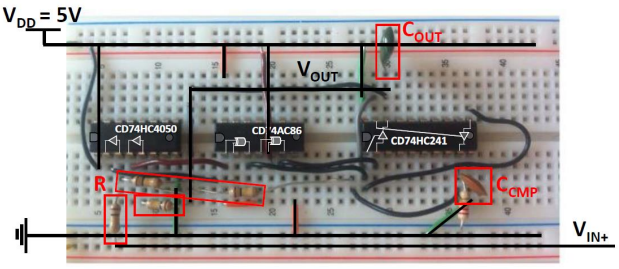

Fig. 4. Proof-of-concept implementation of the digital-based differential circuit, connected in the voltage follower configuration using the off-the-shelf digital component [14].

Fig.3(b), pseudo-codes governing the output and CM three-state inverters are also provided.

The circuit was implemented by off-the-shelf components (Fig. 4) and tested in the voltage follower configuration. Despite its poor analog performance, the paper suggests that better performance could be achieved for a fully integrated and properly designed circuit. Additionally, the DB-OTA has been proven to have high EMI immunity [17] and has been used in open-loop mode as a voltage comparator [11].

The DB-OTA has been demonstrated on silicon in 2019 [20] and 2021 [18], as depicted in Figs. 5(a) and 5(b).

The performance of the DB-OTA silicon implementations illustrated in Figs. 5(c) and 5(d), revealed the potential of the DB-OTA as an ultra-low voltage (ULV) and energy-efficient amplifier, achieving a record-low power consumption of 591 pW at 300 mV V_{DD}, a compact area of 1,426 $\mu\mathrm{m}^2$, and an energy-efficiency figure of merit $FOM_S = 100\,\frac{GBW \cdot C_{\mathrm{OUT}}}{I_{\mathrm{DD}}} = 2,101\,\mathrm{V}^{-1}$, where $C_{\mathrm{OUT}} = 80\,\mathrm{pF}$ and $GBW = 518\,\mathrm{Hz}$.

IV. Standard-Cell Based Digital OTA (DigOTA)

In [19], the original DB-OTA topology has been modified replacing the resistive summing network used for CM compensation with two Muller C-elements, which are commonly used in asynchronous digital circuits [21]. The inputs of the Muller C-elements are connected to both the external OTA inputs and the output of the CM-compensation network. Their outputs, namely $v_{\mathrm{MUL+}}$ and $v_{\mathrm{MUL-}}$, drive a pair of digital inverters

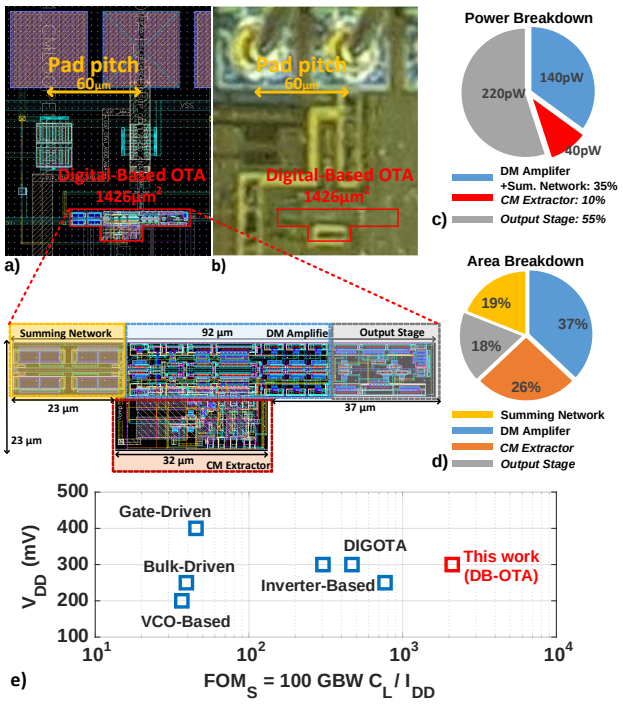

Fig. 5. a) DB-OTA [18] layout total area of 1,426 $\mu\mathrm{m}^2$ b) micrograph of the 180-nm test-chip c) power breakdown d) area breakdown e) V_{DD} vs. FOM_S.

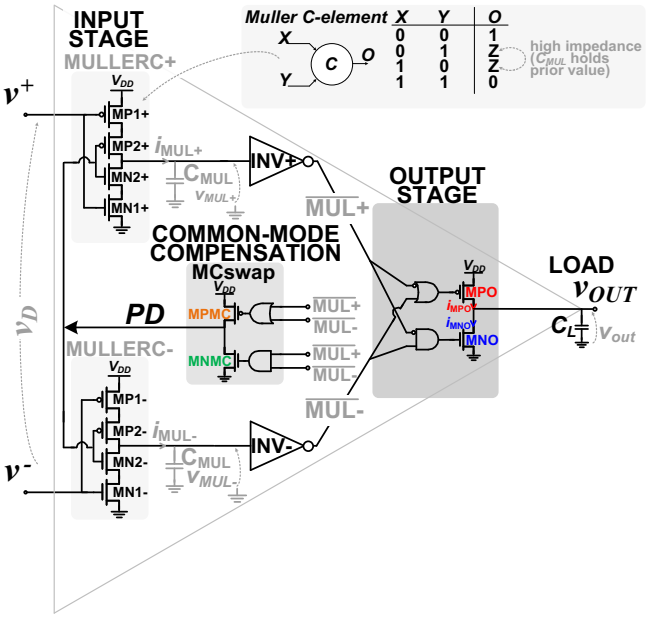

Fig. 6. DigOTA schematic [19].

similar to the digital buffers in the basic DB-OTA in Fig. 3. The CM compensation and output stages remain analogous to the DB-OTA and are operated based on the inverter digital outputs $\overline{\mathrm{MUL}_+}$ and $\overline{\mathrm{MUL}_-}$, following the DB-OTA logic in Fig. 2(c).

By eliminating the resistive summing network, this tech-

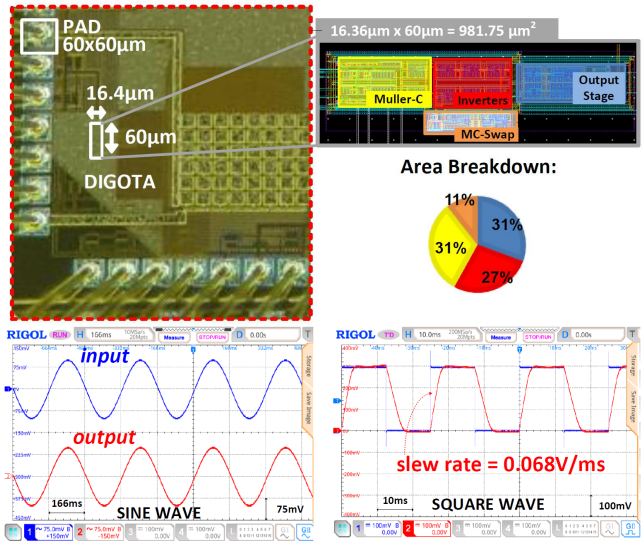

Fig. 7. a) Micrograph of the DigOTA 180 nm testchip; b) area and power breakdown, c) minimum VDD vs. FoM for recently proposed ULV OTAs.

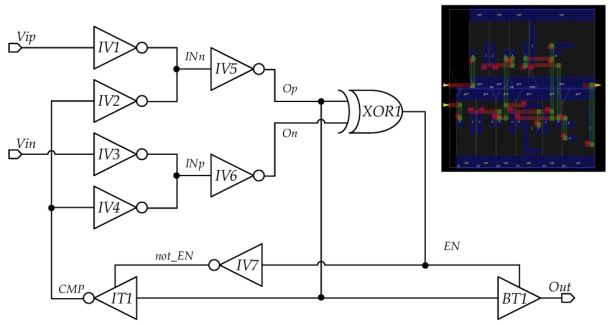

Fig. 8. Schematic and layout of the Standard-cell Based DigOTA proposed in [22].

nique results in a fully-synthesizable design that is compatible with a digital standard cell flow. Furthermore, it exhibits reduced input-referred noise and improved resilience against mismatch and process variations, while maintaining a low power consumption in the nW range and a supply voltage of 300 mV.

The DigOTA test-chip presented in [19] has a compact footprint of only 982 μm^2 in 180 nm CMOS. Fig.7 shows the measured response of the DIGOTA circuit operating in the voltage follower configuration under a low supply voltage of 300 mV, which is directly generated by a miniature solar cell [19]. Under these extreme conditions, the DIGOTA cell is still capable to drive a heavy capacitive load of 150 pF with a DC gain of 30 dB, a gain-bandwidth product (GBW) of 250 Hz, and a phase margin of 90°. The measured CMRR and PSRR are 41 dB and 30 dB, respectively. These results demonstrate the potential of DIGOTA in pure harvested IoT nodes and next-generation biosensors.

In [22] a different fully-synthesizable, standard-cell-based, DigOTA implementation has been proposed. The schematic and the automatically generated layout of the circuit are shown

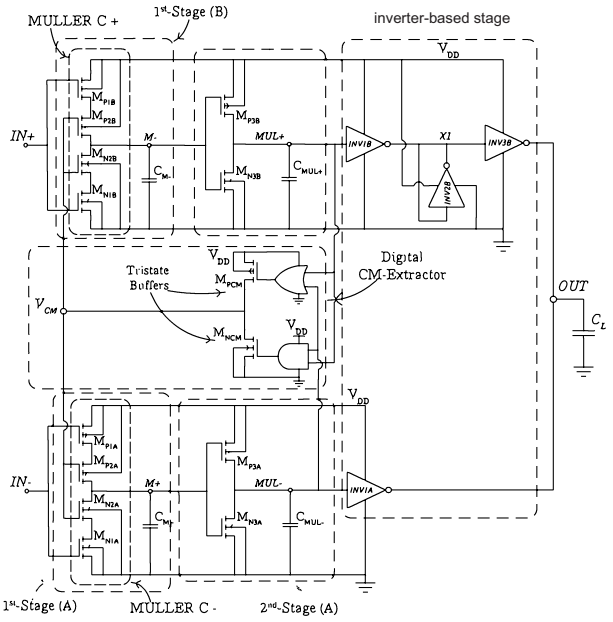

Fig. 9. Hybrid DigOTA circuit proposed in [23].

in Fig.8. In essence, in this variant, the CM extractor is implemented through the XOR1, the IV7 and the IT1 gates, as in the proof-of-concept prototype in [14], and generates a common mode compensation signal CMP which is added to the external inputs in the current domain via the inverters IV1, IV2, IV3 and IV4. The circuit has been tested by simulations in 130 nm, revealing 87 dB DC gain and 3.15 kHz GBW while consuming 8.2μm at 0.55 V power supply.

V. Hybrid Digital OTAs and DigOTA-related approaches

To overcome the DC accuracy limitations of the initial DB-OTA, a hybrid DigOTA topology has been reported in [23]. Compared to previous solutions, it features an inverter-based third amplifying stage. The hybrid solution enables a 66-dB gain at 0.3-V power supply and a GBW product increased to 12.3 kHz under a 250 pF capacitive load. These specifications, together with the average power consumption around 44nW and the area occupation of 625 μm, leading to improved area-normalized small-signal and large-signal FOMs by a factor 4.6X and 1.5X, respectively compared to previous DigOTA implementations.

Interestingly, in the same paper [23], the possibility to describe the DigOTA operation by a simplified, analog-like, small-signal model extracted assuming mid-range analog inputs has been validated by simulations. The introduction of the simplified small-signal model paves the way to Miller-based compensation topologies, typically adopted in conventional multistage OTAs. A more accurate analysis, which takes into account of the time-varying, digital-like DigOTA operation, has also been proposed in

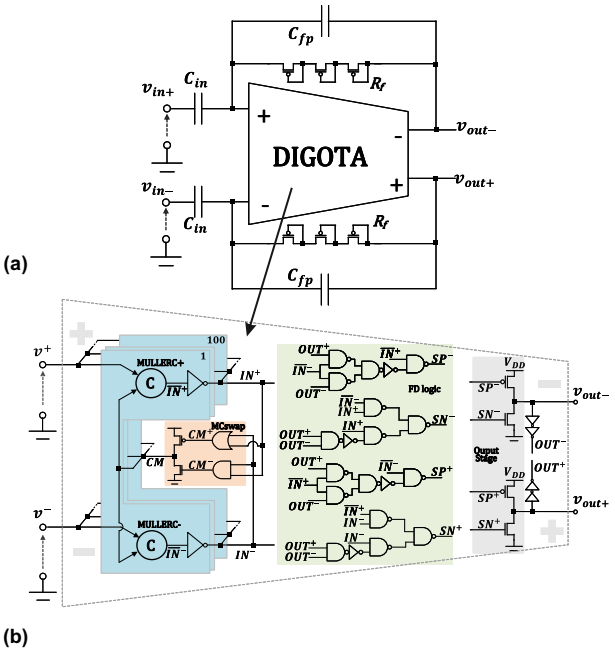

Fig. 10. a) BioDIGOTA schematic b) fully differential DIGOTA [24].

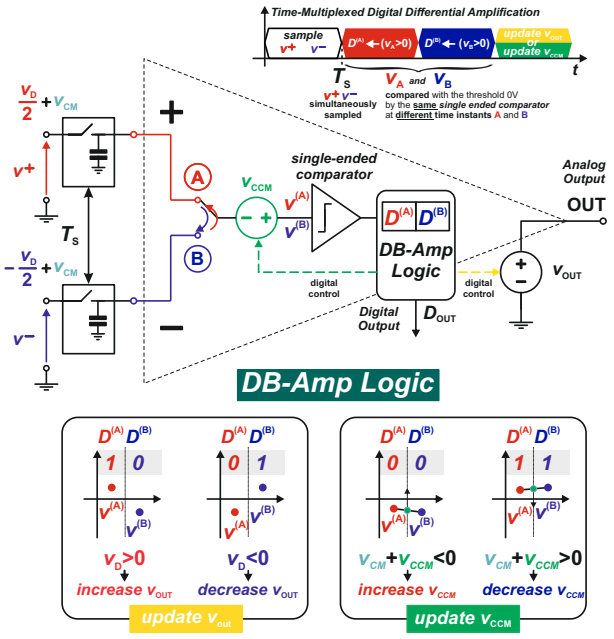

Fig. 11. a) Switched-capacitor and time multiplexed DB-OTA b)state transition graph of the DB-Amp control unit [25].

VI. DIGOTA FOR BIOSIGNAL ACQUISITION (BIODIGOTA)

In [24], a fully-differential (FD) BioDigOTA aimed at biosignal acquisition has been proposed. The full schematic of the AC-coupled biosignal amplifier, which targets electrocardiogram (ECG) signals, is depicted in Fig.10. The proposed FD-DIGOTA includes a noise-optimized Muller-C-based input stage, two inverters, an MCswap common-mode compensation, its internal combinational logic, and an output stage including two three-state inverters. Similar to the DIGOTA, the differential output voltage is also increased/decreased based on the sign of v_{d}. Moreover, two additional inverters are included to sense the CM output and compensate it independently of the CM input.

The BioDigOTA was designed and fabricated in 180 nm CMOS. Its feedback network comprises Metal-insulator-Metal (MiM) on-chip capacitors and MOS-based pseudo-resistors (C_{in}, C_{fp}, R_{f} in Fig. 10). The BioDigOTA was measured at $V_{DD} = 400\,\mathrm{mV}$ and, for a 3 Hz input frequency, it operated as a filter with less than 2% Total Harmonic Distortion (THD) and a power consumption of 100 nW. Under these conditions, the BioDIGOTA circuit functioned correctly, producing an output swing of more than 400mV peak-to-peak. The circuit provided a 10 Hz bandwidth at 35 dB gain and more than 12 V/s slew rate under $C_{\mathrm{out}} = 10\,\mathrm{pF}$.

The BioDigOTA's integrated noise over the entire bandwidth (0.05 Hz - 10 Hz) was measured to be 1.25 μV_{RMS}, which corresponds to a Power Spectral Density (PSD) of 395 nV/$\sqrt{\mathrm{Hz}}$. These results correspond to a Noise Efficiency Factor (NEF) of 7.6 and a Power Efficiency Factor (PEF) of 23.

Aiming to address the DC accuracy limitations of BioDIGOTA and of the other DB-OTAs, the Time-Multiplexed Digital Differential Amplification ($\mathrm{TMD}^2\mathrm{A}$) has been proposed in [25] to design a low frequency, nW power Digital-based Acquisition Front-End (DAFE). The $\mathrm{TMD}^2\mathrm{A}$ principle is illustrated in Fig. 11. In $\mathrm{TMD}^2\mathrm{A}$ - in essence - the two digital buffers with matched trip points, that are used to sense the inverting and the non-inverting inputs of the DB-OTA (Fig. 3), are replaced by a single buffer, which is multiplexed in time so that to compare the inverting and non-inverting input voltages, synchronously sampled on the input capacitors, against its trip point, thus inherently suppressing any matching requirements.

VII. DB-OTA IN FLEXIBLE IGZO TECHNOLOGY

Recently, a DB-OTA in a 800 nm Indium-Gallium-Zinc-Oxide (IGZO) Thin-Film Transistors (TFT) Flexible Integrated Circuits (FlexICs) technology has been developed and compared with an analog implementation [26]. Fig.12 shows the schematic and layout of the flexible DB-OTA. The DB-OTA's mostly-digital architecture allowed for easy porting to the 800nm IGZO technology, achieved by replacing CMOS logic gates with nMOS logic gates [27], using minimum-length transistors. It is worth noting that TFT IGZO technology is not a complementary, i.e. it does not allow the integration of p-type devices.

Based on post-layout simulation, the flexible DB-OTA has achieved several impressive performance metrics. Despite maintaining a comparable gain-bandwidth product (GBW) to analog implementations, it has achieved the smallest area and lowest power consumption. Furthermore, the proposed DB-OTA has achieved the best figure of merit (FOM) of 38.05 MHz·pF/mW, owing to its GBW of 86 kHz and its ability to drive a relatively large load of 50 pF while consuming a reasonably low amount of power. It is worth noting that this

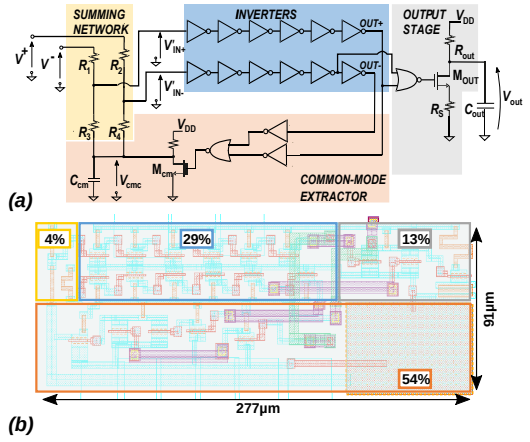

Fig. 12. DB-OTA in flexible IGZO technology: schematic and layout [26].

design also demonstrated one of the best reported slew rate performances in the same technology.

VIII. Comparison and Perspective

Table I summarizes the performance of several DB-OTA-based amplifiers, from the proof-of-concept introduced in [14] to the last solutions. These implementations have demonstrated a steady improvement in performance and/or reduction in size, with areas as small as less than 1,000 μm^2 reported in [19], power consumption as low as less than 600 pW reported in [18], and minimum operating voltage as low as 300 mV reported in [18]–[20].

These achievements demonstrate that DB-OTA-based amplifiers can be compatible with the requirements of energy-autonomous IoT sensor nodes [15] and next-generation biosensing applications [16]. Furthermore, emerging applications in different domains such as charge amplifiers in photodiode readout [28] show further potential.

Despite many improvements, there is still a gap between DB-OTA and traditional analog solutions operating at nominal supply voltage (above 1 V) in terms of DC gain and bandwidth. Addressing this gap will require further research efforts. Nevertheless, it is worth being observed that when aggressively scaled, nanometer technologies and sub-500,mV supply are considered [18]–[20], the gap between DB-OTA and more traditional OTAs almost disappears, and the DB-OTA approach proves to be a highly competitive.

An important aspect of the DB-OTA technology is its compatibility with a fully automated standard cell digital design flow, as demonstrated in all the CMOS prototypes presented in Tab.I, as well as in [22]. While the technologies used in this comparison are relatively mature, this feature will be particularly valuable in aggressively scaled technologies, where manual layout generation is an extremely complex and time-consuming task.

Removing analog device requirements (e.g., matching, intrinsic gain, transconductance, etc.), the DB-OTA approach is

TABLE I
Peformance of DB-OTA implementations

Ref,	Unit	[14]$^+$	[18], [20]$^+$	[19]$^+$	[26]*	[23]*
Date	year	2013	2019	2020	2022	2023
Tech.		Discrete	CMOS	CMOS	IGZO	CMOS
Feat.	nm	N/A	180	180	800	28
Design		gates	stdcell	stdcell	custom	custom
Area	mm^2	-	0.0014	0.00098	0.0252	0.00062
Supply	V	5	0.3	0.3	3.3	0.3
In Range	% V_{DD}	100	100	100	30	93
Power	nW	$165{\cdot}10^6$	0.591	2.4	$113{\cdot}10^3$	44
BW	Hz	100,000	518	250	86,000	12,300
C_{OUT}	pF	22,000	80	150	50	250
DC Gain	dB	30	30	30	36.3	66
In Offset	μV	-	1,100	5,000	7,200	29,080
Noise	$\mu\mathrm{V}_{\mathrm{rms}}$	-	2,900	21	87	88.7
THD	%	3.7	1,26	2	0.31	1.72
Slew Rate	V/ms	100	0.264	0.085	187	3.2
CMRR	dB	30	-	41	45	105
PSRR	dB	35	-	30	39	74
$\mathrm{FOM_S}^{(a)}$	$\frac{\mathrm{MHz{\cdot}pF}}{\mu\mathrm{W}}$	0.013	70.1	15.6	0.038	69.8
$\mathrm{FOM_L}^{(b)}$	$\frac{\mathrm{V/ms{\cdot}pF}}{\mu\mathrm{W}}$	13.33	35,736	5,312	82.74	18.18

$^{(a)}$ $FOM_S = \frac{GBW \cdot C_L}{Power}$, $^{(b)}$ $FOM_L = \frac{SR \cdot C_L}{Power}$, $^+$Measurements, *Simulations

inherently well suited to enable analog and mixed-signal functionalities in virtually any technology in which basic Boolean operations can be implemented. The successful demonstration of a DB-OTA circuit in a flexible IGZO semiconductor technology [26], indeed, has paved the way for exploring its implementation in other beyond-CMOS technologies such as optical computing, spintronics, quantum gates, and more. By extending the DB-OTA approach beyond the realm of CMOS, it is possible to open up new avenues for developing advanced analog circuits and systems that can enable a wide range of exciting applications in the future.

IX. Conclusion

A review of the digital-based amplifiers presented in the litterature has been provided. The analysis highlights that the DB-OTA method is well-suited to implement analog functions that meet the requirements of emerging energy autonomous IoT nodes and biosensing, including ultra-low voltage operation, ultra-low power consumption, and minimal area. Importantly, this is achieved using a fully digital, standard-cell based design flow. The review also outlines the current limitations of the approach and identifies areas for future research.

References

[1] B. Xu, S. Li, N. Sun, and D. Z. Pan, "A scaling compatible, synthesis friendly VCO-based delta-sigma ADC design and synthesis methodology," in *2017 54th ACM/EDAC/IEEE Design Automation Conference (DAC)*, 2017, pp. 1–6.

[2] P. R. Kinget, "Scaling analog circuits into deep nanoscale CMOS: Obstacles and ways to overcome them," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015, pp. 1–8.

[3] P. S. Crovetti, "All-digital high resolution d/a conversion by dyadic digital pulse modulation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 573–584, 2017.

[4] P. Crovetti, F. Musolino, O. Aiello, P. Toledo, and R. Rubino, "breaking the boundaries between analogue and digital," *Electronics Letters*, vol. 55, no. 12, pp. 672–673, 2019. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/el.2019.1622

[5] P. Toledo, R. Rubino, F. Musolino, and P. Crovetti, "Re-thinking analog integrated circuits in digital terms: A new design concept for the iot era," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 3, pp. 816–822, 2021.

[6] R. Rubino, P. S. Crovetti, and F. Musolino, "Fpga-based relaxation d/a converters with parasitics-induced error suppression and digital self-calibration," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 6, pp. 2494–2507, 2021.

[7] P. Toledo, P. Crovetti, H. klimach, and S. Bampi, "Dynamic and static calibration of ultra-low-voltage, digital-based operational transconductance amplifiers," *Electronics*, 2020.

[8] R. B. Staszewski et al., "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, 2004.

[9] J. Park, Y. Hwang, and D. Jeong, "A 0.5V fully synthesizable SAR ADC for on-chip distributed waveform monitors," *IEEE Access*, vol. 7, pp. 63 686–63 697, 2019.

[10] L. Qian et al., "A Fast-Transient Response Digital Low-Dropout Regulator With Dual-Modes Tuning Technique," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 2943–2947, 2020.

[11] A. Singh, A. Goel, and A. Agarwal, "A Digital-Based Low-Power Fully Differential Comparator," *Journal of Circuits, Systems and Computers*, vol. 26, no. 01, p. 1750002, 2017.

[12] P. S. Crovetti, "A digital-based virtual voltage reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 5, pp. 1315–1324, 2015.

[13] V. C. Krishna Chekuri et al., "A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process," in *2020 IEEE Custom Integrated Circuits Conference (CICC)*, 2020, pp. 1–4.

[14] P. S. Crovetti, "A Digital-Based Analog Differential Circuit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 12, pp. 3107–3116, 2013.

[15] M. Alioto, "From less batteries to battery-less alert systems with wide power adaptation down to nws—toward a smarter, greener world," *IEEE Design Test*, vol. 38, no. 5, pp. 90–133, 2021.

[16] S. Carrara, "Body dust: Well beyond wearable and implantable sensors," *IEEE Sensors Journal*, pp. 1–1, 2020.

[17] A. Coccoli, A.Richelli, and J.-M. Redouté, "Emi susceptibility of a digitally based analog amplifier in a 180-nm cmos process," *IEEE Transactions on Electromagnetic Compatibility*, vol. 58, no. 4, pp. 1236–1239, 2016.

[18] P. Toledo, P. Crovetti, H. Klimach, S. Bampi, O. Aiello, and M. Alioto, "300mV-Supply, sub-nw-power Digital-Based Operational Transconductance Amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2021.

[19] P. Toledo, P. Crovetti, O. Aiello, and M. Alioto, "Fully-Digital Rail-to-Rail OTA with Sub-1,000 μm^2 Area, 250-mV Minimum Supply and nW Power at 150-pF Load in 180nm," *IEEE Solid-State Circuits Letters*, pp. 1–1, 2020.

[20] P. Toledo, P. Crovetti, H. Klimach, and S. Bampi, "A 300mV-Supply, 2nW-Power, 80pF-Load CMOS Digital-Based OTA for IoT Interfaces," in *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2019, pp. 170–173.

[21] J. M. Emmert and S. A. VanDewerker, "Emc: Efficient muller c-element implementation for high bit-width asynchronous applications," in *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2021, pp. 816–819.

[22] G. Palumbo and G. Scotti, "A Novel Standard-Cell-Based Implementation of the Digital OTA Suitable for Automatic Place and Route," *Journal of Low Power Electronics and Applications*, vol. 11, no. 4, 2021. [Online]. Available: https://www.mdpi.com/2079-9268/11/4/42

[23] M. Privitera, P. Crovetti, and A. D. Grasso, "A novel digital ota topology with 66-db dc gain and 12.3-khz bandwidth," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 11, pp. 3988–3992, 2023.

[24] H. K. P. Toledo, P.S. Crovetti, F. Musolino, and S. Bampi, "Low-Voltage, Low-Area, nW-Power CMOS Digital-Based Biosignal Amplifier," *IEEE Access*, vol. 10, pp. 44 106–44 115, 2022.

[25] P. Crovetti, R. Rubino, P. Toledo, F. Musolino, H. Klimach, Y. Chen, and A. Richelli, "A 0.01mm2, 0.4v-vdd, 4.5nw-power dc-coupled digital acquisition front-end based on time-multiplexed digital differential amplification," in *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC)*, 2022, pp. 405–408.

[26] S. Adibi, R. Rubino, P. Toledo, and P. Crovetti, "Design of an analog and of a digital-based ota in flexible integrated circuit technology," in *2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2022, pp. 1–4.

[27] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, 3rd ed. USA: Prentice Hall Press, 2008.

[28] Y. Song, S. Smith, B. Karlinsey, A. R. Hawkins, and S.-H. W. Chiang, "The Digital-Assisted Charge Amplifier: A Digital-Based Approach to Charge Amplification," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 8, pp. 3114–3123, 2022.