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Online Monitoring and Correction Method of Threshold Voltage in SiC MOSFET Power Cycling Test

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Abstract

This paper presents an online monitoring and correction method of threshold voltage in SiC MOSFET power cycling test. The results of online monitoring of threshold voltage are coupled with both the effect of the degradation of SiC MOSFET chip and the effect of junction temperature variation caused by the degradation of the package. The proposed correction method can eliminate the influence of the junction temperature variation. And the effect of the chip degradation on the threshold voltage can be well reflected in the corrected results. The experimental results prove the effectiveness of the proposed method.

1. Introduction

Wide-gap semiconductor power devices represented by SiC MOSFET have been widely used due to their superior performance such as high switching frequency and high operating temperature [1]. Meanwhile, the reliability of SiC MOSFET has also attracted a lot of attention [2-3].

The failure of silicon power devices is mostly caused by the degradation of the package, especially the bonding wires and the solder layer [4]. SiC MOSFET has a unique chip-related failure mode due to the reliability of the gate oxide layer [5-6]. Under positive gate bias, electrons in the channel tunnel into the oxide and are trapped by the near-interface oxide traps. The accumulation of electrons in the oxide weakens the electric field. In order to form the inversion layer, a larger gate bias is required. Therefore, there is a positive shift in the threshold voltage. As a result, the threshold voltage can be utilized as an aging precursor to monitor the condition of the SiC MOSFET chip.

The power cycling (PC) test passes intermittent current to the device under test (DUT), which makes the DUT continuously switch between heating state and cooling state, thereby accelerating the aging of DUT. By performing online monitoring of threshold voltage in the PC test, the degradation mechanism and law of SiC MOSFET chip can be explored.

In this paper, a novel online monitoring method of threshold voltage in SiC MOSFET power cycling test is proposed. In addition, a correction method is proposed in this paper to eliminate the effect of junction temperature rise caused by package degradation on online measurement.

The remainder of this paper is organized as follows. Section II introduces the proposed online measurement and correction method of threshold voltage. Then, Section III introduces experimental setup for PC test of SiC MOSFET. In Section IV, the online measurement results of threshold voltage and the corresponding correction results is shown. The test results show that the PC test causes a 25mV increase of threshold voltage for the experimental 1200V/63A SiC MOSFET and a 58mV increase of threshold voltage for the experimental 650V/23A SiC MOSFET. Finally, Section V concludes this article.

2. Online monitoring and correction methods for threshold voltage

2.1. Effect of junction temperature variation on threshold voltage measurement results

Threshold voltage can be measured by shorting the gate and the drain and injecting a mA-level current

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into the drain. The measurement can be arranged at the end of cooling stage of each PC test cycle, when the junction temperature has nearly stabilized.

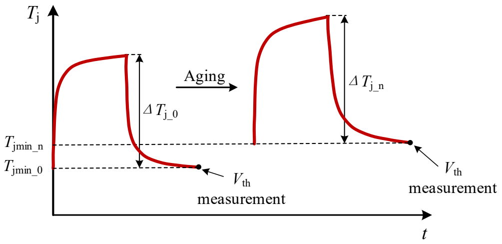


Fig. 1. Variation of junction temperature during PC test.

During the PC test, with the degradation of SiC MOSFET chip and package, the junction temperature fluctuation curve in a PC test cycle changes as shown in Fig. 1. On the one hand, the degradation of the solder layer in the package leads to an increase in the thermal resistance. On the other hand, due to the degradation of the SiC MOSFET chip, the conduction loss in each PC test cycle increases gradually. The conduction loss of the device can be expressed as:

$$P_{loss} = V_{DS} I_{load} = \frac{I_{load} L_{CH}}{Z \mu_{in} C_{ox}} \frac{1}{(V_{gs} - V_{th})} \bullet I_{load} \tag{1}$$

where V_{DS} is the on-state voltage, I_{load} is the load current, L_{CH} is the length of channel, Z is the width of channel, μ_{in} is the channel mobility, C_{ox} is the oxide layer capacitance, V_{gs} is the gate-source voltage and V_{th} is the threshold voltage. With the degradation of the gate oxide of SiC MOSFET chip, threshold voltage shifts gradually and positive threshold voltage shift leads to higher conduction loss.

In summary, under the combined influence of package degradation and chip degradation, both the minimum junction temperature T_{jmin} and junction temperature swing ΔT_j of the device in PC test will increase.

This phenomenon also affects the online monitoring of threshold voltage. As shown in Fig. 1, the measurement of threshold voltage is scheduled at the end of the cooling stage in each PC test cycle. At the beginning of the PC test, the corresponding device temperature during the threshold voltage measurement is T_{jmin_0}. Due to the degradation of the device, T_{jmin} gradually rises to T_{jmin_n}. Therefore, considering the temperature-sensitive characteristics of the threshold voltage, the shift of the threshold voltage measured online is coupled with the effect of the degradation of chip gate oxide layer and the effect of temperature variation caused by degradation of package. Therefore, in order to explore the effect of chip degradation on the threshold voltage, the effect of junction temperature variation should be eliminated.

2.2. Online monitoring and correction methods of threshold voltage

Since the voltage drop of body diode V_{SD} under mA level current injection is a temperature sensitive electrical parameter (TSEP), the junction temperature can be measured by measuring V_{SD} combined with the V_{SD}-T_j relationship obtained by pre-calibration. Fig. 2 shows the change of device junction temperature in a single PC test cycle. From t_0~T, the device is turned off, and T_j continues to decrease and gradually stabilizes.

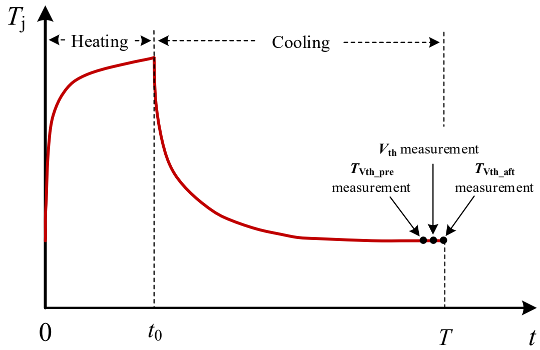


Fig. 2. Arrangement of sampling in each PC test cycle.

Since T_j changes slowly at the end of the cooling stage, the corresponding junction temperature T_{Vth} at the moment of threshold voltage measurement can be obtained by measuring the junction temperature once before and after the threshold voltage measurement T_{Vth_pre} and T_{Vth_aft}. Since the measurement interval is short, T_{Vth} can be calculated using the following equation:

$$T_{Vth} = \frac{T_{Vth\_pre} + T_{Vth\_aft}}{2} \tag{2}$$

The sampling arrangement in each PC test cycle is shown in Fig. 2.

The threshold voltage can expressed as [7]

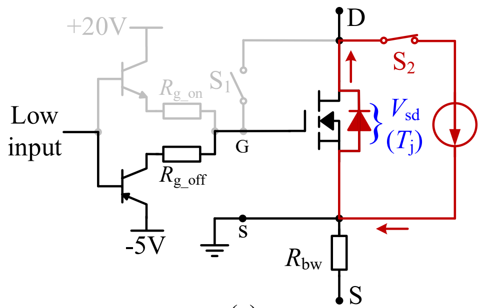
$$V_{th} = \phi_{ms} - \frac{(Q_f - qN_{it})}{C_{ox}} + 2\varphi_B + \frac{\sqrt{4\varepsilon q N_A \varphi_B}}{C_{ox}} \tag{3}$$

where Φ_{ms} is the metal-semiconductor work function difference, Q_f is the density of fixed charge in the oxide layer, N_{it} is the interfacial charge density, φ_B is the potential difference between Fermi level and intrinsic Fermi level, ε is the relative dielectric constant of silicon carbide, q is the elementary charge, *and* N_A is the doping density.

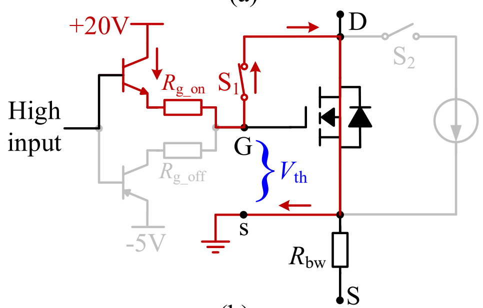
Threshold voltage and temperature have a nearly linear relationship [8]. Therefore, the threshold voltage can be corrected by the following equation to decouple the effect of temperature variation

$$V_{th}(k,T_0)=V_{th}(k,T_{Vth}(k))+\frac{dV_{th}}{dT_j}\bullet(T_0-T_{Vth}(k)) \tag{3}$$

where k represents the number of cycles when these data measured, T_0 is the reference temperature, $V_{th}(k, T_0)$ is the threshold voltage after correcting the temperature to T_0, $T_{Vth}(k)$ is the online monitoring results before correction, $V_{th}(k, T_{Vth}(k))$ is the threshold voltage measured online before correction.



(a)



(b)

Fig. 3. States of measuring circuit.

Fig. 3 (a) shows the state of the measuring circuit under junction temperature measurement. A -5V gate bias is applied to enable the reliable close of the channel when performing junction temperature measurement. Meanwhile, auxiliary switch S_1 is turned off and S_2 is turned on. The SiC MOSFET body diode voltage drop can be obtained by measuring the voltage drop V_{SD} from kelvin source to drain.

Fig. 3 (b) shows state of the measuring circuit under threshold voltage temperature measurement. S_1 is turned on to short the gate and drain. The positive gate bias and a kΩ-level R_{g_on} can inject a mA level measurement current into the drain. The path of measurement current is shown by the red lines in Fig. 3. (b).

3. Experimental setup

The measuring system is shown in Fig. 4. The gate drivers and measurement current source connect to the adapter board with pin headers. Each gate driver controls a single SiC MOSFET chip and monitors the aging precursors. The adapter board supplies power to each gate driver through PCB trace. NI (National Instruments) compactRIO controller sends digital signals to control the DUT and collects aging precursors for condition monitoring. The measurement system connects to the DUT through the data cable on the left side of the adapter board.

Fig. 5 shows the connection of the DUTs.

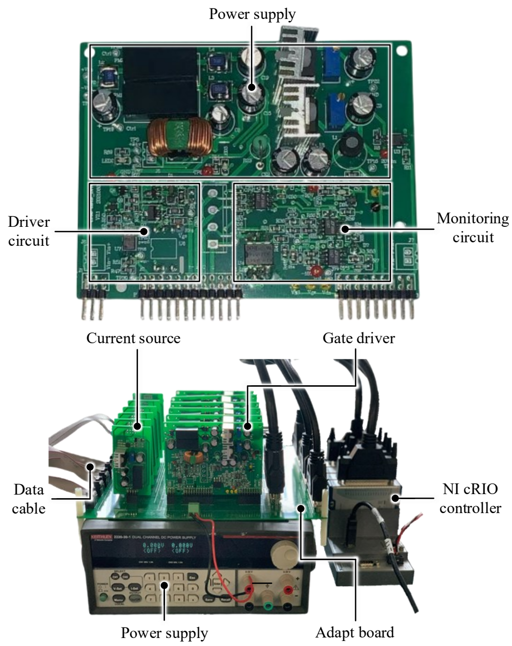


Fig. 4. Measuring system.

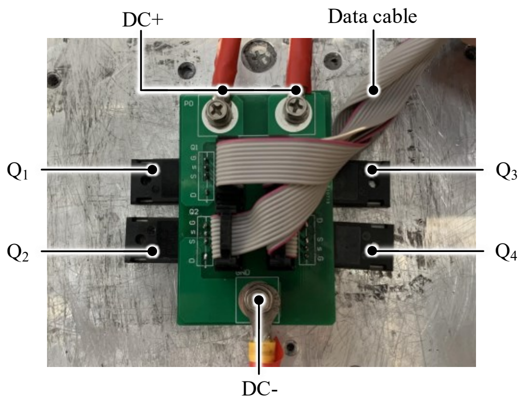
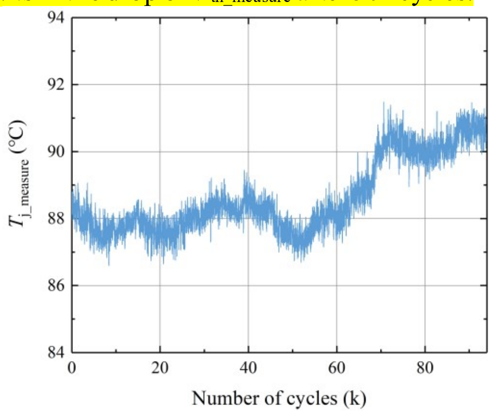


Fig. 5. Device under test.

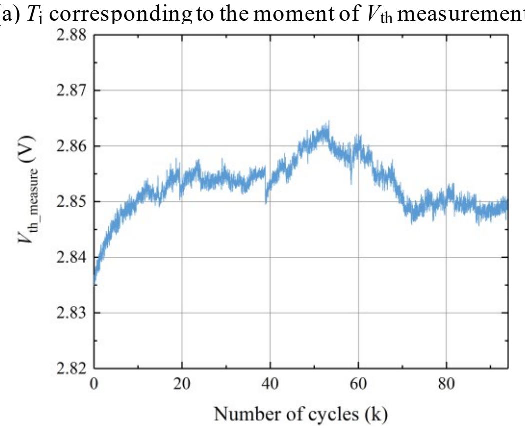
4. Experimental results

Fig. 6 to Fig. 9 are the test results of a 1200V/63A

SiC MOSFET. Fig. 6 (a) shows the junction temperature corresponding to the moment of threshold voltage measurement ($T_{j\_measure}$). Since the measurement of threshold voltage is arranged at the end of the cooling stage in each PC test cycle, $T_{j\_measure}$ is close to T_{jmin}. And Fig. 6 (b) shows the online measurement results of threshold voltage ($V_{th\_measure}$). $V_{th\_measure}$ is influenced both by the degradation of the gate oxide layer of SiC MOSFET chip and the variation of $T_{j\_measure}$. In the first 40k PC test cycles, the positive shift of $V_{th\_measure}$ is mainly caused by the degradation of the SiC chip and $T_{j\_measure}$ changes slightly during this period. After 50k PC test cycles, there is a significantly increase in $T_{j\_measure}$ and this results in the drop of $V_{th\_measure}$ after 50k cycles.



(a) T_j corresponding to the moment of V_{th} measurement



(b) V_{th}

Fig. 6. Online measurement results of $T_{j\_measure}$ and $V_{th\_measure}$.

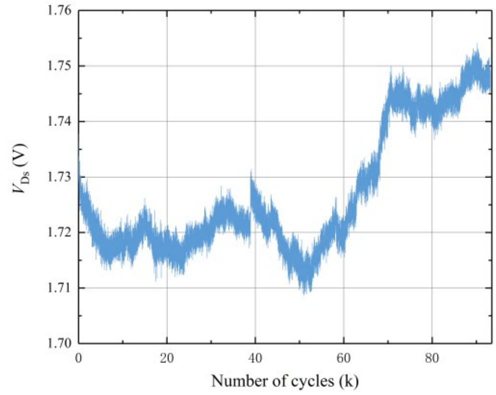


Fig. 7. Online measurement results of V_{Ds}

Fig. 7 shows the online monitoring results of on-state voltage V_{Ds} (voltage drop from drain to kelvin source). Due to the positive temperature characteristics of V_{Ds}, both the positive threshold voltage shift and the junction temperature rise caused by the package degradation will increase V_{Ds}. Since the degradation of threshold voltage is at mV level, the evolution of V_{Ds} is mainly caused by the junction temperature rise caused by package degradation.

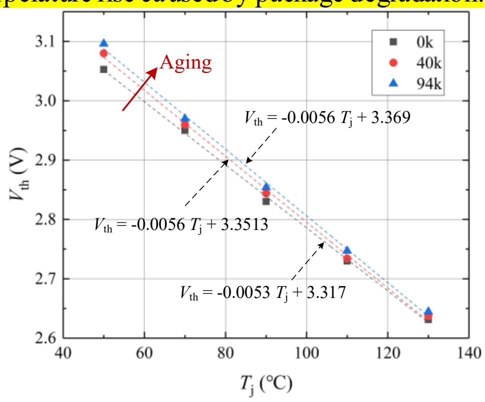


Fig. 8. Calibration results of V_{th}-T_j relationship.

In order to decouple the influence of $T_{j\_measure}$ variation from the online measurement results of threshold voltage, calibrations of the relationship between V_{th} and T_j are performed when the PC test cycle is 0k, 20k, 40k, 60k, 80k and 94k, respectively. And Fig. 8 shows part of calibration results (0k, 40k and 94k).

The temperature sensitivity coefficient of the threshold voltage under different PC test cycles can be obtained from the offline calibration results. The data of Fig. 6 (b) is corrected using equation (3), where the junction temperature uniformly corrected to 90°C, and the correction results is shown in Fig. 9.

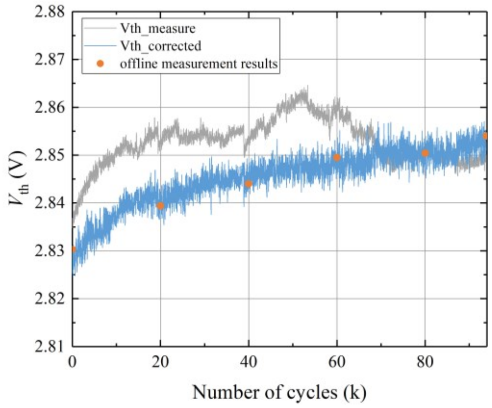
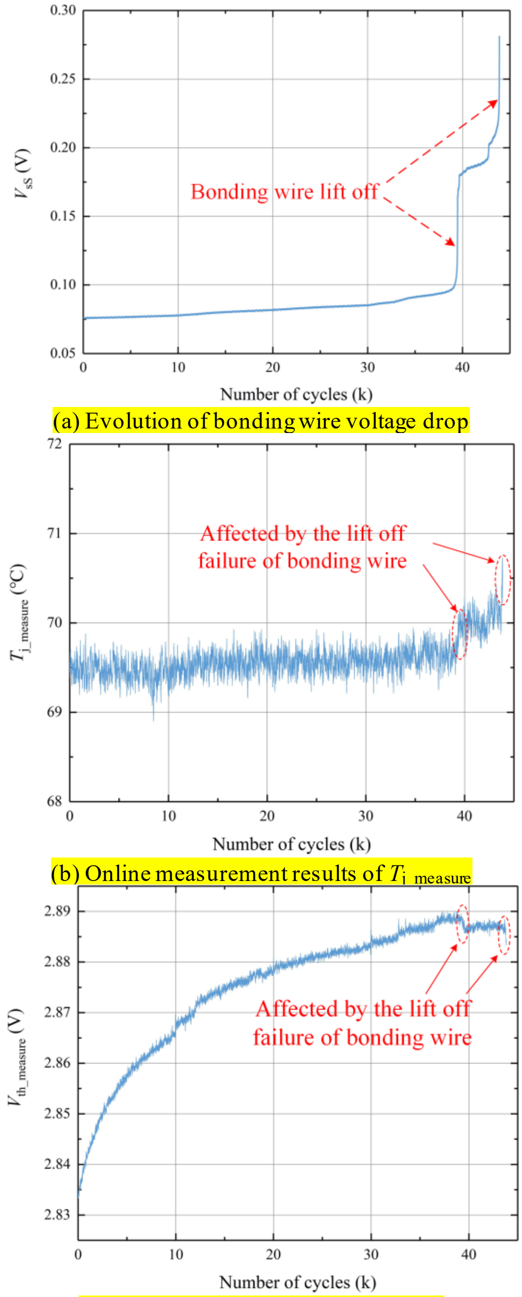


Fig. 9. Results after correction of threshold voltage.

The grey line in Fig. 9 is the result of online measurement of the threshold voltage, which is affected by the temperature difference and cannot well reflect the influence of the degradation of the SiC MOSFET chip on the threshold voltage. The blue line in Fig. 9 is the corrected results. The orange points are the offline calibration results. The calibration results are consistent with the corrected results, which shows the effectiveness of the proposed threshold voltage online measurement and correction method. Test results show that the degradation of the SiC MOSFET chip increases the threshold voltage by about 25mV after 94k PC test cycles.

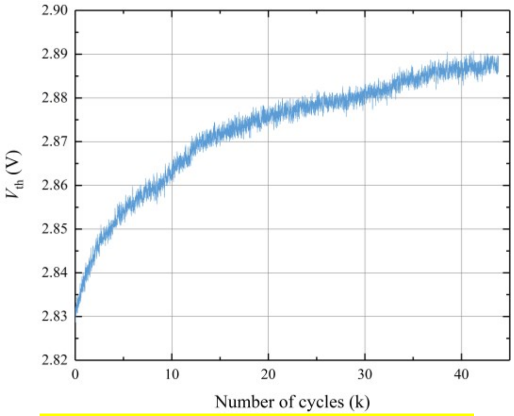
To further verify the effectiveness of the proposed method, a 650V/23A SiC MOSFET is also tested. The test results are shown in Fig. 10. The bonding wires of the device lift off when the test cycles are 39.5k and 43.9k respectively, which can be obtained from the jump of bonding wire voltage drop shown in Fig. 10. (a). The package of selected device is TO247-4, so the bonding wire voltage drop can be obtained by measuring the voltage drop between the kelvin source to power source [9]. The lift off failure of the bonding wires increases the conduction power loss, thereby increasing the junction temperature. As shown in Fig. 10. (b), the junction temperature rises after the failure of bonding wires. The online monitoring results of threshold voltage show a drop due to the increasing of junction temperature as Fig. 10. (c) shows. Fig. 10. (d) shows the results after correcting the junction temperature to 70°C. It can be obtained that the proposed method is also effective in eliminating the effect of the bonding wire lift off failure.



(a) Evolution of bonding wire voltage drop

(b) Online measurement results of $T_{j\_measure}$

(c) Online measurement results of V_{th}



(d) Evolution of V_{th} with T_j corrected to 70°C

Fig. 10. Power cycling test for 650V/23A SiC MOSFET.

It can be obtained from Fig. 8 that the change of dV_{th}/dT_j is only 0.0003 V/°C during PC test, which is negligible. Therefore, dV_{SD}/dT_j and dV_{th}/dT_j can be measured in the calibration stage before the PC test and used for online monitoring and correction for threshold voltage in PC test. The flowchart is shown in Fig. 11.

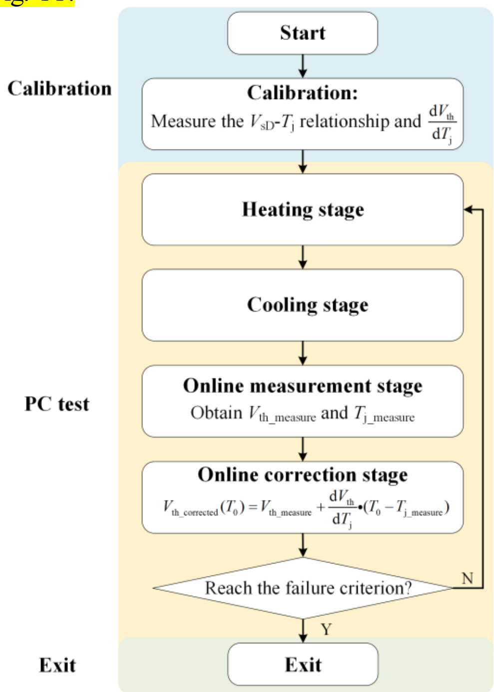


Fig. 11. Proposed flowchart of online monitoring and correction of threshold voltage in power cycling test

5. Conclusion

This paper presents a method for online monitoring and correction of threshold voltage in PC test. The temperature-sensitive characteristics of the threshold voltage and the influence of the junction temperature variation on the measurement results are considered in this paper. The corrected results are consistent with the offline calibration test results, which verifies the correctness of the method proposed in this paper.

Acknowledgements

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