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Comparative Analysis of Power Semiconductor Thermal Stress in DC and AC Power Cycling

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***Abstract*—Power semiconductors are gradually evolving towards lower cost, higher efficiency, higher power density, while they are considered to the most important component in the field of power electronics. Therefore, accelerated power cycling testing of power modules under different temperature stresses is required, where the accurate mapping of junction temperature becomes an important part. In this paper, theoretical analysis is carried out for both the DC and AC power cycling, in which the power dissipation and thermal stress of power semiconductor devices are in focused. Detailed derivation of the relationship between losses dissipation, junction temperature, and temperature swing are presented. At the same time, the differences, advantages and disadvantages of DC power cycling and AC power cycling are compared and analyzed. PLECS simulation is used to verify the correctness of the theoretical models.**

Keywords—power semiconductor, power cycling, junction temperature, PLECS

I. INTRODUCTION

The reliability and lifecycle of power semiconductors are an important indicator for evaluating power electronic systems [1]. In the field of renewable energy power generation, electric vehicle, aerospace application, their harsh working environment can be translated into the thermomechanical stress, which leads to wear-out, aging and degradation. However, various amplitudes of thermal cycling are difficult to be measured in field operation, so thermal models and Temperature Sensitive Electrical Parameters (TSEPs) are required to characterize and mapping the junction temperature values. Therefore, the power cycling tests are ideal to mimic the similar thermal stress of a power module even in an accelerated way.

According to the classification of typical accelerated power cycling, as introduced in [2], [3], accelerated reliability evaluation of power devices can be divided into two types of tests: thermal cycling (passive power cycling) and active power cycling [4]. In the case of thermal cycling, the temperature change of power device is due to the external temperature (e.g., oven or thermal chamber). For the active power cycling, the thermal performance of the power device is changed because of the power dissipation generated by the semiconductor itself.

There are two types of active power cycling depending on the difference in current stress of the power device. If the constant DC current flows through the device, the corresponding circuit is named as DC power cycling. If the pulse width modulation (PWM) based AC current is imposed in the device, the corresponding circuit is called AC power cycling. Currently, few literatures attempt to benchmark these two types of power cycling, this paper will present their operation principles and thermal stress of power device under test [5]-[10].

The structure of the paper is as follows. Section II introduces the operating principle of the DC power cycling circuit. Section III presents working principle of the AC power cycling circuit. In Section IV, both the loss and thermal models are introduced. The theoretical calculations are verified by the simulation results in Section V. Finally, some conclusions are drawn in Section VI between the two power cycling tests.

II. PRINCIPLE AND ANALYSIS OF DC POWER CYCLING CIRCUIT

This section will introduce its circuit design and operating on conditions of DC power cycling in detail. As shown in Fig. 1(a), positive pole of the DC current source is connected to the collector of T_1 and T_2 respectively, while the negative pole of the power supply is connected to the emitter of T_2 and device

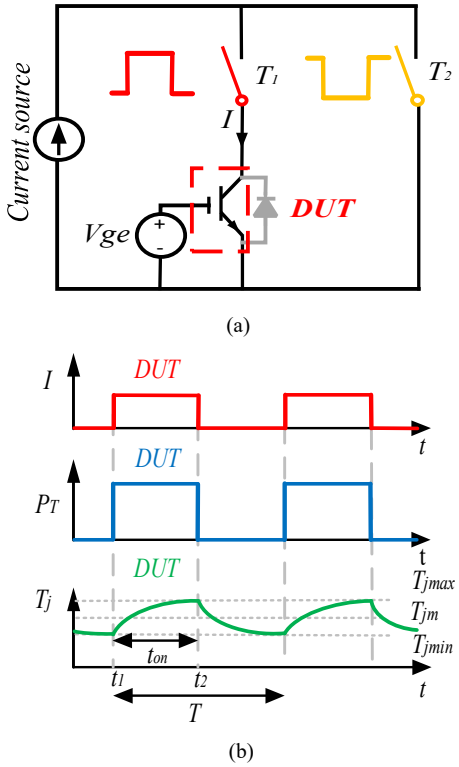


Fig. 1. Operation principle of DC power cycling. (a) DC power cycling circuit. (b) Load current, loss dissipation and junction temperature.

under test (DUT). Moreover, T_1 and DUT are connected in series. In the circuit, T_1 and T_2 apply complementary PWM pulses, while the DUT is permanently turned on.

In the case of normal operating condition, this circuit can produce the DC conduction loss for the IGBT. When T_1 is turned on, the DUT conducts a specific DC current, and the conduction loss occurs due to the on-state voltage drop. When T_1 is turned off, the current flows through T_2, and there is no current flowing through the DUT. This circuit can effectively prevent the risk of open circuit of the current source. The conduction loss P_T generated in the period is shown in Fig. 1(b), and its junction temperature T_j can increase and drop depending on "on" and "off" state of DUT.

It is noted that the DUT is driven by V_{ge}. During the period T, the load current I flows in during the period t_{on}, the minimum junction temperature is T_{jmin} at time t_1 , the maximum junction temperature T_{jmax} is reached at time t_2 and the average value is T_{jm}.

III. PRINCIPLE AND ANALYSIS OF AC POWER CYCLING CIRCUIT

The bridge topology with inductive load is common in power cycling test, some operating parameters such as power factor and modulation index can be adjusted. AC power cycling testing needs to consider cost-effectiveness, the load is generally a small inductor, to match the long-term consumption. A common AC power cycle topology is H-bridge circuit, whose test legs and load legs can be configured in multiple modes according to the mission profiles. This cycling test is usually preferred because it simulates the normal operating environment of the device as closely as possible.

The single-phase H-bridge circuit is shown in Fig. 2(a), which consists of a test leg and a load leg. The inductor, in the middle is used to eliminate PWM harmonics. The test leg provides a reference voltage, and the load leg provide a modulated voltage to simulate the loading characteristics seen from the test leg (e.g., resistance, inductance, or capacitance characteristics). Therefore, the current passing through the test leg can be adjusted flexibility. The driving signal of T_1-T_4 is shown in Fig. 2(a). The waveform of upper and lower switch is complementary.

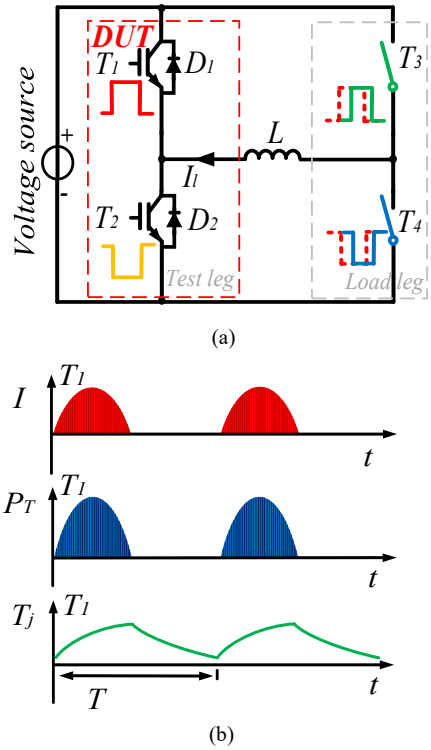


Fig. 2. Operation principle of AC power cycling. (a) AC power cycling circuit. (b) Loading current, power loss and junction temperature.

Under the stable operation, T_1 and D_2 are alternatively turned on within a switching period if the current is negative, while T_2 and D_1 conduct if the current is positive. Due to the symmetry of the half-bridge, the power consumption of the upper and lower switches is identical.

Due to the PWM modulation, the pulse current flows T_1 is indicated in Fig. 2(b). Apart from the conduction loss during the on-state of the power device, the switching loss needs to be considered as well due to the high switching frequency. Based on the loss dissipation P_T, the junction temperature T_j fluctuates since T_1 only conducts for a half of the fundamental period T.

IV. LOSS MODEL AND THERMAL MODEL

This section will describe the loss model, thermal model in detail for different concepts of power cycling. The power loss can be calculated by studying the current distribution of the IGBT in a fundamental cycle in the steady-state, and then the mean junction temperature and junction temperature fluctuations can be calculated according to the thermal impedance of the device.

A. Power loss dissipation

It is worth mentioning that for the DC power cycling, only the conduction loss is considered, due to the slow switching frequency of the device. For the AC power cycling, both the conduction loss and switching loss are considered.

For the DC power cycling, the calculation of the conduction power is relatively simple. The voltage drop between the collector and emitter terminals can be calculated by the following formula:

$$V_{CE}=V_{CE0}+r*I \tag{1}$$

where V_{CE0} denotes the collector-emitter initial voltage drop, r denotes the internal resistance between the collector and emitter terminals.

The conduction loss is equal to the collector-emitter initial voltage drop multiplied by the conduction current. The formula is as follows:

$$P_T=V_{CE}*I=V_{CE0}*I+r*I^2 \tag{2}$$

where P_T denotes the DC power loss, the current I denotes the DC source current value.

For the AC power cycling, the conduction loss of IGBT can be deduced as following:

$$P_T=\frac{1}{T}\int_0^{\frac{T}{2}} V_{CE}(t)i_1(t)d(t)dt \tag{3}$$

where T denotes the fundamental period, V_{CE} denotes the on-state voltage of the IGBT, i_l denotes the load current, and d represents the duty cycle.

If the angle between the voltage and the load current is φ, and the linear approximation of the IGBT forward characteristics, is assumed the conduction loss can be further simplified as:

$$P_T=\frac{1}{2}\left(\frac{1}{\pi}V_{CE0}I_m+\frac{1}{\pi}V_{CE0}I_m^2\right)+Mcos\varphi\left(\frac{1}{8}V_{CE0}I_m+\frac{1}{3\pi}V_{CE0}I_m^2\right) \tag{4}$$

where M is the modulation index, I_m denotes the peak value of load current.

In several literatures, the polynomial fitting method is used to represent the turn-on energies E_{onT} and turn-off energies E_{offT} of the IGBT. As a result, the switching energy of the IGBT E_{swT} can be deduced as:

$$E_{swT}=E_{onT}+E_{offT}=(a_T+b_T*I_m+c_T*I_m^2) \tag{5}$$

where a_T, b_T, c_T denote the corresponding coefficient of the fitting function respectively.

According to the relationship between energy and power dissipation, the switching loss P_{swT} in a fundamental period can be calculated as following:

$$P_{swT}=f_{sw}\frac{V_{dc}}{V_{dc}^*}\left(\frac{a_T}{2}+\frac{b_T}{\pi}I_m+\frac{c_T}{4}I_m^2\right) \tag{6}$$

where f_{sw} denotes switching frequency and V_{dc} denotes the test dc-link voltage, V^*_{dc} denotes the reference dc-link voltage. It is worth noting that when the switching frequency is low, the conduction loss accounts for a large proportion of the total loss, and when the switching frequency is high, the switching loss accounts for a large proportion.

B. Junction temperature estimation

Thermal stress is closely related to the material of the power device itself and the cooling methods. IGBT power modules are constructed of multiple layers of materials with different thermal resistances and thermal capacitances. As shown in Fig. 3, T_j stands for junction temperature (chip surface temperature), T_c indicates the case temperature, and T_a means ambient temperature.

According to the relationship between junction temperature and power loss, the relationship between mean junction temperature T_{jm_T} and junction temperature swing ΔT_{j_T} can be obtained as follows:

$$T_{jm\_T}=P_T\left(\sum_{i=1}^{4}R_{thJC\_T}(i)+R_{thCH\_T}\right)+n(P_T+P_D)*R_{thHA}+T_a \tag{7}$$

where P_T represents the total power dissipation, including conduction loss P_T and switching loss P_{swT}. i represents the number of thermal resistance stacks. R_{thJC}, R_{thCH} denote the junction-to-case and case-to-heatsink thermal resistance. R_{thHA} denotes the thermal resistance between the heatsink and ambient. n denotes the number of IGBT or diode in the module. P_D denote the total power dissipation of the diode.

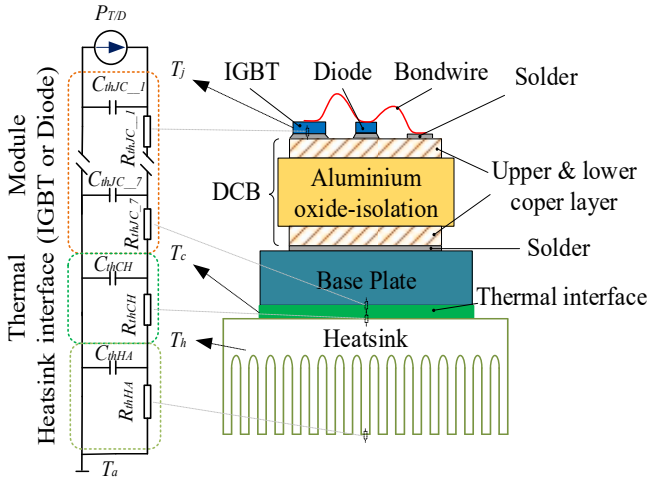


Fig. 3. Thermal impedance model of power module.

$$\Delta T_{j\_T}=2P_T*\sum_{i=1}^{4}R_{thJC\_T}(i)*\frac{\left(1-e^{\frac{-t_{on}}{\tau_{thJC\_T_i}}}\right)^2}{1-e^{\frac{-T}{\tau_{thJC\_T_i}}}}t \tag{8}$$

where, t_{on} denotes a half of fundamental period and T is the fundamental period of current. τ denotes the thermal time constant of each Cauer layer. In general, in order to facilitate calculation, the junction-to-case RC network in the above physical material model will be converted into fourth-order Foster model under the same thermal effect conditions.

V. SIMULATION COMPARATIVE ANALYSIS

The simulated loss dissipation and thermal cycling of the power device will be presented and compared with mathematical calculation from the loss and thermal models in this section. The parameters of DC power cycling and AC power cycling are summarized in Table I and Table II, respectively.

TABLE I. PARAMETERS AND CONDITIONS OF DC POWER CYCLING

Specification	Value
Rated DC current	50 A
Rated switching frequency	10 Hz
Ambient temperature	20 °C

TABLE II. PARAMETERS AND CONDITIONS OF AC POWER CYCLING

Specification	Value
DC voltage	400 V
Filter inductor	3 mH
Fundamental frequency	10 Hz
Switching frequency	10 kHz
Power factor	-1
Peak current	50 A
Ambient temperature	20 °C

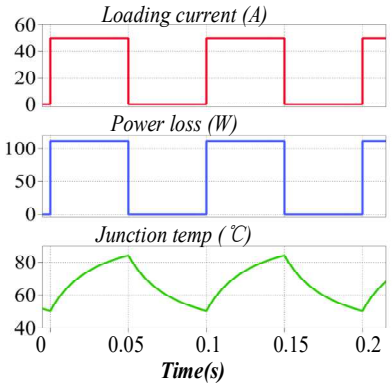


Fig. 4. DC power cycling PLECS simulation result.

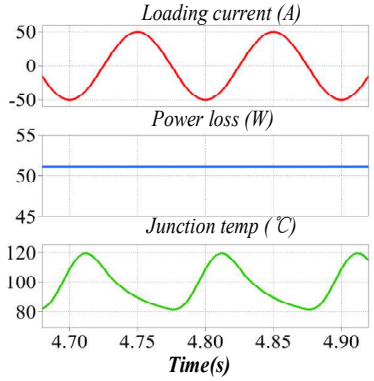
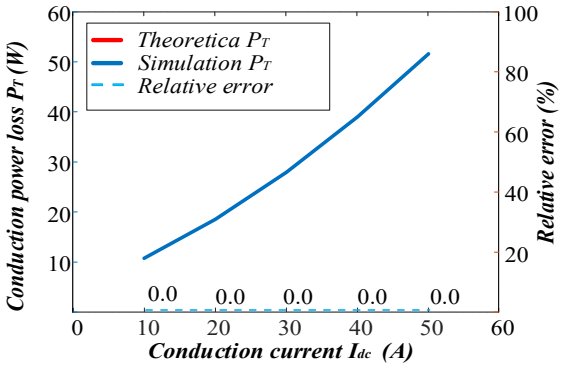


Fig. 6. AC power cycling PLECS simulation result.



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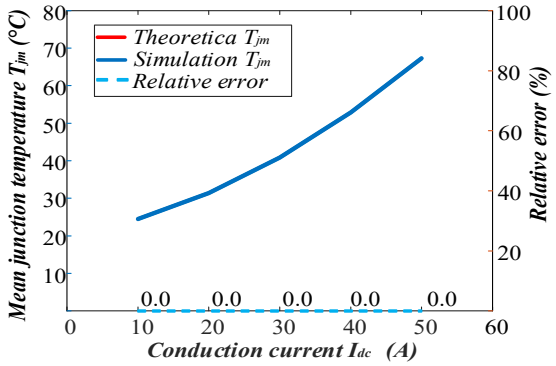

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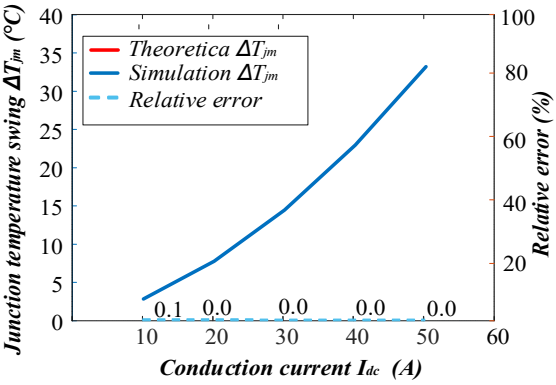
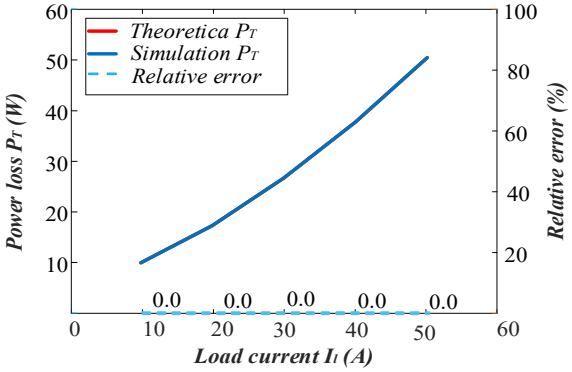


(c)

Fig. 5. Comparison between calculation and simulations with DC 50 A current. (a) Power loss. (b) Mean junction temperature. (c) junction temperature swing.



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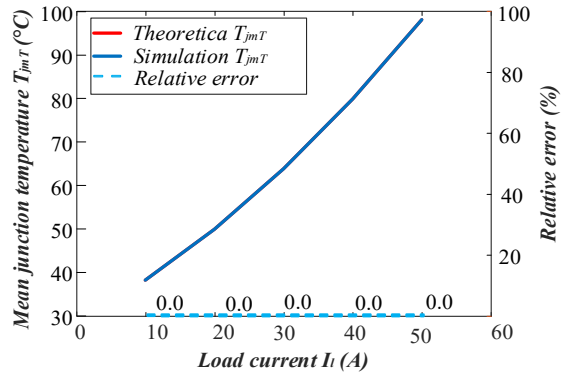

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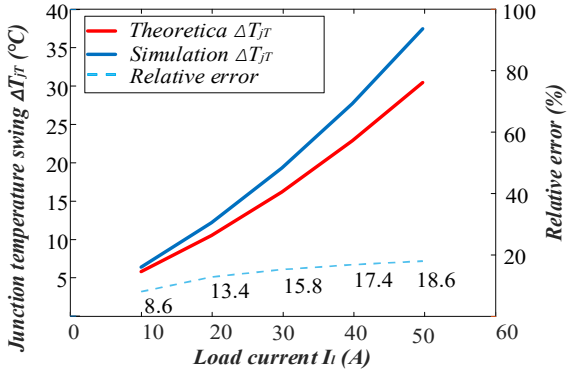


(c)

Fig. 7. Comparison between calculation and simulations with AC 50 A current, f_{sw}=10 kHz. (b) Power loss. (c) Mean junction temperature. (d) junction temperature swing.

A case study is selected by using FP50R12KT4G IGBT power module with the maximum continuous current 50 A, where the maximum switching state junction temperature of 150 ℃ [11]. The simulation model is established by using PLECS. In DC power cycling, as shown in Fig. 4,where only conduction losses are concerned, the DC current that flowing through the DUT and the switching frequency are key parameters. Under the condition of 10 Hz switching frequency and 50 A loading current, by substituting the above parameters into the loss model and thermal model, it can be calculated, the power loss, the peak value is 111.3 W, and the average value is about 55.7 W. Moreover, regarding the junction temperature curve, with the maximum value of 84.1 °C, and the minimum value about 50.5 °C, the average junction temperature is about 67.3 °C, and junction temperature swing is 33.6 ℃.

The DC comparison between the theoretical calculation and the simulation is summarized in Fig. 5(a)-(c). In the cases of the different loading current, the relative error between these two approaches is almost zero, which proves the correctness of the theoretical model.

In the case of AC power cycling, the circuit operates in inverter mode, which indicates the power factor is equal to –1. Under the condition of 50 A testing current. Compared with the DC power cycling, the AC power cycling increases junction temperature, and junction temperature fluctuation the switch on-off process, thereby increasing the switching power loss. Power loss and junction temperature variation also can be obtained by changing the switching frequency during the AC cycle.

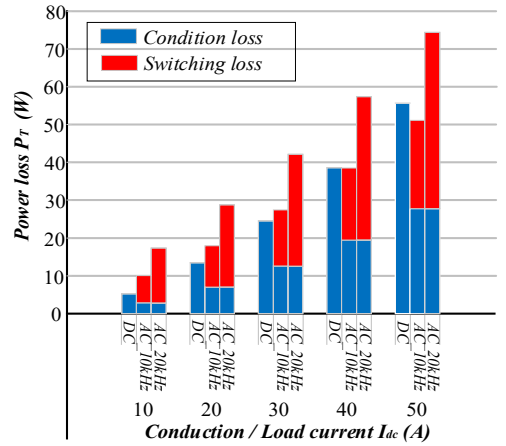
According to the parameters in Table II and the above mathematical models, the total power loss P_T is 51.1 W, the mean junction temperature T_{jmT} reaches 97.5 °C, and junction swing of DUT is 37.8 °C. The PLECS simulation result of AC power cycling is shown in Fig. 6, the red sine curve is the load current with a peak current of 50 A. The middle curve is the total power loss in one sine cycle, the value is 51.1 W. At the same time, the maximum value of the junction temperature is about 119.6 °C, the minimum value is 81.8 °C, and the average junction temperature is 97.5 °C.

As shown in Fig. 7(a)-(c), the simulation results of power loss and average junction temperature are highly consistent with the theoretical models. However, due to the difference in the calculation of the transient thermal resistance, a certain error occurs in the junction temperature fluctuation, the main reason for this error is the difference between the theoretical and simulated junction temperature fluctuation acquisition methods.

In order to facilitate the comparative analysis within the AC power cycling, the theoretical calculation is investigated with the increased switching frequency. When f_{sw} is 20 kHz, the power loss increases to 74.4 W, the mean junction temperature reaches to 135.4 °C, and the junction swing is 53.8 °C. It is obvious that the three values mentioned above increase due to the higher switching frequency.

The calculation of the power loss and thermal stress with DC and AC power cycling is summarized in Fig. 8, where the switching frequency of 10 kHz and 20 kHz are considered in the AC power cycling.

As shown in Fig. 8(a), under the same loading conditions, the conduction losses of the two AC powers are the same, while the switching loss becomes twice with the switching frequency of 20 kHz. Compared with DC and AC power cycling, the conduction loss of the DC power cycling increases more significantly with the higher loading current.



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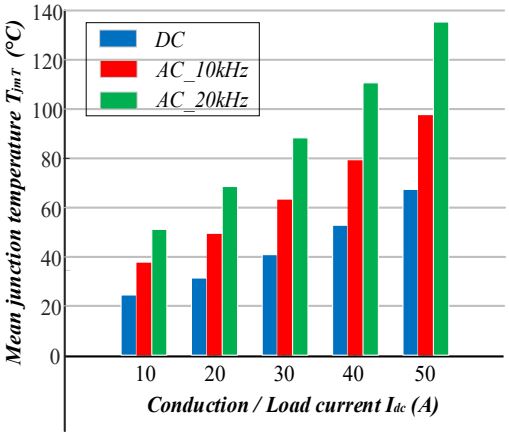

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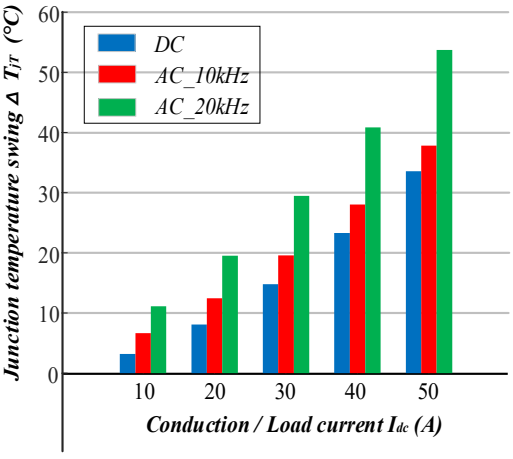

(c)

Fig. 8. DC, AC 10 kHz, AC 20 kHz, comparison. (a)Mean power loss. (b) Mean junction temperature. (c) Junction temperature swing.

As shown in Fig. 8(b), the junction temperature of the AC power cycling is higher due to the presence of switching losses. When the switching frequency increases, the greater total power loss leads to the higher junction temperature.

As shown in Fig. 8(c), among the three cycling comparisons, the DC power cycling junction temperature fluctuation is the smallest, and the fluctuation becomes the highest when the switching frequency is 20 kHz.

VI. CONCLUSION

By comparing the DC power cycling and the AC power cycling methods, the principle of the DC power cycling is relatively simple, but it cannot match the actual working conditions of the device. The AC power cycling method can simulate the actual operating state of the IGBT in the converter, making the results closer to reality. However, the operation is more complicated. The theoretical power loss model and thermal model can predict the thermal stress of the power device. PLECS simulation has been carried out, and it is evident that it is consistent with the theoretical models. In the case of the AC power cycling under the same conditions, the higher switching frequency results in the greater power loss, the higher junction temperature, and its fluctuation. Nevertheless, the junction temperature fluctuation model for AC power cycling still has space for further improvement, which is the place for subsequent improvement. At the same time, the DC and AC power cycling experiments will be carried out to verify the correctness of the above models in the next works.

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