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Article

Evaluation of the Thermal Resistance in GaN HEMTs Using Thermo-Sensitive Electrical Parameters

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Abstract: The thermal management of power converters is not only crucial for their own optimal operation and reliability, but also for the overall system in which they are operating. Reliability is a very serious aspect because power electronics systems are being increasingly widely adopted in mission-critical applications in the e-mobility sector, in smart grids, and other applications where safety and operational continuity are essential. The current trend towards miniaturization of power conversion systems and, consequently, towards high power density solutions is speeding up the diffusion of Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT). GaN HEMT-based high power density converters must be properly managed, making the estimation of the thermal characteristics of these devices essential. This paper proposes the use of some Thermo-Sensitive Electrical Parameters (TSEP) for a simple and effective thermal resistance evaluation. The primary advantages and limitations of these TSEPs have been critically analyzed. The analysis highlighted that the use of the gate-source voltage is the best approach. However, it requires direct access to the gate pin, which may not be available externally in some system-in-package solutions.

Keywords: power electronics; thermal resistance; GaN HEMTs



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1. Introduction

The miniaturization of device packages, together with the creation of components capable of working at ever higher frequencies and dissipating greater power, has led to an increase in heat flow in systems [1]. One of the biggest difficulties has always been removing the heat generated by the device to meet its thermal requirements while ensuring optimal performance [2]. Thermal management is one of the strategic areas of research and development for electronics manufacturers worldwide [3]. Sophisticated heat sink designs have been developed, new materials for heat transfer have been discovered, and complex cooling systems have been designed [4,5] in order to keep the junction temperature of the semiconductor device below the maximum permissible limit.

When an electronic device is subject to heating/cooling cycles, the mechanical stress associated with the thermal expansion of its different materials may cause the detachment of silicon from the metal case or even micro-cracks in the semiconductor [6]. These thermal stresses can cause a reduction in the device's usable lifetime and reliability issues [7]. In this respect, the estimation of the device's peak temperature for a current through the device would enable the evaluation of the thermal resistance, R_{th} [8].

The estimation of the thermal resistance is fundamental when designing the device packaging [9]. To this end, a thermal simulation is required for efficient thermal management as it enables the evaluation of the effect of different dissipating elements, and their placement, on the chip. In [10], mechanical-thermal co-design has been used for the optimization of the electronic package module. A method for thermal characterization

of GaN-based transistors using coupled simulation has been proposed in [11]. CAD technology has been used for modelling the power distribution profiles while finite element analysis has been adopted for simulating the global thermal behavior; the results were combined to improve the model accuracy. 3-D thermal simulations have been used in [12], in order to evaluate the variation of the thermal resistance of GaN High Electron Mobility Transistors (HEMTs) at varying gate geometries. The information is useful when producing suitable circuit models at the design stage. Similarly, ref. [13] has proposed a methodology for extracting the thermal equivalent circuit of a high-density GaN-based power stage using a synchronous buck converter as the test vehicle.

The relation between the breakdown of advanced GaN structures and thermal resistance has been investigated in [14]. Transient thermometry techniques have been used for localizing heating sources using nanoscale thermal transport analysis [8]. A transient electrical characterization method used to determine the temperature in a transient self-heating state of GaN HEMTs has been proposed in [15], which also experimentally identified the heat source. Despite the aforesaid efforts and innovative solutions, thermal characterization of GaN HEMT devices is still in its early stage [16–18].

This paper analyzes the primary benefits and limitations of using temperature-sensitive electrical parameters (TSEPs) for thermal resistance characterization. TSEPs use passive probes to measure electrical quantities at the device terminals without direct access, and these quantities are adopted to estimate the junction temperature, T_j [19]. This approach has limited intrusiveness at the device level [20], making the use of TSEPs an interesting approach [21]. In particular, the on-state drain-source voltage, gate-source voltage, and gate current have been experimentally analyzed as they are measurable quantities, considering the device characteristics.

The remainder of this paper is organized as follows. Section 2 shows some solutions for the estimation of the junction temperature and the characterization of the thermal resistance. A description of the TSEP calibration procedures and some results are reported in Section 3, where the main advantages, limits, and best application fields of the different TSEP are reported. Finally, the conclusions are presented in Section 4.

2. Estimation of the Junction Temperature and Thermal Resistance Characterization

This section first describes the main techniques adopted for junction temperature estimation, primarily focusing on TSEPs. Then, the adoption of TSEPs for evaluating the thermal resistance of GaN HEMTs is analyzed.

Optical methods exploit the dependence between temperature and photoemission [22]. In this field, the use of an integrated photodiode or infrared camera enables contactless temperature monitoring [23]. The use of special paints to print the surface increases the accuracy but also increases the costs [24]. The adoption of optical fibre enables high resolution and fast response time, but it is an expensive solution.

Physical methods execute T_j measurement by contacting thermo-sensitive materials with the device surface [25]. Various pieces of equipment have been used for the measurement: thermocouples, thermistors, scanning thermal probes, multiple contact or blanket coatings, etc. The time response of the probe is the primary limitation when tracking thermal variations. The need for contact is another limit that makes it useless in high-voltage applications.

Electrical methods use some proprieties of the semiconductors that depend on the temperature [26]. Thermal test chips, e.g., resistance temperature detector or diode, are fabricated on the device surface. In the first case, the temperature sensor is a thermistor whose voltage drop changes as its resistance changes due to a temperature variation. In the second case, the modification of the forward voltage is adopted for detecting a temperature variation. The significant cost and layout modification complexity are their primary drawbacks. For this reason, the TSEP are the most used electrical methods thanks to their ability at indirectly inferring the temperature by measuring the current flowing through the device or the voltage drop across it. In this case, the electrical quantities

are measured at the device terminals employing simple op-amp-based electronic circuits, thereby avoiding intrusive direct access. The quantities used for T_j estimation are: on-state voltage [27]; threshold voltage [28]; saturation current [29]; Miller plateau [30]; switching time delay [31]; peak gate current [32,33]; and current and voltage switching speed [34].

Generally, TSEPs are widely used for device condition monitoring [35] because they combine good accuracy with a strong ability in tracking fast temperature transients [36]; however, the granularity in the case of multi-die is limited. In the last few years, some studies have adopted TSEPs to determine the thermal resistance of GaN HEMTs.

In [37], the use of the forward voltage (i.e., a TSEP) of an AlGaIn/GaN Schottky junction has been able to obtain good linearity and the results have shown good accuracy. However, this approach cannot be used online, i.e., the measurements cannot be performed during the normal functioning of the device but only after it is shut down. Consequently, the channel temperature reduces in the interval between when the device is turned off and the acquisition of the TSEP is performed: the longer the delay time, the lower the tested temperature. Moreover, this method is complex.

The conduction resistance and the forward voltage drop between the gate and source are TSEPs that have been proposed to test the thermal characteristics of the GaN HEMTs [38]. However, few details have been provided on the evaluation of thermal resistance using these quantities. Furthermore, sensing the conduction resistance is problematic because the overall conduction resistance is the sum of the junction resistances and the bond wires and solder joints [39]. An interesting approach based on using the gate current or the drain-source voltage as a TSEP is reported in [21]. The current sensing is indirectly obtained through a resistor, which is also used to avoid electric stresses during the turn-on. The results are accurate and reproducible, but the access to the measurement is complex.

3. Considered TSEP for Thermal Resistance Characterization in GaN HEMTs

The temperature characterization has been performed using the following TSEPs:

- V_{ds} (on-state drain-source voltage)
- V_{gs} (gate-source voltage)
- I_g (gate current)

They have been selected because of their good features, including linearity, calibration process simplicity, accuracy, and the possibility of online temperature measurements.

Linearity is an interesting indicator for data processing. It is also important for the calibration step because a linear TSEP does not need a lot of measurement points. The calibration of a TSEP is an important step in the temperature assessment of the device. In particular, the relationship between the TSEP and device temperature is determined by a calibration procedure that consists of a measurement of the TSEP at different values of temperature [19]. Every TSEP requires a calibration step, and the calibration time depends on the TSEP. For GaN devices, the calibration curve can significantly change from one GaN HEMTs device to another in the same product family, but it does not influence the final calculation of R_{th} .

First, an estimation of the thermal impedance, Z_{th} , is performed considering the T_j evaluation at 120 s. Then, the steady-state T_j is estimated in order to perform the R_{th} calculation. Finally, a simple relation between them, that enables the smaller Z_{th} estimation time to benefit, is reported. For each TSEP and testing current, 10 measurements have been performed and the average value of Z_{th} and R_{th} have been evaluated; the difference between the average value and the extrema (minimum and maximum) has also been noted.

For all three TSEPs (V_{ds} , V_{gs} , and I_g), the equipment used for the calibration and measurement is shown in Figures 1 and 2. The calibration process has been carried out using the following tools:

The equipment includes:

- a thermostream, to force the device under test (DUT) at different temperatures;
- a source meter 2450;
- a thermocouple to monitor the temperature.

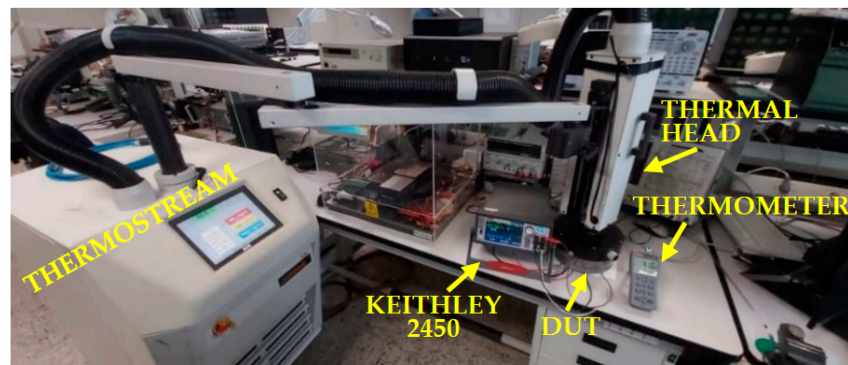


Figure 1. Calibration setup.

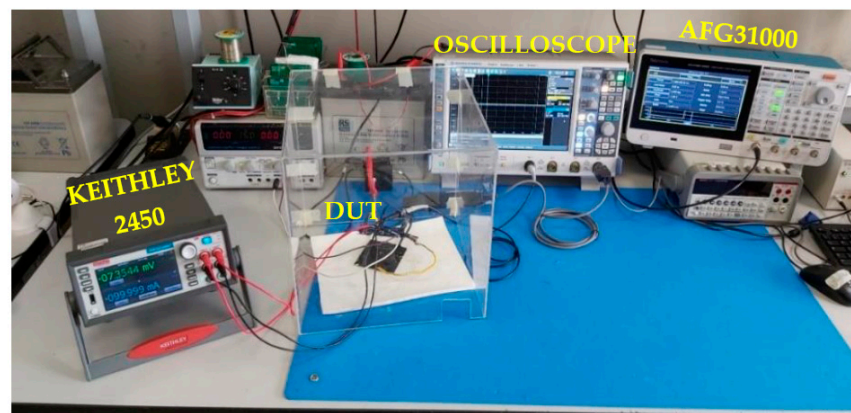


Figure 2. Measurement setup.

To perform the R_{th} measure, a test bench has been equipped with a Digital Oscilloscope RTO 2014 to view the waveforms of TSEPs used (V_{ds} , V_{gs} , and I_g). The GPS-3303 Power Supply is exploited to supply the gate of the DUT, while 6060B is used as an active load, which is driven by an AFG31000 Arbitrary Function Generator. A Source Meter 2450, set in the 4-wire mode, is used to force a current and simultaneously read the variations of the TSEPs (V_{ds} , V_{gs} , and I_g), and a thermocouple is used to monitor the temperature.

It is worth noting that the Z_{th} and R_{th} evaluation (e.g., Equation (3)) requires the concurrent knowledge of the junction temperature increment (ΔT_j) and the incoming power that has caused it. However, there is no accurate and simple way to concurrently measure these quantities while the GaN HEMT is working. An indirect measurement of T_j is necessary and the TSEPs are adopted to fulfil this purpose. From this perspective, it is necessary to know the value of the TSEP at different T_j (for example see the calibration curves in Section 3.1)

The calibration process aims to obtain this information to find a mathematical relationship between the TSEP and T_j (e.g., Equation (1)). At this stage, it is necessary to determine the junction temperature for each measured value of the TSEP. Therefore, the ambient temperature is set at different values using the thermostream heater and a small test current is applied to perform the TSEP measurement. The junction temperature is assumed to be equal to the ambient temperature at this stage. This condition is true if the self-heating due to the test current is negligible.

During the Z_{th} or R_{th} evaluation, the initial T_j is equal to the room temperature; it is increased by a large pulsed current (i.e., it causes self-heating expressly to increase T_j). The power generated into the device is estimated from the known heating current and the measured drain-source voltage. At this stage, the information acquired during the calibration process is used to estimate T_j from the TSEP measurement. In detail, the

mathematical relation (e.g., Equation (1)) is rearranged to evaluate T_j according to the TSEP (e.g., Equation (2)).

Finally, it is worth noting that the value of these TSEPs changes over time; consequently a TSEP measure at an early stage and after a significant amount of time provides different values under the same T_j . Therefore, the calibration performed at an early stage to evaluate the R_{th} cannot be used accurately after an extended time. In this case, it is necessary to repeat the calibration process to account for the effect of device degradation on the TSEPs.

The Z_{th} and R_{th} measurements have been performed on a GaN power transistor device soldered on a 2-layer application board with the following characteristics:

- $R_{DS(on)} = 80 \text{ m}\Omega$
- $V_{ds} = 650 \text{ V}$
- $I_{ds} = 15 \text{ A}$
- Package: PowerFLAT $5 \times 6 \text{ HV}$

3.1. On-State Drain-Source Voltage TSEP

The first TSEP used is on-state drain-source voltage, V_{ds} . The relationship between the TSEP and the temperature has been first determined by employing a calibration process. The setup used to perform this initial step is shown in Figure 3.

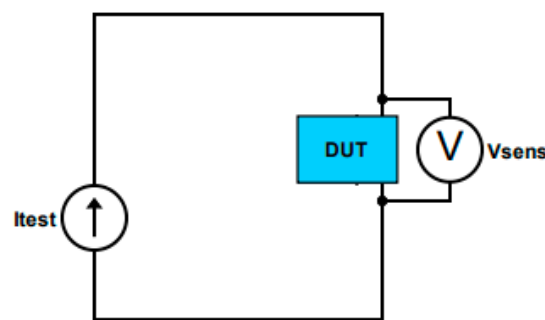


Figure 3. Calibration electrical circuit for sensing the drain-source voltage, V_{ds} .

During the calibration, the source meter 2450, set in the 4-wire mode, forces a 100 mA current while simultaneously measuring the variations of the V_{ds} . A very important aspect to emphasize is that, for the calibration to be carried out correctly, it is necessary to apply a current that avoids the DUT self-heating. In addition, the calibration has been performed starting at the ambient temperature and then increased to $80 \text{ }^\circ\text{C}$.

The device has been placed in a glass chamber (Figure 4) so that the airflow from the thermostream heats the DUT. The calibration curves of the V_{ds} vs. the temperature carried out using four sensing currents are shown in Figure 5.

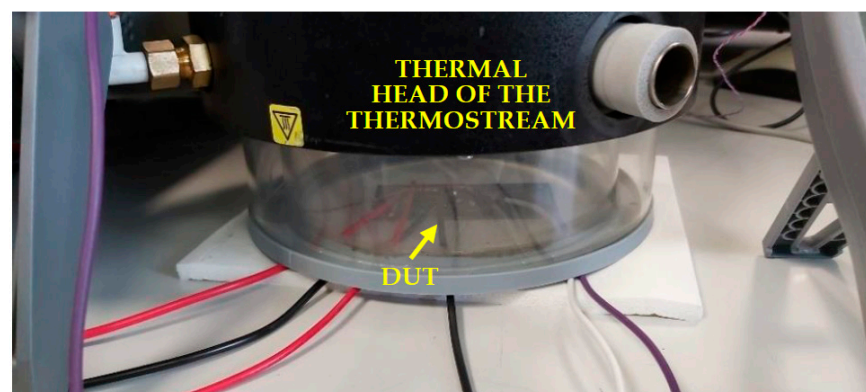


Figure 4. The device under the airflow.

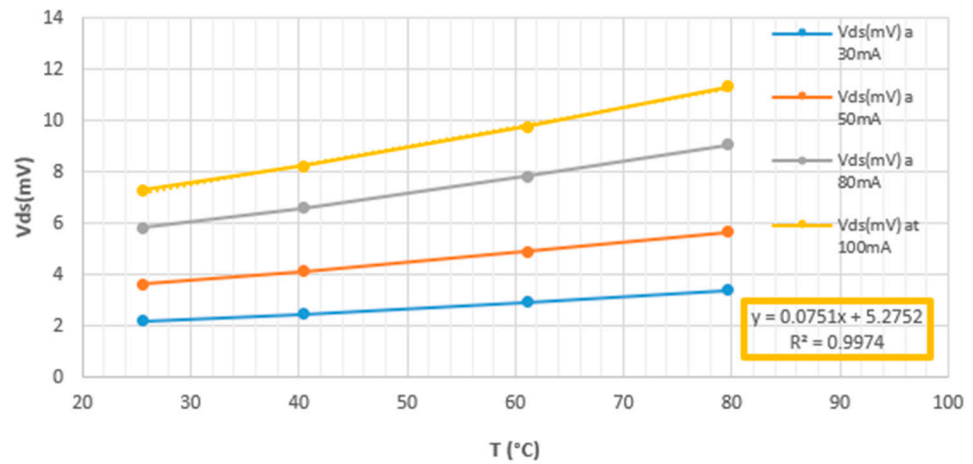


Figure 5. Calibration curves of V_{ds} .

As expected, the value of the V_{ds} increases as the temperature increases. During the calibration phases, four different current values were used: 30 mA, 50 mA, 80 mA, and 100 mA. In addition, Figure 5 shows that the trend of the V_{ds} with the temperature was almost linear and the factor R^2 was about 0.9974 for any current.

Considering the curve at 100 mA, which is the best compromise between accuracy and avoiding self-heating, the following expression is obtained:

$$V_{ds} = 75.1 \cdot 10^{-6} T + 5.2752 \cdot 10^{-3} \tag{1}$$

In this equation, the ambient temperature (set by the thermostream) and the junction temperature coincide because a test current that avoids the self-heating has been used. Therefore, a simple relation between T_j and the drain-source voltage can be derived from Equation (1):

$$T_j = 13300 V_{ds} - 70200 \tag{2}$$

To carry out the thermal characterization of the device, the test conditions reported in Table 1 and the setup reported in Figures 6 and 7 have been used. Equation (2) is valid when T_j is in the calibration range. The current values refer to I_{ds} .

Table 1. Test conditions for V_{ds} measurements.

Parameters	Value
Heating current	2.5 A, 3 A, 3.6 A
Test current	100 mA
Heating time	120 s

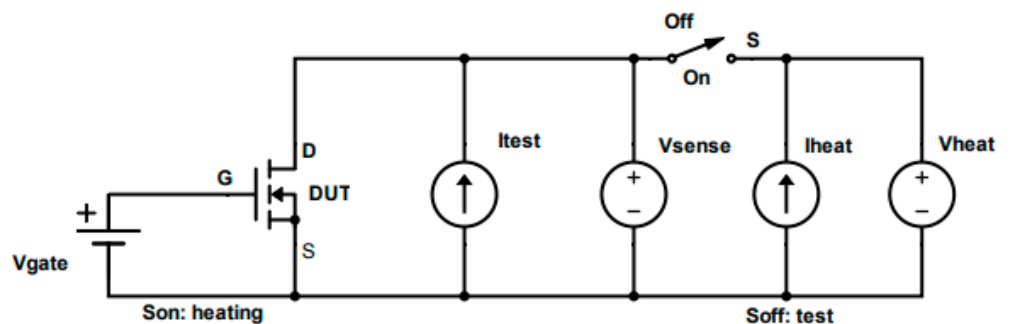


Figure 6. Schematic of the electrical circuit for V_{ds} measurement.

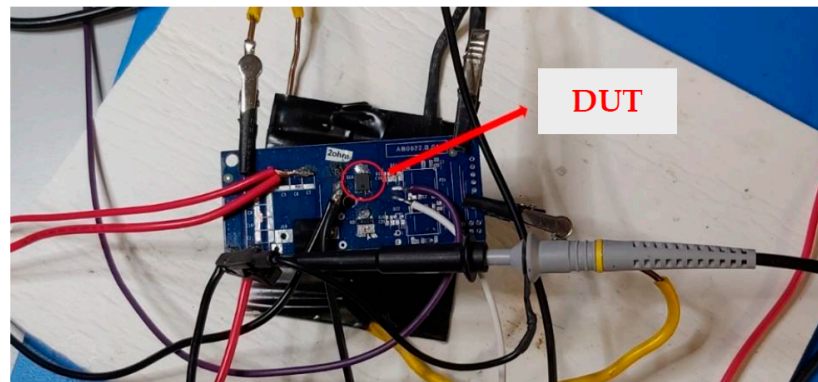


Figure 7. V_{ds} measurement setup.

During the measurement, three different heating currents were used (2.5 A, 3 A, and 3.6 A). For each of them, 10 measurements were performed to ascertain the robustness of the method. Some of these measurements are reported in Figure 8 where, during the interval labelled “1”, the device was at room temperature with no heating current, so the value of V_{ds} was measured for a current equal to 100 mA.

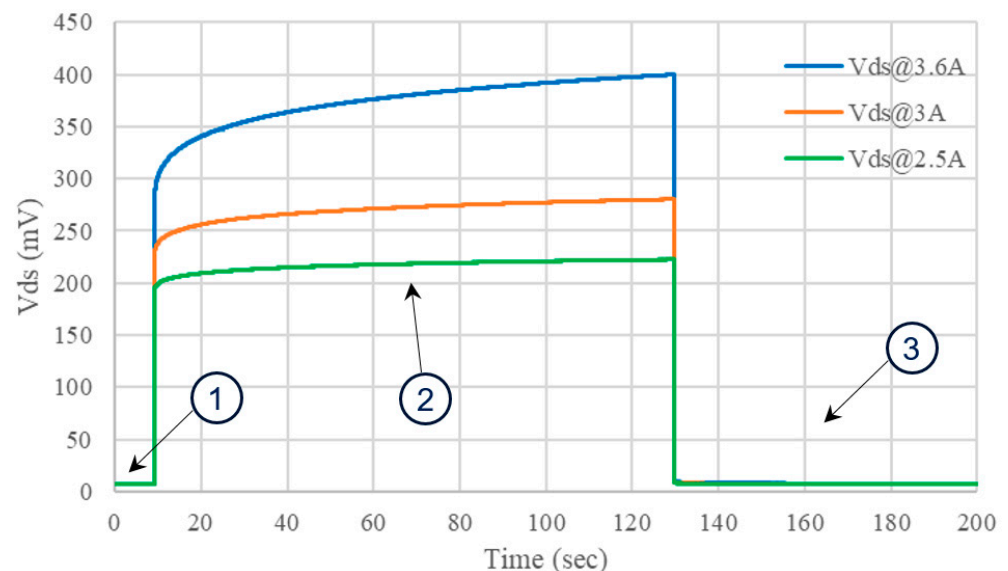


Figure 8. Trend of V_{ds} .

Once the heating current pulse is applied (“2”), V_{ds} instantaneously increased significantly due to the large current. Then, the device began to heat up and, consequently, V_{ds} increased further. When the pulse vanished (“3”), the heating current no longer flowed into the device and only the sensing current flow remained. Consequently, the cooling phase began, and, in the end, V_{ds} returned to the initial value. The cooling curves of the V_{ds} have been reported in Figure 9. As mentioned before, during the interval “1”, V_{ds} is measured using Equation (2) to indirectly measure the initial T_j ($T_{j,0}$). Similarly, at the beginning (after 100 μ s) of interval “3”, V_{ds} is measured again to indirectly estimate the new T_j ($T_{j,end}$).

Indicating with:

$V_{ds,avg,2}$ the average value of V_{ds} during the interval “2”;

T_{j0} the temperature before the application of the heating current, $I_{heating}$, i.e., at $t = 0$ s;

$T_{j,end}$ the value of the temperature when $I_{heating}$ is removed and only the sensing current flows into the DUT;

then, the thermal impedance (i.e., at $T_{j,end}@120s$) or the thermal resistance (i.e., at $T_{j,end}@1000s$) can be computed as follows:

$$R_{th} = \frac{\Delta T_j}{P} \quad (3)$$

where $\Delta T_j = T_{j_{end}} - T_{j_0}$, $P = I_{heating} V_{ds,avg,2}$.

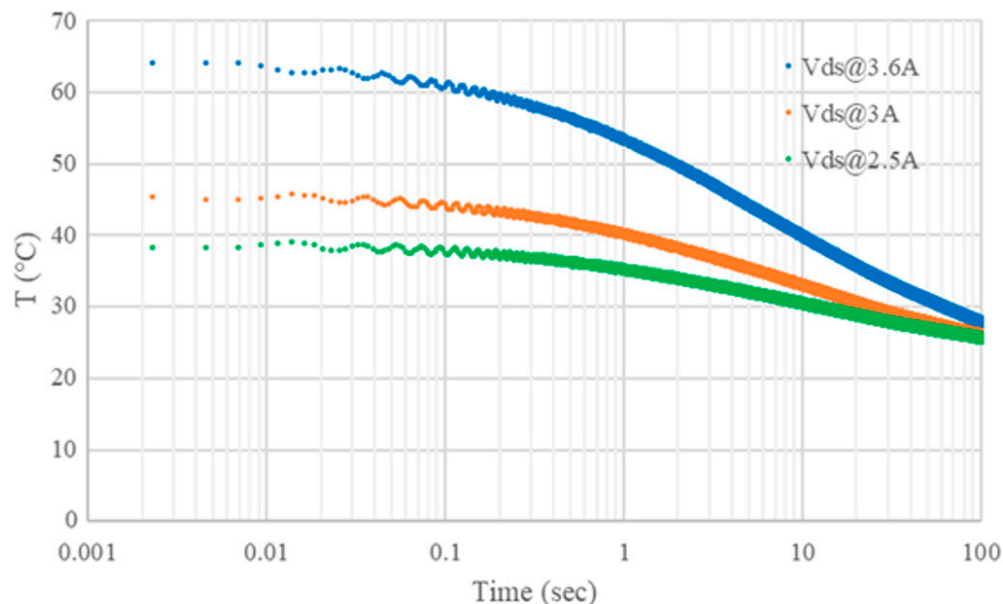


Figure 9. Cooling curves of V_{ds} .

Equation (3) is valid when T_j is in the calibration range. The Z_{th} calculation can be performed using Equation (3) when T_j is in the calibration range. The difference with the R_{th} calculation is the choice of $T_{j_{end}}$; it is equal to the steady-state temperature for R_{th} evaluation, but it is lower for Z_{th} evaluation. During the calibration process, and at the beginning of the Z_{th} or R_{th} evaluation (T_{j_0}), the junction temperature is equal to the ambient temperature. After that, they differ once the pulsed current is adopted ($T_{j_{end}}$). Table 2 reports the average value of Z_{th} evaluated according to Equation (3) by considering the three heating currents. For each current, the difference between the average value of Z_{th} and the minimum and maximum values obtained during the ten tests is lower than 2%.

Table 2. Values of Z_{th} evaluated using V_{ds} as TSEP.

Heating Current		
2.5 A	3 A	3.6 A
29.0 °C/W	28.8 °C/W	28.4 °C/W

Linearity is an advantage of this approach., In contrast to the approaches based on the other two TSEPs, it does not need an accessible gate pin.

The challenge is the detection of small voltage variations. The sensing current must be increased to increase the voltage variations, thus facilitating appreciation of the voltage variations. On the other hand, the self-heating could become not negligible if the sensing current is too high. In this work, a current value of 100 mA is the best compromise to limit the self-heating current while maintaining a good accuracy in V_{ds} voltage measurement.

The use of V_{ds} as a TSEP for R_{th} estimation should be avoided when the device presents a conduction resistance value below 10 m Ω . In fact, it is difficult to understanding if a small V_{ds} variation (μ V) is due to the variation of the conduction resistance or to the variation of the parasitic resistance of metallic contacts (leads, bonding wires, and so on). As such, thermal resistance characterization using V_{ds} is preferable when the parasitic resistances are negligible.

3.2. Gate-Source Voltage TSEP

In this case, the first step was calibration to determine the relationship between V_{gs} and temperature. The setup used to perform this initial step is shown in Figure 10.

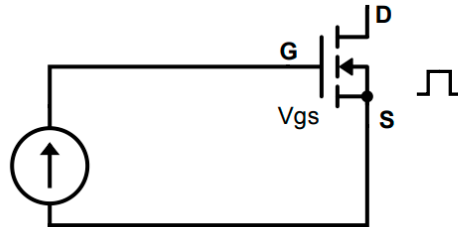


Figure 10. Calibration electrical circuit for V_{gs} .

The calibration was performed by measuring the V_{gs} at a sensing current of 45 μA forced by the source meter. The value of the current was appropriately chosen to ensure that, during the calibration step, the V_{gs} was in a range that enabled the device to turn on. The calibration curve of V_{gs} vs. temperature is reported in Figure 11.

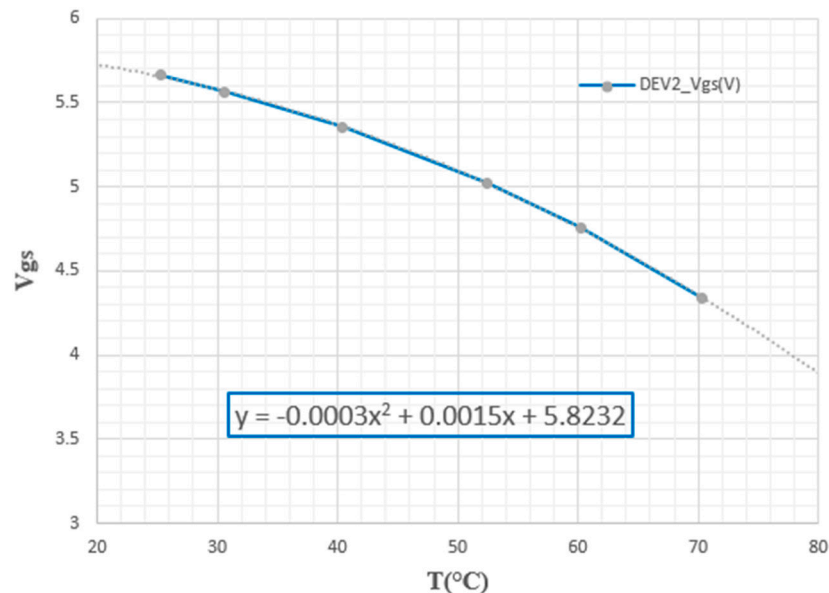


Figure 11. Calibration curve of V_{gs} .

The gate-source voltage can be expressed as a function of the imposed temperatures once the calibration process has been performed:

$$V_{gs} = -0.0003T^2 + 0.0015T + 5.8232 \quad (4)$$

In order to carry out the thermal characterization of the device, the test conditions reported in Table 3 were considered, and the setup is indicated in Figure 12. The heating current values refer to I_{ds} while the sensing current refers to I_g .

Table 3. Test conditions of V_{gs} .

Parameters	Value
Heating current	2.5 A, 3 A, 3.6 A
Test current	45 μA
Heating time	120 s

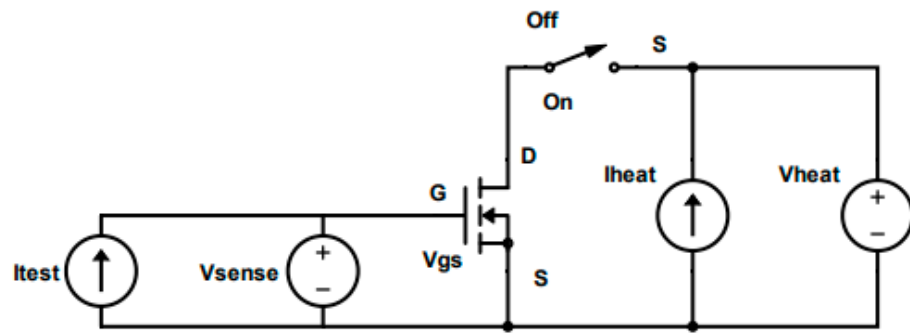


Figure 12. Schematic of the electrical circuit for V_{gs} measurements.

The results of the measurement are shown in Figure 13.

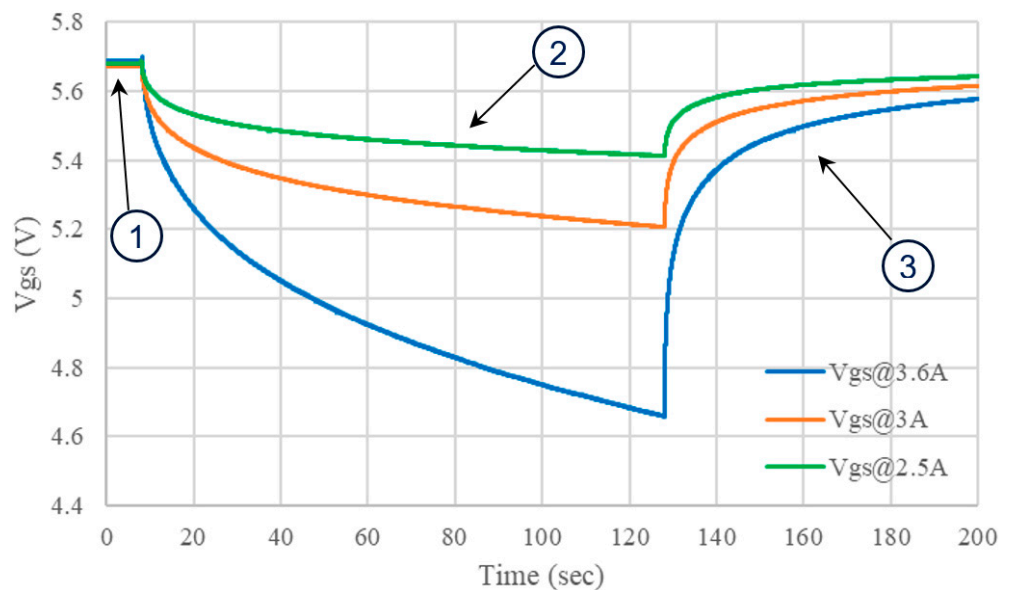


Figure 13. Trend of V_{gs} .

Looking at Figure 13, in the first part (labelled “1”), the device was operating at room temperature, similarly to the previous TSEP, so the value of V_{gs} was measured and $T_{j,0}$ is indirectly estimated when only the sensing current was applied. Once the heating current was applied (“2”), the device began to heat up. When the current pulse was interrupted (“3”), the heating current no longer flowed through the device and V_{gs} was measured (after 100 μs due to the pulse interruption) to obtain $T_{j,end}$. After that, the cooling phase began and V_{gs} started increasing, thus returning to the initial value. The cooling curves of V_{gs} are reported in Figure 14 for different heating currents.

Analyzing the cooling curve, it is evident that, when the pulse is removed, the value of V_{gs} begins to decrease until it reaches room temperature. As aforementioned, as for the previous TSEP, T_j (thus $T_{j,0}$ and $T_{j,end}$) is derived from the Equation (4), as:

$$T_j = \frac{5}{2} + \frac{50}{3} \sqrt{\frac{15^2}{10^4} - 12(5.8232 - V_{gs})} \tag{5}$$

Equation (5) is valid when T_j is in the calibration range. Table 4 reports the average values of Z_{th} computed using Equations (3) and (5) as a function of the heating currents applied. In this case, the difference between the average and extrema is lower than 2%.

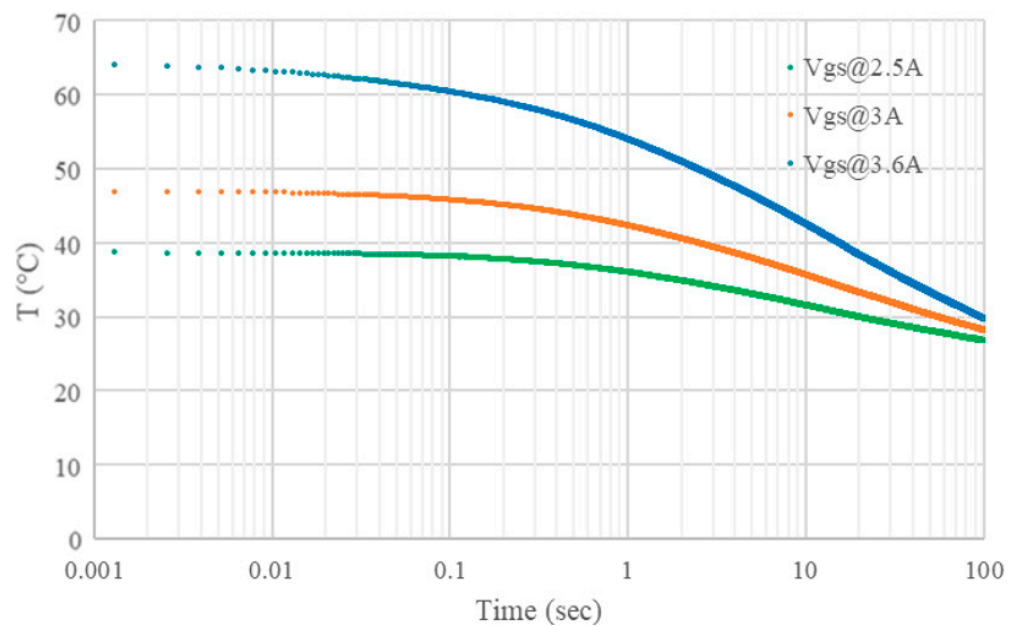


Figure 14. Cooling curves of V_{gs} .

Table 4. Values of Z_{th} obtained using V_{gs} TSEP.

Heating Current		
2.5 A	3 A	3.6 A
29.1 °C/W	28.7 °C/W	28.3 °C/W

The primary advantage of this approach is related to the measurement instrumentation used because it is not particularly critical in terms of performance and accuracy. In fact, the gate-source voltage presents a volt order of magnitude that enables the measurement to be obtained with high precision. The gate current value (typically μA is the order of magnitude) must be properly chosen to avoid the device being accidentally turned off due to the temperature increment.

On the other hand, this approach cannot be used when the gate pin is not available. This case occurs when GaN devices using system-in-package (SIP) solutions are considered because they have a driver circuit integrated and the gate pin is not connected to any outside pin. When the pin is available, V_{gs} TSEP is more suitable than V_{ds} for devices with low conduction resistance. The lack of linearity is an additional (minor) drawback of the method.

3.3. Gate Current TSEP

The setup used to perform the calibration is shown in Figure 15. The calibration was performed by measuring I_g at a sensing voltage of 6 V. The value of the voltage was chosen according to the datasheet threshold voltage. The calibration curve of I_g vs. temperature is shown in Figure 16.

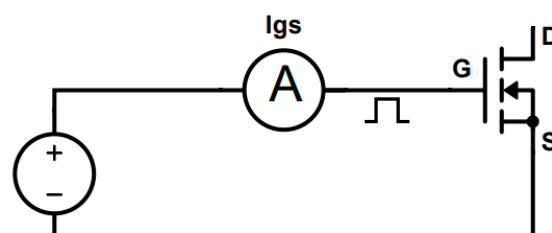


Figure 15. Calibration electrical circuit for I_g .

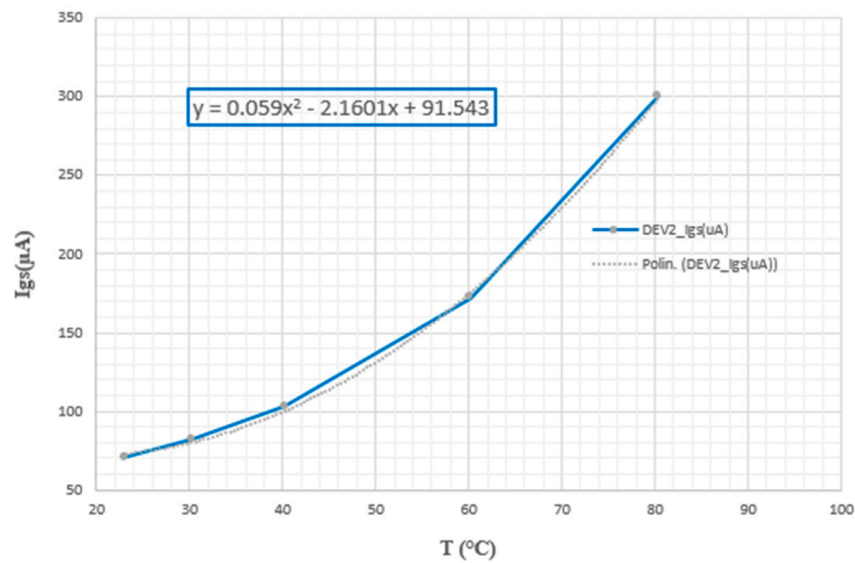


Figure 16. Calibration curve of I_g .

Once the calibration process was performed, the interpolation function was obtained:

$$I_g = 59 \cdot 10^{-9} T^2 - 2160 \cdot 10^{-9} T + 91.543 \cdot 10^{-6} \quad (6)$$

The test conditions are reported in Table 5 and the setup of Figure 17 has been adopted in order to carry out the thermal characterization of the device.

Table 5. Test conditions of I_g .

Parameters	Value
Heating current	2.5 A, 3 A, 3.6 A
Test voltage	6 V
Heating time	120 s

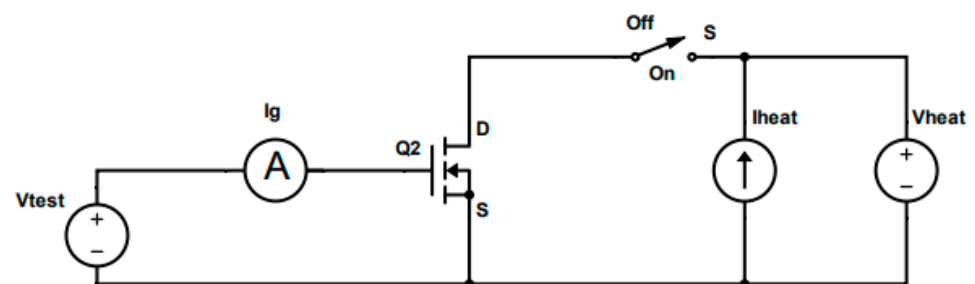


Figure 17. Measurement electrical circuit for I_g .

The result of some measurements is shown in Figure 18.

Figure 18 shows, in the first part, the device gate current at room temperature (the value of I_g at 6 V). As for the previous TSEP, the value of I_g is used for T_{j0} evaluation. Following the application of the pulse, shown in part 2, the device began to heat up. When the pulse was interrupted, in part 3, the heating current no longer flowed through the device. When the pulse was removed, I_g was measured, after 100 μ s, for $T_{j,end}$ evaluation. Then, the cooling phase began and I_g started decreasing and returned to the value presented before the application of the pulse. Some cooling curves of I_g are reported in Figure 19.

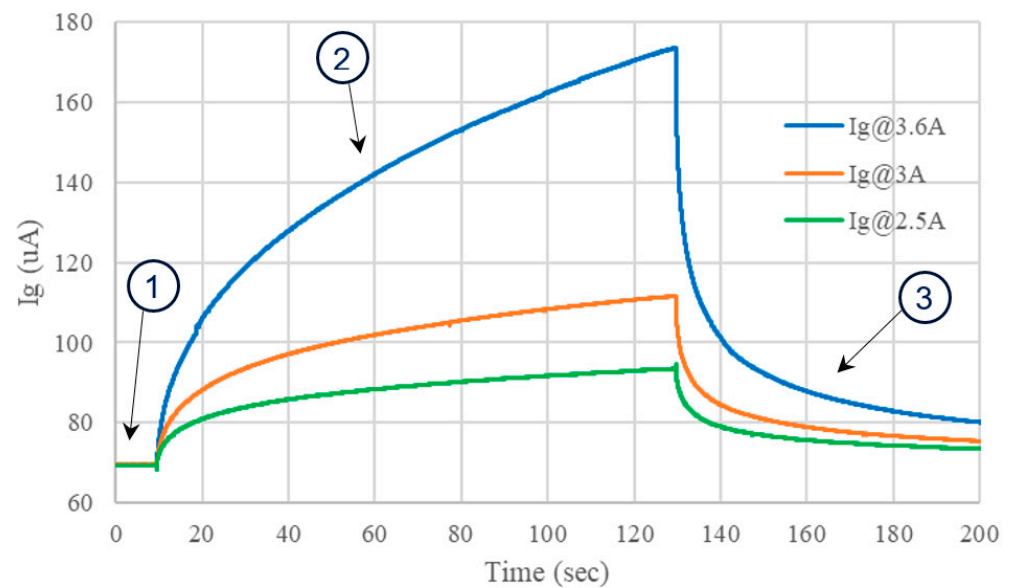


Figure 18. Trend of I_g .

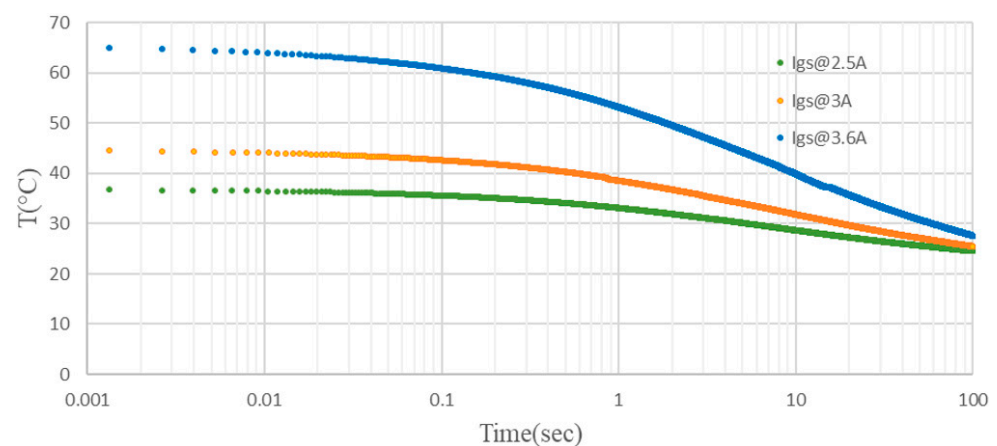


Figure 19. Cooling curves of I_g .

Analyzing the cooling curves, it is evident that when the pulse is removed the value of the gate current begins to decrease and, in the end, reaches room temperature. The value of T_j can be derived and, consequently, the evaluation of $T_{j,0}$ and $T_{j,end}$ is obtained by rewriting Equation (6) as:

$$T_j = 18.3 \left(1 + \sqrt{1 - 50.6 \cdot 10^{-3} \left(91.543 - \frac{I_g}{10^{-6}} \right)} \right) \quad (7)$$

Equation (6) is valid when T_j is in the calibration range. Table 6 reports the average values of the thermal resistance computed using Equations (3) and (7), as a function of the three heating currents applied. In this case, the difference between the average value and the extremes is lower than 2% for each current level.

Table 6. Values of Z_{th} (I_g TSEP).

Heating Current		
2.5 A	3 A	3.6 A
29.0 °C/W	28.6 °C/W	28.1 °C/W

The use of I_g as a TSEP for evaluating the thermal resistance presents almost the same advantages and limits reported for the V_{gs} . The accurate setting of V_{gs} ensures the optimal conditions for the I_g measurement while the device is in on state. However, V_{gs} is preferable to I_g as a TSEP because expensive sensing circuitry is necessary for current measurement due to its low value (μA). In this application, to make the measurement robust to the noise, the Printed Circuit Board has been designed to place the sensing pin close to the DUT. The gate current measurements have been performed using a Keithley 2450 that presents a $5 \mu\text{A}$ resolution, while the DUT gate current order of magnitude is tens or hundreds μA .

In summary, regardless of the TSEP and current level, the difference between the average and minimum or maximum value is always less than 2%. The measurements carried out also show that the three TSEPs (V_{ds} , V_{gs} , and I_g) have a similar temperature trend and that the average Z_{th} presents a limited variation for a given current value. For example, it is about 1% when a 3.6 A heating current is considered, as shown in Table 7. The table also reports the value of R_{th} obtained as the average value among ten measurement repetitions for each TSEP. Differently from Z_{th} , the maximum difference between the average value and the extremes (minimum and maximum R_{th} for the given TSEP) is less than 1%. Another difference between Z_{th} and R_{th} is their dependence on the pulsed heating current. Z_{th} increases as the current decreases while no appreciable difference among the R_{th} values occurs at the three currents. Equation (3) is useful to understand the reasons behind this different behavior. First, it is worth noting that when R_{th} is computed using Equation (3), T_j has reached the steady-state value (the maximum value) and then the value of R_{th} is greater than the value of Z_{th} , which is computed while T_j is increasing. At a low current, the steady-state temperature is reached after a shorter time, thus the T_j evaluated at 120 s is closer to the one measured at 1000 s than it is in the case of a large current that involves greater temperature variation. Consequently, the value of Z_{th} at a low current is greater than the value at a higher current. However, since the Z_{th} evaluation also depends on the average V_{ds} , and this quantity arises during the heating period when Z_{th} is evaluated, the value of P in Equation (3) is less than the one used for R_{th} , thus reducing the difference among the Z_{th} value evaluated at the three different currents.

Table 7. Comparison of Z_{th} and R_{th} values of all TSEP @3.6A.

TSEP	Z_{th} [$^{\circ}\text{C}/\text{W}$]	R_{th} [$^{\circ}\text{C}/\text{W}$]	Ratio
V_{ds}	28.4	35.4	80.23%
V_{gs}	28.3	35.5	79.72%
I_g	28.1	35.1	80.06%

Finally, as can be seen in Table 7, Z_{th} enables a good estimation of R_{th} , since the former is about 80% of the latter, thus leading to timesaving (1200 s vs. 10,000 s).

Figure 20 shows the comparison between the cooling curves of the 3 TSEPs at the same heating current:

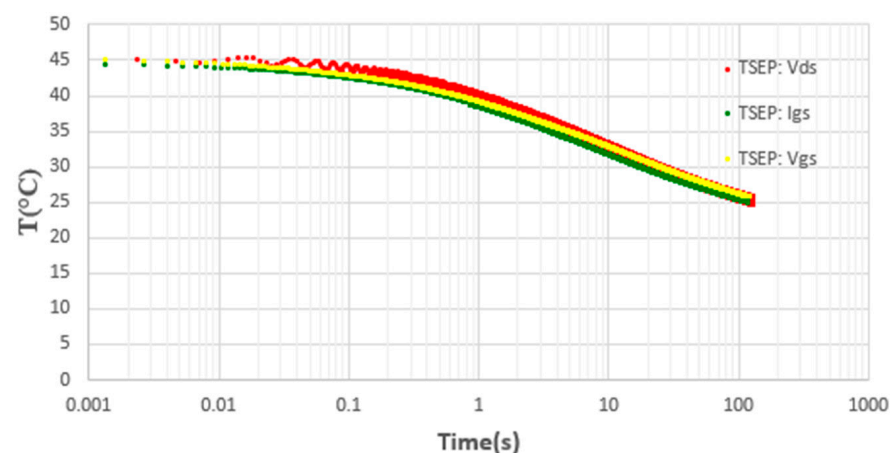


Figure 20. Comparison of cooling curves when the heating current is 3 A.

4. Conclusions

In this paper, some TSEPs were used to estimate the junction temperature of GaN HEMTs devices to evaluate their thermal resistance. An analysis of the advantages and limitations of these methods has been reported alongside some guidelines to select the optimal one. When the device presents a small value of the conduction resistance, and the gate pin is available, the use of V_{ds} to estimate the thermal resistance should be avoided due to the difficulty in appreciating small variations in the order of μV . Another challenge is the choice of a sensing current with negligible self-heating that also enables good accuracy when V_{ds} voltage is measured. Pin availability is another important factor. When the gate pin is not accessible (e.g., system-in-package), the V_{gs} and I_g method cannot be used, and V_{ds} is the only choice. In this case, the equipment resolution is a crucial aspect in terms of estimation accuracy. Moreover, noise could alter the measurements. When the gate pin is available, an advantage of using V_{gs} or I_g is the simplicity of the measurement setup. The nonlinearity of these TSEPs is a minor drawback. However, the use of V_{gs} as a TSEP is preferable to I_g due to the different magnitudes of the two quantities. The gate-source voltage is a few Volts while the gate current is tens or hundreds of Ampere, thus the latter requires more expensive instrumentation to accurately measure the current and, in turn, to estimate the junction temperature.

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References

1. Maxa, J.; Novikov, A.; Nowotnick, M.; Heimann, M.; Jarchoff, K. Phase Change Materials for Thermal Peak Management Applications with Specific Temperature Ranges. In Proceedings of the 2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), San Diego, CA, USA, 29 May–1 June 2018; pp. 92–101.
2. Kang, S.S. Advanced Cooling for Power Electronics. In Proceedings of the 2012 7th International Conference on Integrated Power Electronics Systems (CIPS), Nuremberg, Germany, 6–8 March 2012; pp. 1–8.
3. Jones-Jackson, S.; Rodriguez, R.; Yang, Y.; Lopera, L.; Emadi, A. Overview of Current Thermal Management of Automotive Power Electronics for Traction Purposes and Future Directions. *IEEE Trans. Transp. Electrification* **2022**, *8*, 8–2412. [[CrossRef](#)]
4. Seal, S.; Glover, M.; Mantooh, H.A. Design of a reduced form factor passive heat sink for high power applications. In Proceedings of the 2015 IEEE International Workshop on Integrated Power Packaging (IWIPP), Chicago, IL, USA, 3–6 May 2015; pp. 44–47.
5. Gautam, D.; Wager, D.; Edington, M.; Musavi, F. Performance comparison of thermal interface materials for power electronics applications. In Proceedings of the 2014 IEEE Applied Power Electronics Conference and Exposition—APEC 2014, Fort Worth, TX, USA, 16–20 March 2014; pp. 3507–3511.
6. Stinson-Bagby, K.; Huff, D.; Katsis, D.; Van Wyk, D.; Lu, G.Q. Thermal performance and microstructure of lead versus lead-free solder die attach interface in power device packages. In Proceedings of the IEEE International Symposium on Electronics and the Environment, 2004, Scottsdale, AZ, USA, 10–13 May 2004, 2004. Conference Record; pp. 27–32.
7. Andresen, M.; Ma, K.; Buticchi, G.; Falck, J.; Blaabjerg, F.; Liserre, M. Junction Temperature Control for More Reliable Power Electronics. *IEEE Trans. Power Electron.* **2018**, *33*, 765–776. [[CrossRef](#)]
8. Pavlidis, G.; Kendig, D.; Heller, E.R.; Graham, S. Transient Thermal Characterization of AlGaIn/GaN HEMTs Under Pulsed Biasing. *Trans. Electron Devices* **2018**, *65*, 1753–1758. [[CrossRef](#)]
9. Cheng, S.; Liu, C.-H. The novel V-groove TO 3P packaging design and electrical test of AlGaIn/GaN power HEMT. In Proceedings of the 2012 IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL), Kyoto, Japan, 10–13 June 2012; pp. 1–5.
10. Cheng, S.; Li, C.Y.; Liu, C.H.; Chou, P.-C. Characterization and thermal analysis of packaged AlGaIn/GaN power HEMT. In Proceedings of the 2011 6th International Microsystems, Packaging, Taipei, Taiwan, 19–21 October 2011, Assembly and Circuits Technology Conference (IMPACT); pp. 195–197.
11. Šodan, V.; Stoffels, S.; Oprins, H.; Baelmans, M.; Decoutere, S.; De Wolf, I. A modeling and experimental method for accurate thermal analysis of AlGaIn/GaN powerbars. In Proceedings of the 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Hong Kong, China, 10–14 May 2015; pp. 377–380.

12. González, B.; Lázaro, A.; Rodríguez, R. RF Extraction of Thermal Resistance for GaN HEMTs on Silicon. *IEEE Trans. Electron Devices* **2022**, *69*, 2307–2312. [[CrossRef](#)]
13. Jones, E.A.; de Rooij, M. Thermal Characterization and Design for a High Density GaN-Based Power Stage. In Proceedings of the 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, USA, 31 October–2 November 2018; pp. 295–302.
14. Pavlidis, G.; Yates, L.; Kendig, D.; Lo, C.-F.; Marchand, H.; Barabadi, B.; Graham, S. Thermal Performance of GaN/Si HEMTs Using Near-Bandgap Thermoreflectance Imaging. *IEEE Trans. Electron Devices* **2020**, *67*, 822–827. [[CrossRef](#)]
15. Kuzmik, J.; Bychikhin, S.; Neuburger, M.; Dadgar, A.; Krost, A.; Kohn, E.; Pogany, D. Transient thermal characterization of AlGaIn/GaN HEMTs grown on silicon. *IEEE Trans. Electron Devices* **2005**, *52*, 1698–1705. [[CrossRef](#)]
16. González, B.; De Santi, C.; Rampazzo, F.; Meneghini, M.; Nunez, A.; Zanoni, E.; Meneghesso, G. Geometric Modeling of Thermal Resistance in GaN HEMTs on Silicon. *IEEE Trans. Electron Devices* **2020**, *67*, 5408–5414. [[CrossRef](#)]
17. Sun, Y.; Zhang, H.; Yang, L.; Hu, K.; Xing, Z.; Liang, K.; Yu, H.; Fang, S.; Kang, Y.; Wang, D.; et al. Correlation between Electrical Performance and Gate Width of GaN-Based HEMTs. In *IEEE Electron Device Letters*; IEEE: Piscataway, NJ, USA, 2022; Volume 43, pp. 1199–1202.
18. Tomoaki, H.; Funaki, T. Transient Thermal Characterization for GaN HEMTs with p-Type Gate. *Trans. Jpn. Inst. Electron. Packag.* **2020**, *13*, E19002.
19. Avenas, Y.; Dupont, L.; Khatir, Z. Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters—A Review. *Trans. Power Electron.* **2012**, *27*, 3081–3092. [[CrossRef](#)]
20. Rizzo, S.A.; Susinni, G.; Iannuzzo, F. Intrusiveness of Power Device Condition Monitoring Methods: Introducing Figures of Merit for Condition Monitoring. *IEEE Ind. Electron. Mag.* **2022**, *16*, 60–69. [[CrossRef](#)]
21. Sarkany, Z.; Musolino, M.; Sitta, A.; Calabretta, M.; Nemeth, M.; Farkas, G.; Rencz, M. Thermal transient testing alternatives for the characterisation of GaN HEMT power devices. In Proceedings of the 2022 28th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Dublin, Ireland, 28–30 September 2022; pp. 1–4.
22. Susinni, G.; Rizzo, S.; Iannuzzo, F.; Raciti, A. A non-invasive SiC MOSFET Junction temperature estimation method based on the transient light Emission from the intrinsic body diode. *Microelectron. Reliab.* **2020**, *114*, 113845. [[CrossRef](#)]
23. Dupont, L.; Avenas, Y.; Jeannin, P.-O. Comparison of junction temperature evaluations in a power IGBT module using an IR camera and three thermosensitive electrical parameters. *IEEE Trans. Ind. Appl.* **2013**, *49*, 1599–1608. [[CrossRef](#)]
24. Yang, S.; Xiang, D.; Bryant, A.; Mawby, P.; Ran, L.; Tavner, P. Condition Monitoring for Device Reliability in Power Electronic Converters: A Review. *Trans. Power Electron.* **2010**, *25*, 2734–2752. [[CrossRef](#)]
25. Sathik, M.H.M.; Prasanth, S.; Sasongko, F.; Padmanabhan, S.K.; Pou, J.; Simanjorang, R. Online junction temperature for off-the-shelf power converters. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018; pp. 2769–2774.
26. Kempiak, C.; Lindemann, A.; Idaka, S.; Thal, E. Investigation of an Integrated Sensor to Determine Junction Temperature of SiC MOSFETs During Power Cycling Tests. In Proceedings of the 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019—ECCE Asia), Busan, Republic of Korea, 27–30 May 2019; pp. 3084–3089.
27. Fritz, N.; Kamp, T.; Polom, T.A.; Friedel, M.; Doncker, R.W.D. Evaluating On-State Voltage and Junction Temperature Monitoring Concepts for Wide-Bandgap Semiconductor Devices. *IEEE Trans. Ind. Appl.* **2022**, *58*, 7550–7561. [[CrossRef](#)]
28. Etoz, B.; Gonzalez, J.O.; Deb, A.; Jahdi, S.; Alatise, O. Impact of threshold voltage shifting on junction temperature sensing in GaN HEMTs. In Proceedings of the 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 5–9 September 2022; p. 1.
29. Ayadi, M.; Fakhfakh, M.; Moez, G.; Neji, R. Electro-Thermal Simulation of a Three Phase Inverter with Cooling System. *J. Model. Simul. Syst.* **2010**, *1*, 163–170.
30. Liu, B.; Guo, C.; Wang, S.; Wei, H.; Wei, L. Online Junction Temperature Measurement Method of SiC MOS Devices Using Multiple Electrical Parameters at Transient Surge Current. In Proceedings of the 2020 3rd International Conference on Electron Device and Mechanical Engineering (ICEDME), Suzhou, China, 1–3 May 2020; pp. 48–51.
31. Sharma, K.; Barón, K.M.; Ruthardt, J.; Kallfass, I. Online Junction Temperature Monitoring of Wide Bandgap Power Transistors using Quasi Turn-on Delay as TSEP. In Proceedings of the 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Redondo Beach, CA, USA, 7–11 November 2021; pp. 129–134.
32. Liu, J.; Chen, H.; Lin, J.; Li, Z.; Wu, H.; Ji, B. Investigation of TSEPs based on the feature extraction from the gate current. In Proceedings of the 11th International Conference on Power Electronics, Machines and Drives (PEMD 2022), Newcastle, UK, 21–23 June 2022; pp. 451–455.
33. Borghese, A.; Di Costanzo, A.; Riccio, M.; Maresca, L.; Breglio, G.; Irace, A. Gate Current in p-GaN Gate HEMTs as a Channel Temperature Sensitive Parameter: A Comparative Study between Schottky- and Ohmic-Gate GaN HEMTs. *Energies* **2021**, *14*, 8055. [[CrossRef](#)]
34. Gonzalez, J.O.; Alatise, O.; Hu, J.; Ran, L.; Mawby, P. Temperature sensitive electrical parameters for condition monitoring in SiC power MOSFETs. 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, UK, 19–21 April 2016; pp. 1–6.
35. Susinni, G.; Rizzo, S.A.; Iannuzzo, F. Two Decades of Condition Monitoring Methods for Power Devices. *Electronics* **2021**, *10*, 683. [[CrossRef](#)]

36. Hedayati, M.H.; Dymond, H.C.P.; Liu, D.; Stark, B.H. Fast temperature sensing for GaN power devices using E-field probes. In Proceedings of the 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), Aalborg, Denmark, 9–12 November 2020; pp. 1–7.
37. Feng, S.; Hu, P.; Zhang, G.; Guo, C.; Xie, X.; Chen, T. Determination of channel temperature of AlGaIn/GaN HEMT by electrical method. In Proceedings of the 2010 26th Annual IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), Santa Clara, CA, USA, 21–25 February 2010; pp. 165–169.
38. Shan, Y.; Gao, W.; Huang, Z.; Kuang, W.; Wu, Z.; Zhang, B. Test Methods and Principles of Thermal Resistance for GaN HEMT Power Devices. In Proceedings of the 2020 21st International Conference on Electronic Packaging Technology (ICEPT), Guangzhou, China, 12–15 August 2020.
39. Roschatt, P.M.; McMahon, R.A.; Pickering, S. Temperature measurements of GaN FETs by means of average gate current sensing. In Proceedings of the 2015 IEEE 11th International Conference on Power Electronics and Drive Systems, Sydney, NSW, Australia, 9–12 June 2015; pp. 673–677.

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