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Published in:
Microelectronics Reliability

DOI (link to publication from Publisher):
10.1016/j.microrel.2023.115138

Publication date:
2023

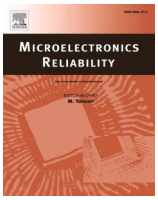
Document Version
Publisher's PDF, also known as Version of record

Microelectronics Reliability 150 (2023) 115138

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Accuracy estimation of low-current voltage drop method for junction temperature monitoring under DC power cycling

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ARTICLE INFO

Keywords:
TSEP method
DC power cycling
Accuracy estimation of TSEP
Infrared camera
Bond wire lift-off

ABSTRACT

A thorough accuracy estimation of the well-known low-current voltage drop method is carried out in this paper. A high-performance infrared camera is utilized as the reference in a DC power-cycling test on a commercial IGBT power module. The result shows that the low-current voltage drop method produces generally a higher temperature than the actual, in particular at the bond wire's joint point. However, a simple compensation method with a linear function can be easily adopted to compensate the temperature difference. After compensation, the maximum error of temperature swing is 0.28 °C.

1. Introduction

Nowadays, renewable energies are playing a more important role than in the past, in particular solar energy and wind energy. However, being these sources fluctuating in nature, a power converter is vital to interface them to the power grid. Power converters are in charge of the voltage- and frequency regulation as well as the power flow control. Therefore, the reliability of power converters directly affects the entire system's reliability. Let alone, due to the large per-unit power capacity of renewable power systems, even a minor failure will result in severe operational economic losses (OpEx) and endanger safety. More in detail, as the key components in power converters, power semiconductor devices are the most fragile part and are usually the main cause of power converter failures [1]. Therefore, improving the reliability of power semiconductor devices is now highly demanded.

Insulated gate bipolar transistors (IGBT) are now widely used in several applications. Although their production process has been improved a lot in the past decades and the resulting chip-level reliability is now much higher than in the past, the overall reliability is still limited at the package level [2].

As shown in Fig. 1, direct bonded copper (DBC) technology is by far the most adopted technology for the substrate of power modules. The DBC is soldered onto the baseplate and the IGBT chip is soldered onto the top copper of the DBC. Bond wires are connected to the chip surface to form the electrical connections among chips and terminals, where ultrasonic welding is most widely used. Inside the power module, there are several interfaces between different materials, for example, the interface between baseplate and DBC, between DBC and chip, and between chip and bond wires. In the practical operations of power converters, the load is changing frequently, especially in renewable energy systems. Therefore, the power losses generated on power modules are always changing, resulting in the junction temperature fluctuation in power devices. Due to the different expansion coefficients of different materials, the interfaces undertake mechanical stress when there is a temperature swing. After bearing such stress for a long time, degradation will occur, where solder layer delamination and bond wire lift-off are most common [2]. After these degradations happen, the thermal impedance and on-resistance of the power module will increase, resulting in a higher temperature swing in turn. When the degradation further develops, catastrophic failures will finally happen.

To evaluate the package reliability, DC power cycling test is proposed and is now the most adopted method to estimate the device lifetime [3,4]. In the DC power cycling test, temperature swing is the most important factor that determines the device lifetime [5], even a small difference in temperature swing leads to a significant difference in device lifetime [6], hence knowing the accurate temperature swing is important. To obtain the junction temperature in DC power cycling, temperature-sensitive electric parameters (TSEPs) based methods have been widely used [7–10]. For IGBTs, the low-current voltage drop method is commonly adopted, where the V_{ce} under a small current is used to infer the junction temperature. However, due to the thickness of the chip, whether the inferred junction temperature can represent the real temperature of the concerned interface remains unknown [11]. For example, when concentrating on the bond wire lift-off, the interface we

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https://doi.org/10.1016/j.microrel.2023.115138
Received 2 June 2023; Accepted 17 July 2023
Available online 1 October 2023

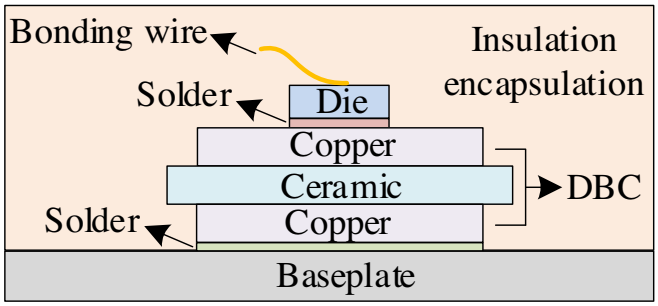

Fig. 1. Common structure of power modules.

care about is between the top surface of the chip and the bond wire where the joint point sits, however, the inferred junction temperature represents the temperature inside the chip, more in detail, represents the average temperature of the area around the current path inside the chip. Therefore, there will be a difference between the TSEP based result and the actual temperature we care about. Therefore it is of great significance to conduct the accuracy estimation of TSEP based method for junction temperature monitoring under DC power cycling, which will provide guidance for using TSEP methods to estimate device lifetime under power cycling.

In this paper, firstly the low-current voltage drop method and infrared camera temperature measurement system are introduced. Then a DC power cycling is carried out for a commercial IGBT power module and the TSEP method is used to estimate the junction temperature. Afterwards, the temperature of the chip surface, the temperature of the joint point of bond wires, and the temperature of bond wires are recorded by the infrared camera and are compared to the TSEP method. Based on the obtained result, a simple linear compensation method is proposed, which will help improve the estimation accuracy of TSEP methods. In this paper, the concerned failure mechanism is focused on the bond wire lift-off, but this methodology is also applicable to other analyses.

2. Introduction of low-current voltage drop method and infrared camera temperature measurement system

First of all, the DC power cycling test needs to be introduced, its schematic is shown in Fig. 2. DC power cycling test is to apply thermal cycling to the device under test (DUT), emulating the practical operations. For IGBTs, the device is always turned on, and the load current I_L flowing through the device is controlled by the external power supply. Unlike the practical switching condition, there are only conduction losses under DC power cycling; therefore, the gate voltage usually needs to be lowered to reach the target temperature swing. To extract the junction temperature, a positive low-current I_S is continuously injected into the device, under this small current, a relationship between voltage drop V_{ce} and junction temperature can be obtained in advance in a calibration process. Furthermore, to achieve high measurement accuracy, extra measurement cables are used to monitor the voltage on the devices, avoiding the voltage drop in the cable due to the current as shown in Fig. 3.

During the DC power cycling test, the maximum junction temperature can be extracted by measuring the V_{ce} under low current right after the large load current is removed, and the minimum temperature can be measured right before the appearance of the load current as shown in Fig. 4.

It is also worth mentioning that a proper I_S needs to be selected as the injection current. In our debugging process, it is found that when choosing a larger injection current, the voltage drop V_{ce} will reach its steady state faster. This is caused by two factors, one is that a larger injection current will extract the extra carrier inside IGBT at a faster speed; therefore, the voltage drop will stabilize faster. Another is due to the characteristics of the current source we are using a larger injection current will help go through the oscillation period faster during the current switching transient. However, a too large current will bring extra heating power which will affect the measurement accuracy. By following this trade-off principle, we finally choose 100 mA as our injection current.

In our test, the commercial power tester PWT-2400A is used as the DC power cycling test platform as shown in Fig. 5. The temperature of the device is controlled by the Julabo temperature control system.

In order to obtain the actual temperature of the device, a high-performance infrared camera is used as the reference. To guarantee measurement accuracy, special treatment needs to be conducted on the DUT first. In our test, one IGBT chip in a commercial IGBT power module from Infineon company is selected as DUT as shown in Figs. 6 and 7. First, the gel is removed using the chemical method, and then the black paint is applied to the surface of the device as shown in Fig. 8. To keep the effect brought by the black paint minimal, the paint was applied layer by layer until it could just cover the surface of the chip so that the thickness of the paint is as thin as possible.

The high-performance infrared camera has a resolution of 1280 × 1024 with a frame rate of 181 Hz. The infrared camera is set perpendicular to the chip surface as shown in Fig. 9.

In our test, the gate voltage is selected as 13 V, the load current ranges from 15A to 33A, and the on- and off-period are both 2 s. During the power cycling test, the TSEP based results are collected from the power tester platform, and the actual temperatures are recorded by the infrared camera during the power cycling. Then a comprehensive comparison can be carried out between these results.

3. Experimental results

For each test current, the test results are collected after running for some time until reaching the thermal equilibrium. In this paper, the concerned failure mechanism is about bond wire lift-off, therefore, three areas are chosen (indicated in Fig. 12) whose actual temperatures are

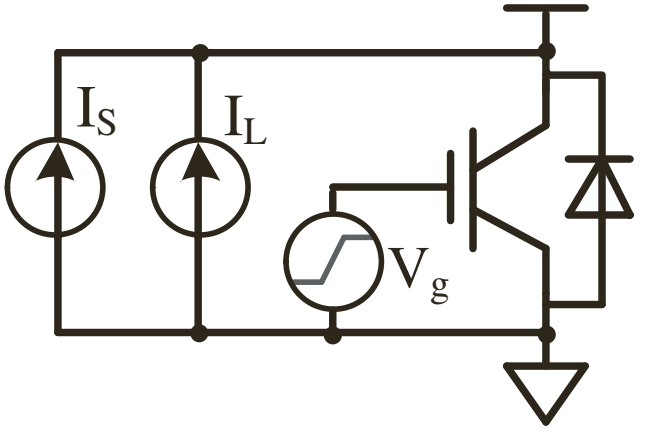

Fig. 2. Test schematic of DC power cycling.

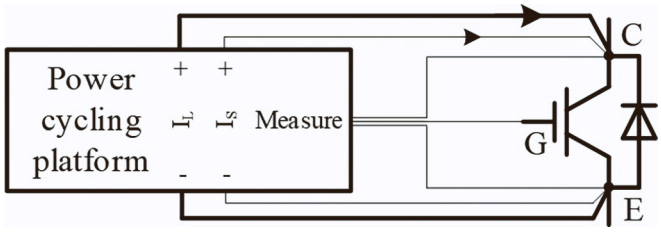

Fig. 3. Connections of the DC power cycling platform.

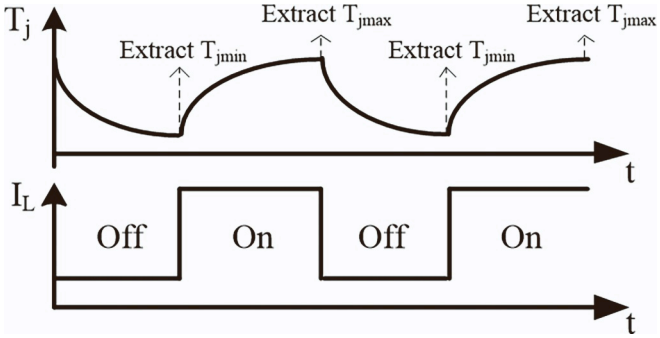

Fig. 4. Current and Tj waveform under DC power cycling.

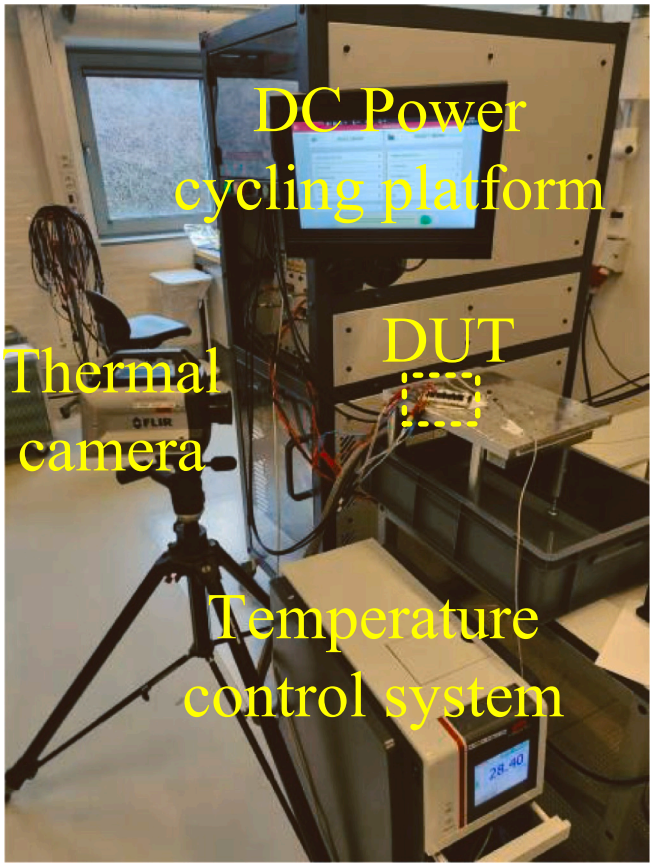

Fig. 5. Photo of DC power cycling test platform.

measured by the infrared camera, which are the average temperature of a rectangular window on the chip surface (active area zone), the temperature of the joint point between the bond wire and chip surface, and the temperature of the bond wire. The thermal images at the maximum temperature point (refer to the T_{jmax} in Fig. 4) and minimum temperature point (refer to the T_{jmin} in Fig. 4) during power cycling under different load currents are shown from Figs. 10 to 14. All the data of minimum temperature, maximum temperature, and temperature swing collected from TSEP method and infrared camera is concluded in Table 1.

From the experimental data, it is seen that the average chip surface temperature is the lowest one, the joint point of bonding wire has a slightly higher temperature than the chip surface, and they are both lower than TSEP based results. For bond wire temperature, the minimum temperature is always lower than the TSEP based results, its maximum temperature depends on the current, when the current is low,

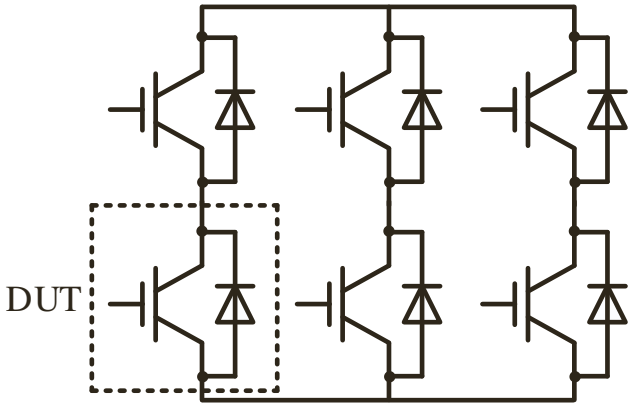

Fig. 6. Schematics of the power module.

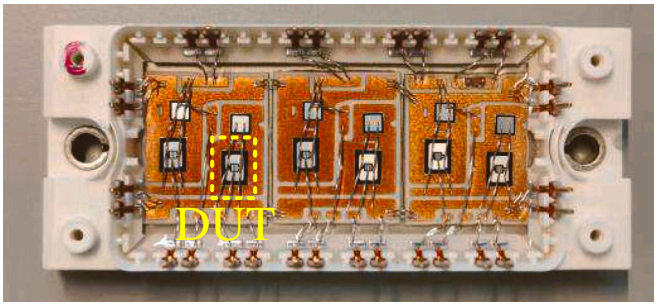

Fig. 7. Photo of the power module before treatment.

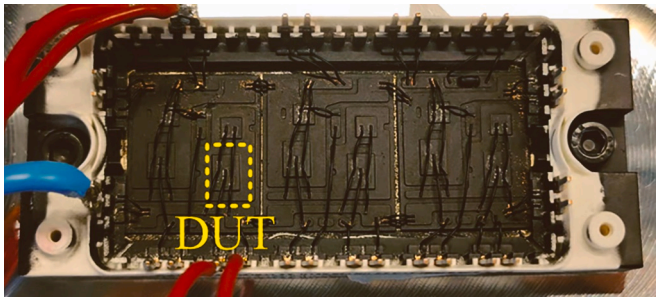

Fig. 8. Photo of the power module after special treatment.

it is lower than TSEP based result, and when the current is large, it becomes larger than that of TSEP based, which is reasonable because the heat generated on the bond wire is brought by the current.

The result can be interpreted that the TSEP based results represent the junction temperature of the current flowing area inside the chip, which should be the highest one. Due to the thickness of the chip, there is thermal impedance between the chip surface and the junction area, therefore the temperature of the chip surface is lower than the junction temperature. At the same time, due to the contact resistance of the joint point between bond wire and chip surface, the joint point's temperature is slightly higher than the surface temperature. As for the bond wire, it is another heating source during power cycling, hence the temperature of the bond wire depends on the value of the current.

The temperature swing is calculated for each data point as shown in Table 1. It is known that the temperature swing is the dominant factor resulting in package failure. When focusing on the bond wire lift-off, after comparing the temperature swing obtained from TSEP method and the temperature swing of the joint point, it is found that the difference is not as large as the difference of the absolute temperature. The

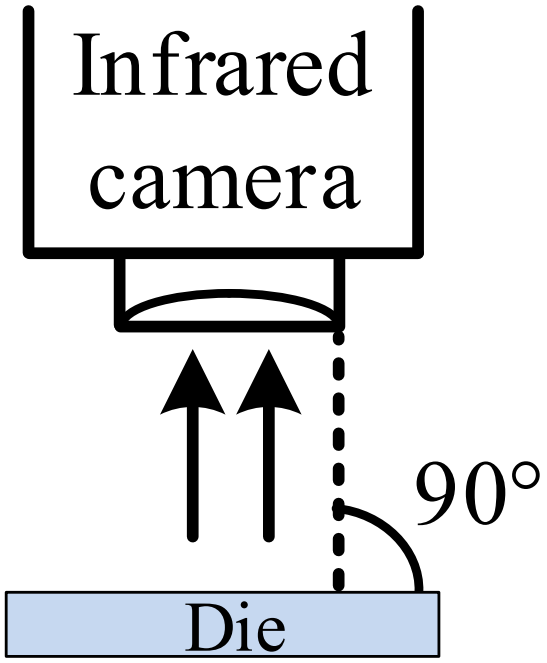

Fig. 9. Diagram of the position of the infrared camera.

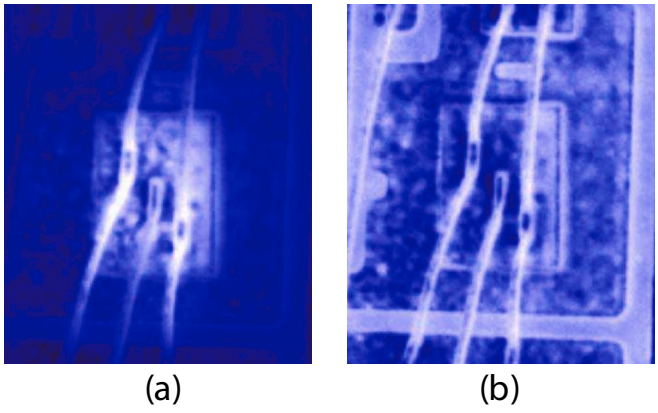

Fig. 10. Thermal image of the chip under 15A power cycling (a) At T_{jmax}. (b) At T_{jmin}.

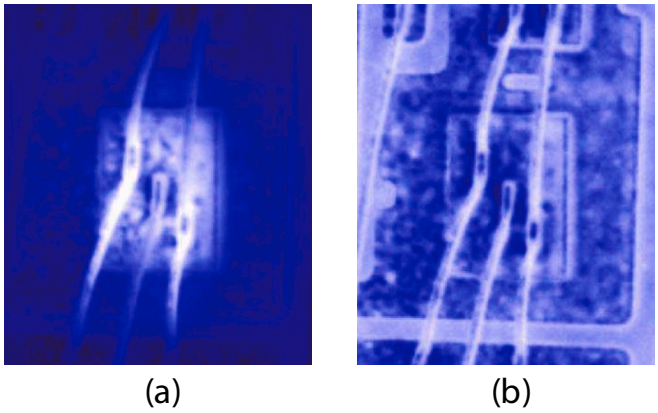

Fig. 11. Thermal image of the chip under 20A power cycling (a) At T_{jmax}. (b) At T_{jmin}.

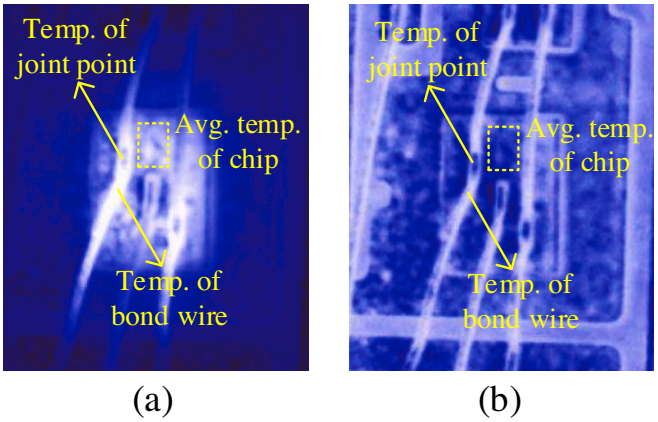

Fig. 12. Thermal image of the chip under 25A power cycling (a) At T_{jmax}. (b) At T_{jmin}.

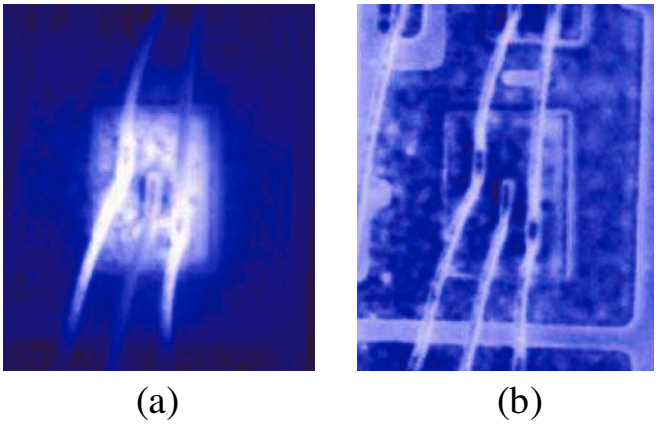

Fig. 13. Thermal image of the chip under 30A power cycling (a) At T_{jmax}. (b) At T_{jmin}.

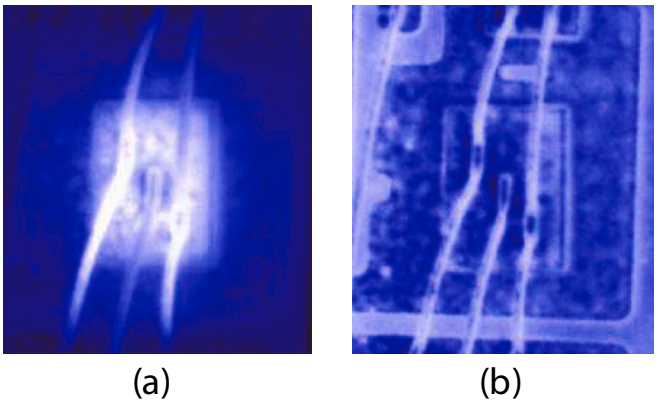

Fig. 14. Thermal image of the chip under 33A power cycling (a) At T_{jmax}. (b) At T_{jmin}.

maximum difference of temperature occurs under 25A power cycling, which is 1.5 °C. Although a 1.5 °C difference seems not like a large value, according to [6,12,13], the temperature swing is an exponential item when estimating the device lifetime, whose exponent value is −4.416. When taking the difference of temperature swing under 25A into account, where TSEP based result is 37.2 °C and the actual temperature of the joint point is 35.7 °C, this 1.5 °C difference will result in a longer lifetime of 20 %. Therefore, it is of great significance to compensate this

Table 1
Experimental data under different load currents (Data format is minimum temperature, maximum temperature, temperature swing).

I/A	V_{ce} based	Avg. temp. of chip sur.	Joint point temp.	Bond wire temp.
15	58.1, 74.5, 16.4	51.3, 66.1, 14.8	52.1, 67.2, 15.1	55.6, 72.3, 16.7
20	61.7, 87.3, 25.6	54.4, 78, 23.6	55.1, 79.5, 24.4	59.3, 86.1, 26.8
25	65.4, 102.6, 37.2	57.9, 92.9, 35	59.2, 94.9, 35.7	63.1, 103.4, 40.3
30	71.8, 124.3, 52.5	63.6, 113.9, 50.3	64.6, 116.5, 51.9	69.5, 128.3, 58.8
33	76.3, 140.5, 64.2	67.7, 129.6, 61.9	68.7, 133, 64.3	74, 146.5, 72.5

difference.

4. Proposed compensation method

When we are investigating the bond wire lift-off failure, the joint point temperature of the bonding wire is what we care about. From the above experimental results, it is found that there is a temperature difference between the TSEP based result and joint point temperature. To compensate this temperature difference, a linear compensation method is proposed based on obtained experimental results. The relationships between the TSEP based results and infrared camera results are plotted in Figs. 15, 16, and 17.

It is seen that the actual temperatures have a good linearity with the TSEP based results. Hence a linear fitting curve can be adopted as shown in these figures. More specifically, the expressions between the actual temperature of joint point and TSEP based result for T_{jmin}, T_{jmax}, and temperature swing are written in all these three figures. By using these expressions, the temperature difference can be easily compensated, making the estimation result from TSEP method closer to reality. For the temperature swing, the maximum error between the compensated TSEP result and actual result is 0.28 °C, which is much smaller than the uncompensated one 1.5 °C. Therefore, this compensation method can help improve the estimation accuracy of device lifetime in DC power cycling tests.

There may be a concern that the work in this paper is based on a gel-removed power module, and the decapsulation process will have an effect on the final temperature distributions in the power modules. It is true that the existence of gel will change the temperature distribution, but the work in this paper provides a comprehensive comparison between TSEP method and the actual results, the methodology proposed in this paper is general and can be applied in practical applications with the help of optical fiber temperature measurement methods [14]. For example, during the final power cycling tests, an optical fiber can be put onto the joint point of bond wires in the power module (without the need of removing gel) to monitor its actual temperature, then the compensation method proposed in this paper can be used to compensate the error.

5. Conclusion

In this paper, to facilitate improving the prediction accuracy of device lifetime, an accuracy estimation of low-current voltage drop method for junction temperature monitoring under DC power cycling is conducted. The infrared camera is used as a reference, and the actual temperature of the chip surface, the temperature of the joint point between bond wire and chip surface, and the temperature of the bond wire are obtained through the infrared camera and are compared to the TSEP based results. It is found that the TSEP based temperature is higher than the actual chip surface temperature and that of the bond wire joint point. But the differences in their temperature swings are smaller. To compensate this temperature difference, a simple linear compensation method is proposed, which lowers the error of TSEP based temperature swing from 1.5 °C to 0.28 °C before and after compensation.

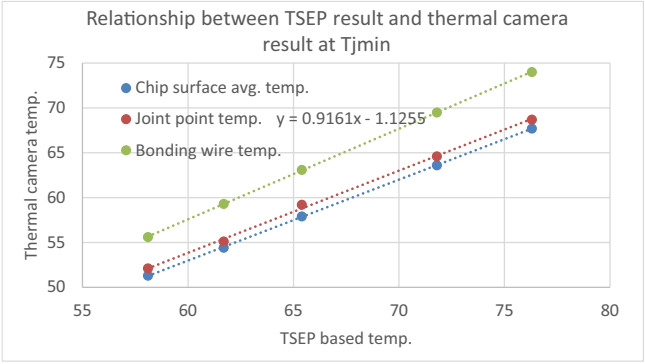

Fig. 15. Relationship between TSEP result and infrared camera result at T_{jmin} in power cycling.

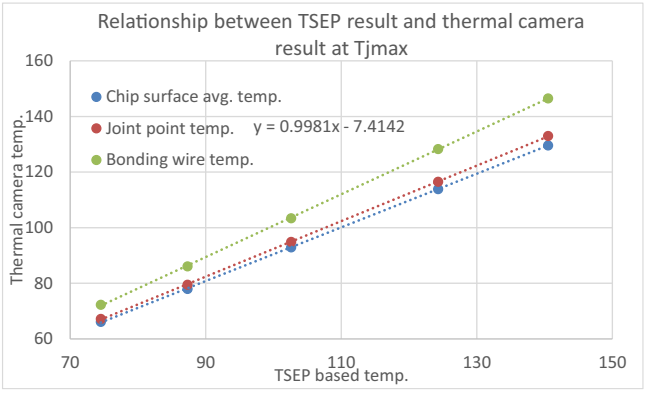

Fig. 16. Relationship between TSEP result and infrared camera result at T_{jmax} in power cycling.

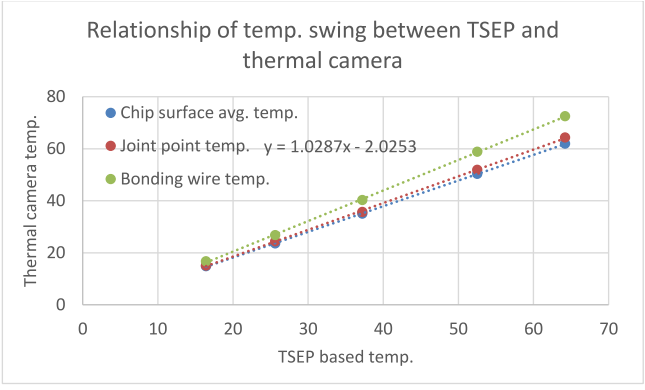

Fig. 17. Relationship of temperature swing between TSEP based result and thermal camera result.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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