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# Highly Efficient and Linearity-Enhanced S-band Doherty Power Amplifier

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***Abstract*—This work presents the design and characterization of a hybrid Doherty power amplifier for $S$ band aiming at enhancing linearity near saturation while maintaining high efficiency. The design combines two highly linear branch amplifiers in a Doherty configuration through a quadrature coupler with reactive termination at the isolated port. At 2.7 GHz, the amplifier demonstrates 13.9 dB small signal gain, 41 dBm saturated power, and 67% maximum efficiency. The linearity is evaluated through two-tone and modulated signal characterizations, showing -30 dBc IMD3 up to 36 dBm of output power. Additionally, the ACPR is -30 dBc and -39 dBc, respectively, before and after digital predistortion.**

***Index Terms*—ACPR, Doherty power amplifier, GaN, IMD3, Linearity-enhanced.**

## I. Introduction

The power amplifier (PA) is a critical component of modern transmitter architectures. With the increasing adoption of complex modulation schemes, PAs are required to deliver the target output power while exhibiting high linearity and efficiency. Achieving these objectives simultaneously is challenging, as efficiency enhancement techniques often involve operating the amplifier closer to saturation, which introduces nonlinear behavior. While system-level linearization techniques, such as digital predistortion (DPD) [1], can mitigate nonlinearity and meet modern requirements, it remains essential to design PAs that inherently satisfy stringent linearity specifications. This approach simplifies the external linearization requirements and reduces the system complexity.

Gallium nitride (GaN) technology has emerged as the preferred choice for high-efficiency PAs due to its superior power density, high breakdown voltage, and wideband capabilities. Compared to GaAs, which is limited to watt-level output power at MMIC scale [2], GaN offers a better tradeoff between power capability and design complexity. Since its initial development [3], GaN technology has significantly matured, with continuous improvements in device fabrication, epitaxial growth, and packaging [4]. However, thermal management remains a key design consideration, as the high power density of GaN devices results in elevated junction temperatures, impacting long-term reliability and efficiency [5]. Proper thermal optimization, including the use of high-thermal-conductivity substrates such as silicon carbide (SiC), is essential to leverage the full potential of GaN-based amplifiers.

This work focuses on designing a Doherty power amplifier (DPA) optimized for enhancing linearity while maintaining good efficiency, gain and output power targeting an operating frequency band centered at 2.65 GHz. The target requirement is set at 36 dBm of output power, with a small signal gain greater than 12 dB, which is sufficient for the PA to be measured with a reasonable input drive in the order of 100 mW. The linearity target is set to a third-order intermodulation (IMD3) lower than -30 dBc in a two-tone test with relatively wide band of 20 MHz, while simultaneously maximizing efficiency.

## II. Design

The DPA is developed using a stand-alone class-AB PA, optimized for linearity, as the main amplifier, while the auxiliary amplifier adopts the same PA biased in class-C. To enhance the linearity of the DPA, a quadrature coupler is employed as the output combiner. For narrowband DPAs, increasing efficiency at the first peak can be achieved through waveform-engineered single-stage designs, such as class-F [6]. However, in this work, where the primary focus is on linearity, a class-AB PA [7] optimized for linearity has been preferred over efficiency-oriented topologies.

The class-AB branch PA is designed in a 200 MHz band centered at $f_0 = 2.65$ GHz, compatible with a hybrid implementation targeting 5G applications. The 10 W packaged Wolfspeed GaN HEMT (CG2H40010F) is selected as active device.

An input stabilization circuit ensuring unconditional stability in and out of the band is designed. It includes a parallel RC (225 Ω || 2 pF) block connected to the gate of the transistor. The stability is verified for several bias conditions, foreseeing a gate bias voltage around class-B and deep class-AB (i.e., ranging between -3.2 V and -2.9 V) to exploit the IMD3 sweet spots thus trading off between gain, efficiency, and linearity.

Following the design strategy discussed in [8], the source and load terminations are simultaneously optimized to satisfy the requirements of IMD3 lower than -30 dBc, maximum PAE and power above 36 dBm, to account for combiner losses. Considering the operating frequency of $f_0 = 2.65$ GHz and the maximum frequency of operation of the packaged transistor $f_p = 8$ GHz, the terminations are optimized up to the second harmonic. Higher harmonics have been verified to have a negligible impact on the performance in the target band.

The simulated single-tone and two-tone fundamental load pull contours at an input power of 24 dBm are shown in Fig. 1, providing a basis for selecting the fundamental load termination $\Gamma_{L,f0}$.

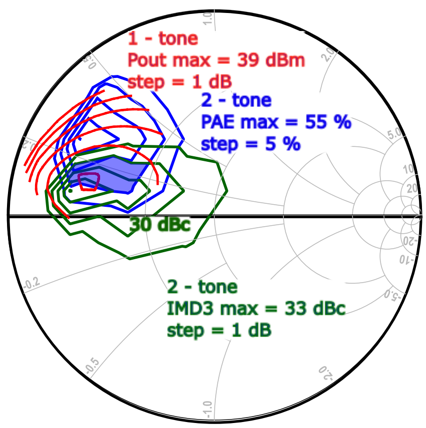



Fig. 1: Simulated fundamental load pull contours at 2.65 GHz for the selected $\Gamma_{S,f_0}/\Gamma_{S,2f_0}$ and $\Gamma_{L,bb}/\Gamma_{L,2f_0}$: single-tone output power (red), and two-tone PAE (blue) and |IMD3| (green) at 24 dBm input power. The light shaded area corresponds to the design space for $\Gamma_{L,f_0}$ based on the power and linearity constraints, with a |IMD3| better than 30 dBc.

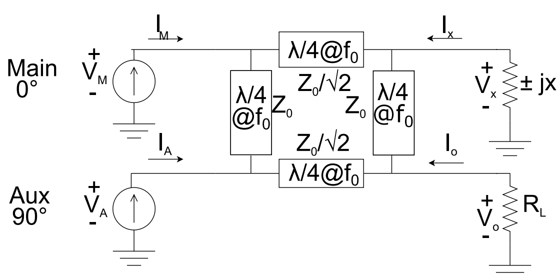
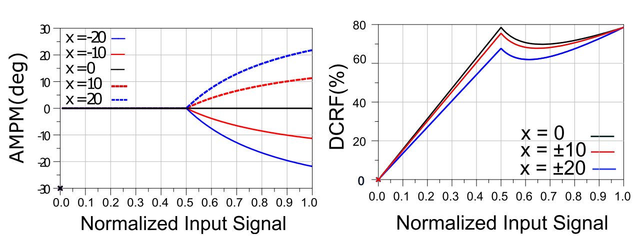



Fig. 2: Schematic of the quadrature-coupler based combiner.

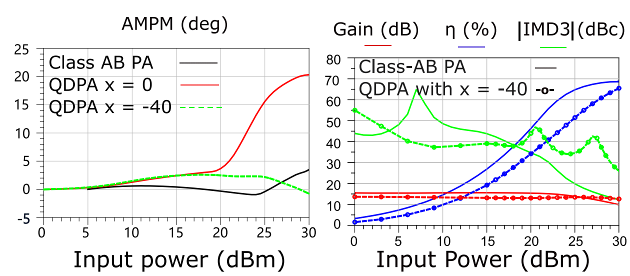



(a) (b)

Fig. 3: Simulated (a) AM-PM and (b) efficiency performance of the DPA adopting the quadrature coupler of Fig. 2.

A quadrature coupler is selected as the Doherty combiner to enhance the linearity of the module [9]. As shown in Fig. 2, the coupler features four ports, each connected through quarter-wave transmission lines. A specific feature of this combiner is that the isolated port is terminated with a small reactive load, which modifies the output voltage profile. This reactive termination introduces an additional degree of freedom, enabling fine-tuning of the overall load line and optimization of both amplitude-to-amplitude modulation (AM-AM) and amplitude-to-phase modulation (AM-PM) behaviors. To investigate its linearity enhancement capabilities, a simplified simulation setup is developed, as shown in Fig. 2, where two ideal current sources emulate the signals from the main and auxiliary branches in a classical DPA configuration. Using this setup, the overall AM-AM and AM-PM characteristics are simulated. Fig. 3a illustrates how increasing the reactive loading at the isolated port significantly affects AM-PM behavior compared to a short termination. The phase distortion varies when the auxiliary branch is activated, with the reactive loading actively shaping the output voltage profile. Meanwhile, as shown in Fig. 3b, the efficiency remains approximately higher than 60% within the Doherty region, despite changes to the reactive loading.

The AM-PM distortion of the DPA is mainly influenced by the variation of the input impedance of the main due to the load modulation. Therefore, the reactive load at the isolated port must be carefully adjusted to compensate for this distortion. Fig. 4 shows that the AM-PM of the stand-alone class-AB PA is almost flat until 20 dBm, thanks to the selection of the most linear bias point, and only slightly expands near saturation. The AM-PM of a DPA with a conventional combiner (i.e., with $x = 0$) would result in a strong expansion after the auxiliary turn-on. By incorporating a reactive load of -j40 Ω (implemented as a 1.2 pF capacitance) in the quadrature combiner, the auxiliary presents a phase compression which compensates for the expansion observed in the red curve, resulting in a flat AM-PM profile. This adjustment improves the IMD3 response compared to the stand-alone class-AB PA, while maintaining similar efficiency levels.




(a) (b)

Fig. 4: Two-tone simulation of class-AB PA and quadrature-coupler-based DPA: (a) AM-PM and (b) gain, efficiency and |IMD3|.

Two identical stand-alone PAs are combined using an asymmetric (in favour of the main branch) input power splitter, implemented with a Wilkinson power divider on 50 Ω. This design choice is intended to enhance efficiency at lower power levels, which is a key target, while mitigating the gain loss typically observed in Doherty configurations.

To simplify the circuit and reduce the number of bias lines, the gate biases for the main and auxiliary amplifiers are derived from the same -5 V source. Surface-mount trimmers are added to each branch, providing tunability and allowing for precise adjustment of the bias levels to optimize performance. Fig. 5 shows the manufactured DPA.

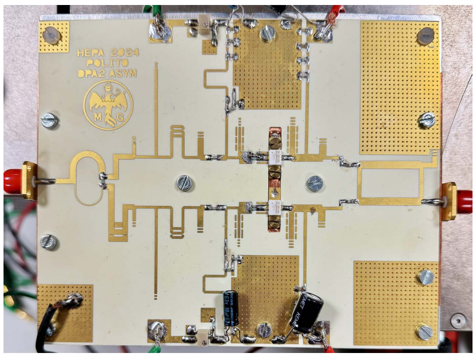


Fig. 5: Photograph of the manufactured DPA prototype.

## III. Characterization

The small signal characterization is performed over a (0.1–7) GHz frequency range at the nominal bias point: $V_{\mathrm{G,M}}$=-2.8 V, $V_{\mathrm{G,A}}$=-4.4 V, $V_{\mathrm{DD}}$=28 V, $I_{\mathrm{D}}$=42 mA.

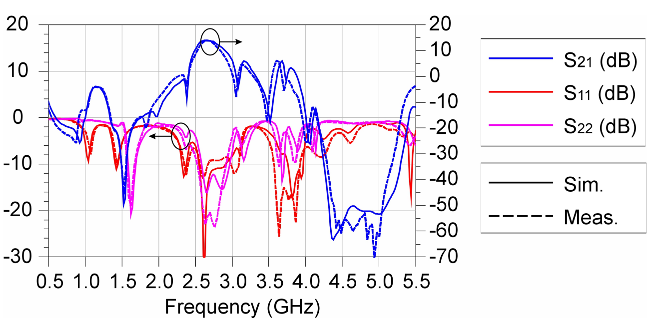



Fig. 6: Simulated (solid) and measured (dashed) S-parameters.

Fig. 6 shows the small-signal simulated and measured performance of the DPA. The $|S_{21}|$ is of the order of 14 dB, with $|S_{11}|$ and $|S_{22}|$ lower than -10 dB in a 200 MHz band around 2.7 GHz. It is observed that in measurement the peak of $S_{21}$ shifts toward higher frequencies by approximately 50 MHz. This shift is attributed to an earlier cutoff at lower frequencies, rather than a uniform frequency shift in performance. Consequently, the optimal performance frequency of 2.7 GHz is selected for further characterization. Overall the small-signal characteristics align well with the simulated results.

Fig. 7 compares the simulated large signal single-tone performance at 2.65 GHz with the measured one at 2.7 GHz. The results demonstrate a good overall agreement, with a small-signal gain of 13 dB, a saturated output power of 41 dBm, and a maximum PAE of 67%. However, a gain reduction of 1 dB and earlier onset of gain compression significantly reduce the margin to just 0.2 dB relative to the target output power of 36 dBm. In fact, at an input power of 24 dBm, the DPA achieves an output power of 36.2 dBm and a PAE of 46%.

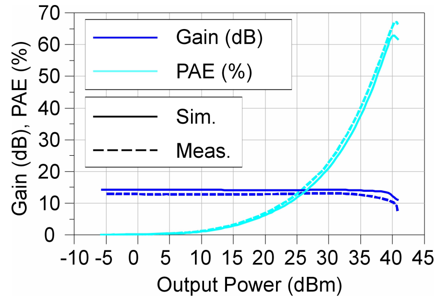
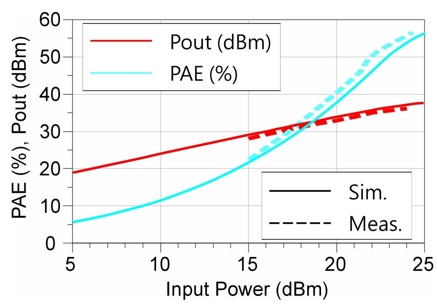


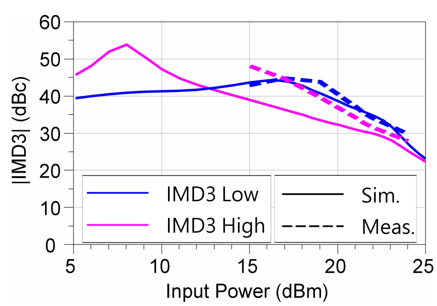

Fig. 7: Performance simulated in large-signal at 2.65 GHz (continuous) and CW characterized at 2.7 GHz (dashed).

To assess the linearity of the stage, a two-tone characterization with a 20 MHz tone spacing has been performed with an ESG Signal Generator, a driving pre-amplifier, a filter and an MXA Signal Analyzer, all from Keysight.

The optimization of the gate bias required to identify the IMD3 sweet spot is carried out by exploiting the trimmers embedded in the branches bias lines.




(a)




(b)

Fig. 8: Simulated (continuous line) and measured (dashed line) two-tone characterization at 2.65 GHz and 2.7 GHz respectively, with 20-MHz tone spacing: (a) output power and PAE and (b) |IMD3| versus input power.

Fig. 8 presents the comparison between simulated performance at 2.65 GHz and measured two-tone performance at

2.7 GHz: at the target input power of 24 dBm, the DPA exhibits IMD3 lower than -28 dBc, along with an output power in excess of 36.2 dBm and a PAE of 56%. The good agreement between measured and simulated linearity performance, particularly at the IMD3 -30 dBc crossover point, validates the design strategy.

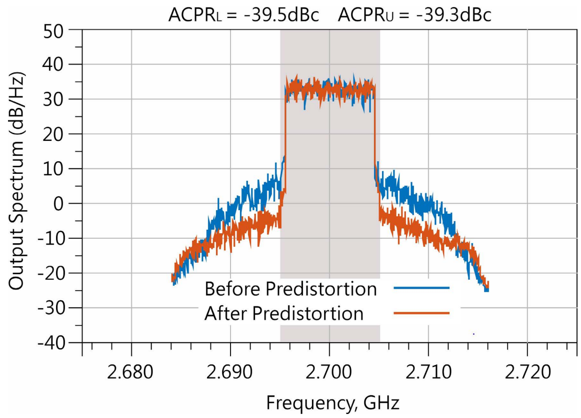



Fig. 9: Output power spectrum of a 64-QAM modulated LTE signal with 10-MHz bandwidth and 8-dB PAPR, at 2.7 GHz, before (blue) and after (red) DPD. Reported performance refers to the predistorted PA.

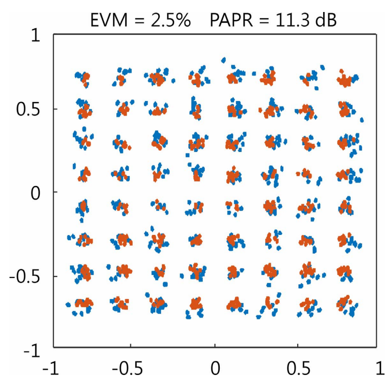



Fig. 10: Measured output constellation of a 64-QAM modulated LTE signal with 10-MHz bandwidth and 8-dB PAPR, at 2.7 GHz, before (blue) and after (red) DPD. Reported performance refers to the predistorted PA.

A system-level characterization is performed at 2.7 GHz with a 64-QAM modulated LTE signal with 10-MHz bandwidth and 8-dB PAPR. Fig. 9 and 10 show respectively the output power spectrum and the constellations before and after DPD. Before DPD, at an average output power of 33 dB and 35% efficiency, the circuit exhibits an ACPR of -31 dBc and an EVM of 4%, confirming the validity of the approach based on the minimization of one-tone AM-PM and two-tone IMD3. After applying direct DPD with a maximum limit of 5 iterations, the performance further improves to ACPR of -39 dBc and EVM of 2.5%.

## IV. Conclusion

This paper has presented the design and characterization of an efficient and linear hybrid Doherty power amplifier for S-band wireless communication applications. At 2.7 GHz and 36 dBm output power, the design achieves simultaneously -30 dBc of IMD3 and PAE higher than 45%. A complete characterization has been presented, including small and large signal measurements. System level characterization is performed both with two-tone and modulated input signals, which allows to prove the validity of the design approach and the consistency of the results under different stimuli.

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