A Novel Bypass Architecture for RB-COT Buck Converters

This article has been accepted for publication in IEEE Transactions on Circuits and Systems II: Express Briefs. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2025.3555695

A Novel Bypass Architecture for RB-COT Buck Converters

Francesco Gabriele, *Graduate Student Member, IEEE*, Samuele Gisonno, Filippo Fiori, Davide Lena, Salvatore Rosario Musumeci, Fabio Pareschi, *Senior Member, IEEE*, Gianluca Setti, *Fellow, IEEE*

***Abstract*—In this brief we propose a novel ByPass (BP) circuit that overcomes the voltage regulation limit in the Ripple Based Constant On-Time (RB-COT) Buck converters due to intrinsic presence of a minimum achievable OFF time. The BP stage is conceived to be embedded in the RB-COT modulator located within the converter feedback loop, and only intervening when the minimum OFF time condition is reached. The latter implies that the COT modulator saturates, and consequently, the output voltage regulation of the converter is no longer guaranteed. Conversely, the BP stage does not affect the behavior of the circuit when it operates in normal regulating condition. The effectiveness of the proposed BP stage is confirmed through both transistor-level simulation results derived from the SPICE platform and experimental measurements on a integrated circuit prototype implemented in a 0.18 um Bipolar-CMOS-DMOS process.**

***Index Terms*—DC-DC converter, Buck converter, COT control, minimum OFF Time, Adaptive COT, Bypass Mode.**

I. Introduction

In the field point-of-load voltage regulator, the DC-DC Buck converter topology is extensively used to step-down the high-voltage of an intermediate bus to feed several system components (e.g., ASICs, µC, DSPs, etc.) operating in a low-voltage domain. The Buck converter must feature high efficiency level, maintaining an accurate output voltage despite variations in the external operating conditions. To meet these tight performance requirements, the Ripple-Based Constant On-Time (RB-COT) control has become increasingly attractive by virtue of its architectural simplicity, improved dynamic performances and enhanced efficiency at light-loads [1], [2].

Nevertheless, a notable limitation of the RB-COT control architecture is the lack of a well-defined switching frequency [1]. By fixing a-priori the on-time $T_{\rm ON}$ in the Pulse-Width Modulated (PWM) control signal $\texttt{PWM}(t)$, and changing the off-time $T_{\rm OFF}$ by means of the COT modulator according to the target output voltage level $V_{\rm out}^{\rm target}$, the switching period $T_{\rm sw} = T_{\rm ON}+T_{\rm OFF}$ is unknown. To cope with this, an Adaptive Constant On-Time (ACOT) timer is typically introduced in the COT modulator stage, as in Fig. 1(a) [3]–[6]. Referring to the RB-COT operation in Continuous Conduction Mode (CCM) depicted in Fig. 1(b), the $T_{\rm ON}$ is stretched or tightened depending on the converter operating condition (e.g., the DC input and output voltage levels, respectively $V_{\rm in}$ and $V_{\rm out}$, and the output current load $I_{\rm out}$), aiming a quasi-constant $T_{\rm sw}$.

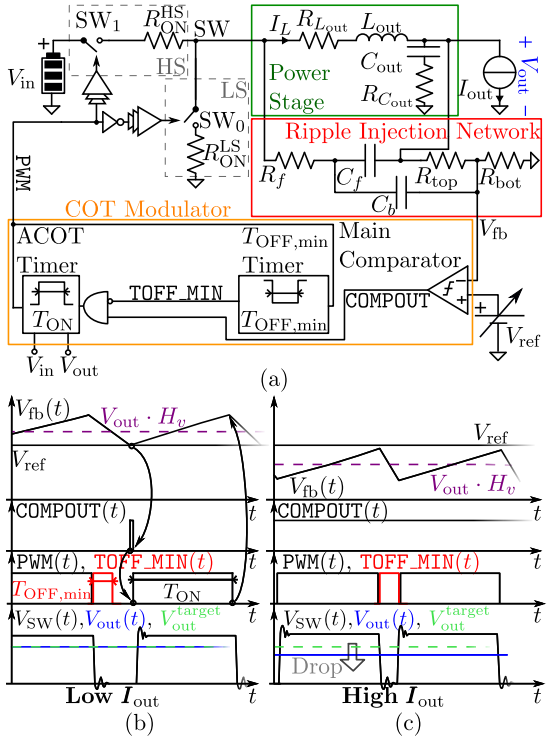

Fig. 1. (a) The examined RB-COT Buck converter; (b) the normal operation of the converter at high-duty and light loads; (c) the voltage regulation limit at high-duty and heavy loads.

In practical cases, when the Buck converter operates with high Conversion Ratio (CR), i.e., when the $V_{\rm out}$ is close to $V_{\rm in}$ either due to a $V_{\rm in}$ reduction due to a battery discharge or an increase of the $V_{\rm out}^{\rm target}$ level, the COT modulator may enter a saturation region. A minimum OFF time $T_{\rm OFF,min}$, in fact, always exists [2], [7], [8], so that the duty-cycle D_c of $\texttt{PWM}(t)$ saturates to a fixed value and it cannot increase further. This problem is shown Fig. 1(c), where a $T_{\rm OFF,min}$ timer after the end of a $T_{\rm ON}$ is enforced. Note that, when a saturation condition occurs, the more the $I_{\rm out}$ increases, the more the $V_{\rm out}$ deviates from $V_{\rm out}^{\rm target}$ since the losses in the converter (e.g., the ohmic voltage drops due to the presence of the ON resistances of the power MOSFETs $R_{\rm ON}^{\rm HS,LS}$ and the winding resistance $R_{L_{\rm out}}$) increase. These cannot be compensated anymore by adjusting the D_c, as it is fixed to its saturation level. In consequence, the converter accuracy degrades, severely compromising the correct behavior of the

F. Gabriele and F. Pareschi are with the Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Torino, Italy (e-mail: {francesco.gabriele, fabio.pareschi}@polito.it).

S. Gisonno, F. Fiori, D. Lena and S. R. Musumeci are with STMicroelectronics s.r.l. – Torino, Italy. (email: {samuele.gisonno, filippo.fiori, davide.lena, salvo.musumeci}@st.com).

G. Setti is with CEMSE, King Abdullah University of Science and Technology (KAUST), Saudi Arabia (e-mail: gianluca.setti@kaust.edu.sa).

This article has been accepted for publication in IEEE Transactions on Circuits and Systems II: Express Briefs. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2025.3555695

cascaded powered systems.

To overcome this issue, a ByPass (BP) operating mode is typically implemented in RB-COT designs [9]–[11]. In most cases, it consists in bypassing the converter by turning ON an auxiliary power MOSFET when the V_{in} and V_{out} levels are a pre-defined voltage threshold apart. Nevertheless, this implies the introduction of an additional power switch, along with its controller and driver stages. The literature proposes several Buck converter control architectures that permit to extend the duty-cycle range, such as [12]–[15]. Nevertheless, a D_c upper bound always exists, consequently restricting the achievable V_{out} values to be significantly lower V_{in}.

In this work, we propose a novel and smart BP circuit stage that does not require any auxiliary power MOSFET. Referring to Fig. 1(a), it can be embedded in the COT modulator and exclusively activates when a persistent saturation condition is detected together with a V_{out} drop. The proposed BP stage thus seamlessly activates, acting on the PWM signal and resorting on the available High-Side (HS) MOSFET. This ensures an accurate V_{out} level.

The paper is organized as follows. In Sec. II, we briefly describe the RB-COT architecture of Fig. 1(a), detailing the regulation limit issue for both the COT and ACOT architectures and highlighting differences. In Sec. III, we describe the BP stage architecture, detailing its working principle. In Sec. IV the validation of the proposed circuit is performed at system-level, demonstrating its effectiveness through both transistor-level circuit simulations performed in and experimental measurements. Finally, we draw the conclusion.

II. RB-COT Converter Architectural Description and the Voltage Regulation Limits

The RB-COT Buck converter architecture we refer is shown in Fig. 1(a) and it is widely adopted in both portable devices and power management applications. It includes the HS and Low-Side (LS) MOSFETs, modeled with the switches pair $\text{SW}_{0,1}$ and the $R_{\text{ON}}^{\text{HS,LS}}$, followed by the Power Stage (PS). The latter includes the power inductor L_{out}, the output capacitor C_{out} and their series parasitic resistances, respectively $R_{L_{\text{out}}}$ and $R_{C_{\text{out}}}$. The output load is a constant DC current I_{out}.

The Ripple Injection Network (RIN) we consider is widely employed in various commercial products [16]–[18]. From a high-level perspective, this circuit synthesizes an artificial ripple signal V_{fb} that is in phase with the inductor current I_L. The components R_f and C_f reconstruct the I_L shape, generating a signal that is AC-coupled via the capacitor C_b and fed back to the FB node. The bias of V_{fb} is set from the V_{out} through the resistor divider consisting of R_{top} and R_{bot}. Finally, the RB-COT modulator stage includes the Main Comparator (MC), the ACOT timer and the $T_{\text{OFF,min}}$ timer.

As shown by the steady-state waveforms in Fig. 1(b), V_{fb} is compared against an externally programmable voltage reference V_{ref} that set the $V_{\text{out}}^{\text{target}}$ value. Whenever V_{fb} intercepts V_{ref}, the output of the MC rises. This triggers a new ON pulse through the ACOT timer. When it ends, the $T_{\text{OFF,min}}$ timer inhibits the beginning of a new T_{ON} for a $T_{\text{OFF,min}}$ time interval. The T_{OFF} is consequently adjusted by the RB-COT feedback loop to regulate the $V_{\text{out}}^{\text{target}} = V_{\text{ref}}/H_v$, where

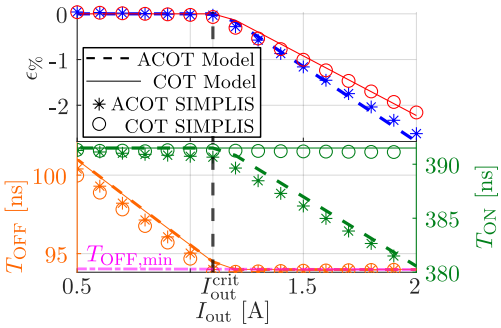

Fig. 2. Voltage regulation limit of COT and ACOT Buck converter: SIMPLIS vs the mathematical models given in III. The value $\epsilon_{\%}$ is the percentage relative error between V_{out} and $V_{\text{out}}^{\text{target}}$, i.e., $\epsilon_{\%} = \left(V_{\text{out}} - V_{\text{out}}^{\text{target}}\right)/V_{\text{out}}^{\text{target}} \cdot 100$.

$H_v = R_{\text{bot}}/\left(R_{\text{bot}} + R_{\text{top}}\right)$. For instance, it progressively reduces either when the actual V_{out} level approaches V_{in} (e.g., either due to a V_{in} drop or a $V_{\text{out}}^{\text{target}}$ increase) or the I_{out} increases (e.g., due to the increase of the converter ohmic voltage drop on $R_{\text{ON}}^{\text{HS,LS}}$ and $R_{L_{\text{out}}}$). Therefore, the RB-COT feedback loop keeps regulating the converter output voltage provided that $T_{\text{OFF}} > T_{\text{OFF,min}}$. Conversely, the RB-COT converter starts sub-regulating (i.e., it provides a $V_{\text{out}} < V_{\text{out}}^{\text{target}}$), as shown in Fig. 1(c).

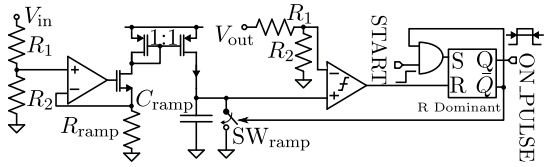

Fig. 3. Circuit implementation of the ACOT Timer stage shown in Fig. 1(a).

In order to analytically formulate the voltage regulation limit of the converter in Fig. 1(a) operating under COT control, we resort to the principle of *inductor volt-second balance* under the *small-ripple* assumption [19]. It results in

$$V_{\text{out}} = V_{\text{in}} D_c - \left(\frac{R_{\text{ON}}^{\text{HS}} T_{\text{ON}} + R_{\text{ON}}^{\text{LS}} T_{\text{OFF}}}{T_{\text{OFF}} + T_{\text{ON}}} + R_{L_{out}} \right) I_{\text{out}}, \tag{1}$$

where $D_c = T_{\text{ON}}/(T_{\text{ON}} + T_{\text{OFF}})$. When $T_{\text{OFF}} > T_{\text{OFF,min}}$ this equation predicts the T_{OFF} variation as a function of the I_{out} value as the converter feedback loop guarantees $V_{\text{out}} = V_{\text{out}}^{\text{target}}$. On the contrary, when the T_{OFF} saturates at $T_{\text{OFF,min}}$, it captures the V_{out} reduction as I_{out} increases.

Regarding the voltage regulation limit under ACOT control, we will refer to the ACOT timer architecture shown in Fig. 3. It generates an ON pulse with duration $T_{\text{ON}} = k_T \cdot V_{\text{out}}/V_{\text{in}}$, where $k_T = R_{\text{ramp}} C_{\text{ramp}}$. Since in CCM $V_{\text{out}}/V_{\text{in}} = T_{\text{ON}}/T_{\text{sw}} = D_c$, this results in $T_{\text{sw}} = k_T$. An analytical expression for the ACOT voltage regulation limit is derived by substituting the T_{ON} in (1) and solving for V_{out}.

Considering the component values listed in Table I, the COT and ACOT voltage regulation limits are both shown in Fig. 2. A threshold value $I_{\text{out}}^{\text{crit}}$ marks the emergence of the voltage regulation issue. It can be derived by imposing $V_{\text{out}} = V_{\text{out}}^{\text{target}}$ and $T_{\text{OFF}} = T_{\text{OFF,min}}$ in the analytical expressions derived

This article has been accepted for publication in IEEE Transactions on Circuits and Systems II: Express Briefs. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2025.3555695

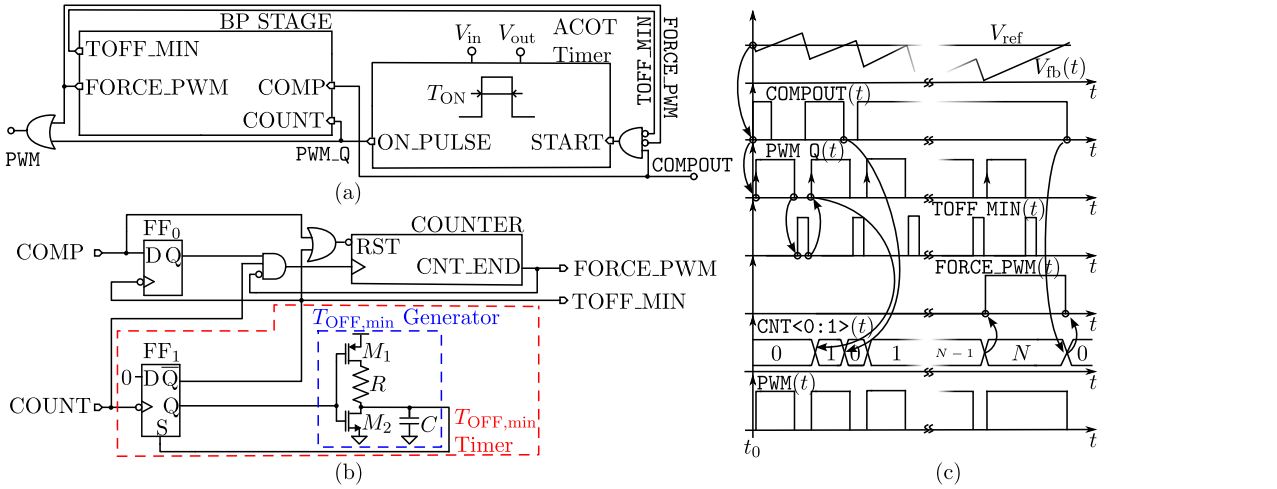

Fig. 4. (a) The BP stage embedded in the COT modulator of the RB-COT Buck converter shown in Fig.1(a); (b) a detailed view of the BP stage architecture; (c) the set of waveforms highlighting the BP stage working principle.

TABLE I
NOMINAL COMPONENT VALUES OF THE BUCK CONVERTERS CONSIDERED IN THIS PAPER.

$R_{ON}^{HS,LS}$ [mΩ]	$R_{C_{out}}$ [mΩ]	$R_{L_{out}}$ [mΩ]	$T_{OFF,min}$ [ns]	k_T [ns] (ACOT *only*)	T_{ON} [ns] (COT *only*)	L_{out} [µH]	C_{out} [µF]	R_f [kΩ]	C_f [pF]	C_b [pF]	R_{top} [MΩ]	R_{bot} [kΩ]	V_{ref} [mV]
50	2	45	94	500	390	1	44	300	100	2.5	2.375	625	580-875

above. Compared to COT control, the behavior of the converter with ACOT control is unchanged when $I_{out} < I_{out}^{crit}$. On the contrary, when $I_{out} > I_{out}^{crit}$, the T_{ON} value progressively reduces as the I_{out} increases, leading to a V_{out} reduction at a faster rate. SIMPLIS simulations confirm these results.

III. Architectural and Behavioral Analysis of the BP Stage

Overall, in both the COT and ACOT cases, the results shown in Fig. 2 highlight a non-negligible voltage regulation issue. The latter becomes increasingly impactful as the I_{out} increases and for high-D_c values. In order to address this issue, we propose an additional BP stage architecture. The latter is embedded in the COT modulator of the RB-COT converter of Fig. 1(a) as shown in Fig. 4(a). It monitors the COT feedback loop signals and solely intervenes when an output voltage drop condition is detected. The BP stage does not interfere with the feedback loop in normal operating condition, i.e., in the scenario of Fig. 1(b).

The internal architecture of the proposed BP stage block is shown in Figure 4(b). It incorporates the $T_{OFF,min}$ Timer, that is the circuit responsible for the generation of the minimum OFF time window $T_{OFF,min}$. The timer operates as follows. When the ON pulse ends, the flip-flop FF_1 propagates the logic '0' on its input pin D towards the output Q, turning ON the MOSFET M_1, here operating as a switch. This triggers the charging phase of the capacitor C via the resistance R. During this phase, the TOFF_MIN signal is asserted. It lasts until the voltage drop on C is approximately equal to half the logic supply voltage, since at that instant the FF_1 is set via the pin S. This leads to turn ON the MOSFET M_2, instantaneously discharging the C. According to this procedure, the minimum OFF time duration is equal to $T_{OFF,min} = \ln 2 \cdot RC$. The latter is straightforwardly derived from the capacitor voltage equation in a simple RC circuit by imposing that the C is initially uncharged and the voltage drop on C after a $T_{OFF,min}$ interval is half the logic voltage supply.

The behavior of the BP stage and its interaction with the RB-COT feedback loop is sketched in Fig. 4(c). Let's assume that the bypass mode is not active at $t = t_0$. When V_{fb} falls below V_{ref}, the COMPOUT signal becomes high. In turn, the latter asserts the PWM_Q, causing the V_{fb} to increase. As soon as the PWM_Q falling edge takes place, i.e., when the T_{ON} pulse ends, the $T_{OFF,min}$ interval starts and the signal TOFF_MIN is asserted. When it become deasserted, the state of the COMPOUT is sampled by the FF_0. In this case, since the feedback signal V_{fb} lies below V_{ref} at the end of $T_{OFF,min}$, COMPOUT is in the high state. This causes an increase of the COUNTER stage as soon as the PWM_Q signal is engaged by the ACOT timer. On the contrary, the COUNTER is reset any time the COMPOUT signal is deasserted outside a $T_{OFF,min}$ window, as occurs in the next cycle. Instead, whenever the counter increments N times, it reaches the end of the count and asserts the FORCE_PWM signal. This triggers a bypass intervention, asserting the PWM signal and consequently turning the HS MOSFET on. In the bypass mode, the activity of the ACOT Timer is thus inhibited, meaning that the signal COMPOUT cannot be asserted. The bypass mode lasts until the first time the signal COMPOUT is deasserted outside a $T_{OFF,min}$ interval. In this scenario, the counter is reset terminating the bypass mode. The selection of N involves

This article has been accepted for publication in IEEE Transactions on Circuits and Systems II: Express Briefs. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2025.3555695

a trade-off between the converter output ripple increase and the susceptibility of the COT modulator to switching noise. Indeed, although a small N minimizes the increase of the output voltage ripple when the BP stage intervenes, it may lead to spurious and irregular interventions of the BP stage due to the presence of switching noise. This consequently results in an uncontrolled behavior of the RB-COT converter.

IV. Validation Of The Proposed BP Circuit

The BP stage effectiveness has been validated by means of both transistor-level simulations and experimental measurements. In the following, we will consider the set of circuital parameters listed in Table I.

A. Transistor-Level Simulation Results

When the BP stage is disabled the achieved output voltage level V_{out} is smaller than $V_{\text{out}}^{\text{target}}$, as shown in Fig. 5(a). Indeed, as inferable from the V_{SW} waveform, the T_{OFF} saturates to $T_{\text{OFF,min}}$ and the externally imposed I_{out} lead to an output voltage drop, as further confirmed by Fig. 2. When the BP stage is enabled, the output voltage regulation is recovered and a well-regulated $V_{\text{out}} = V_{\text{out}}^{\text{target}}$ is achieved. Owing to the BP intervention, the length of ON pulses periodically increases in order to keep the V_{out} close to $V_{\text{out}}^{\text{target}}$.

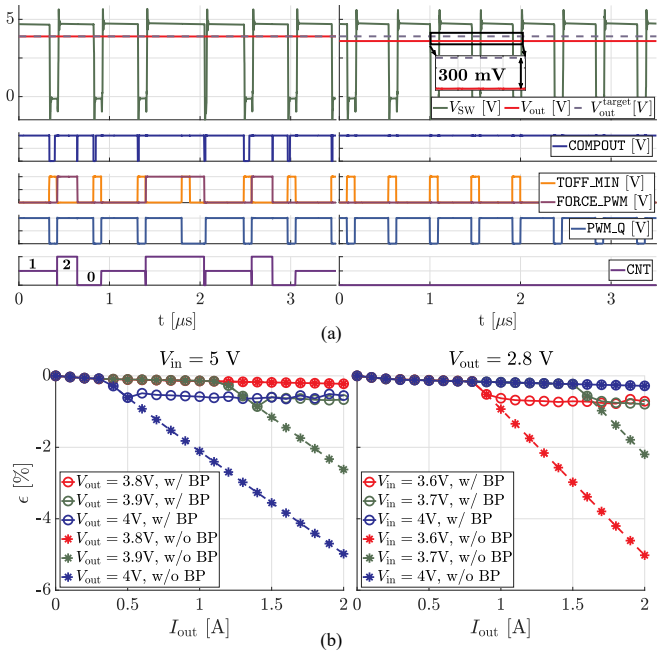

Fig. 5. (a) Transistor-level simulation of the RB-COT converter with $V_{\text{in}} = 5\,\text{V}$, $V_{\text{out}} = 3.9\,\text{V}$ and $I_{\text{out}} = 2\,\text{A}$, with BP stage enabled with $N = 2$ (left), and BP stage disabled (right). (a) Simulated accuracy of the RB-COT converter at different V_{in} and V_{out} with BP stage enabled and disabled. ϵ is defined as in Fig. 2.

The accuracy of the RB-COT converter embedding the BP stage is characterized in Fig. 5(b) for a set of I_{out}, V_{in} and V_{out} values. Similarly to Fig. 2, the converter output voltage starts derating when a I_{out} threshold value is reached. When the BP stage is enabled, it intervenes in order to achieve $V_{\text{out}} \approx V_{\text{out}}^{\text{target}}$. The maximum output voltage error is -0.8%.

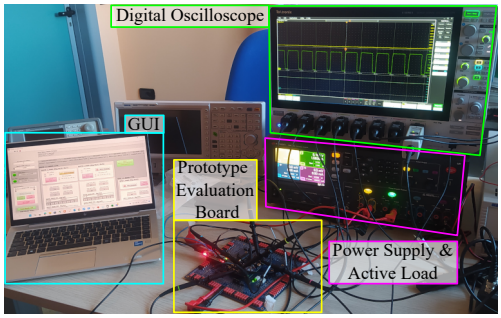

Fig. 6. The experimental setup includes the DC-DC converter with featuring the presented BP stage, the Power Supply and the Active Load Keysight N6705C. Results are collected through the Digital Oscilloscope Tektronix MSO58B. The custom GUI allows to set up main circuit parameters.

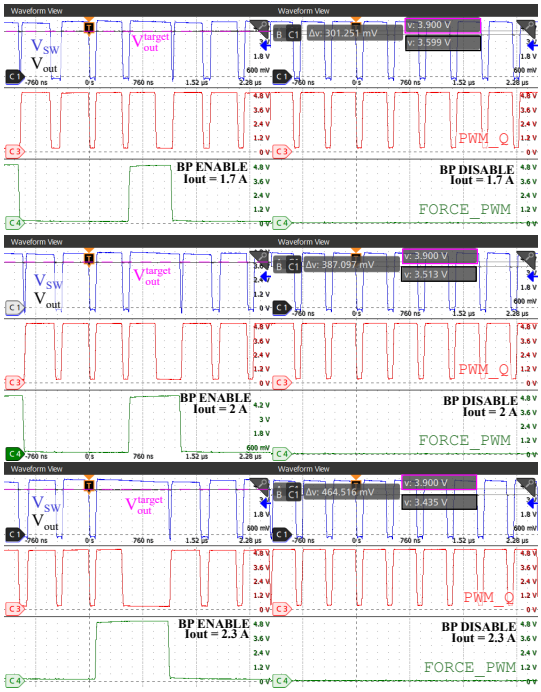

Fig. 7. Experimental validation at $V_{\text{in}} = 5\,\text{V}$, $V_{\text{out}} = 3.9\,\text{V}$, different I_{out} and $N = 2$.

B. Experimental Measurements

The test bench used for validation is shown in Fig. 6. A prototype Integrated Circuit (IC) of the RB-COT converter, implemented in a $0.18\,\mu\text{m}$ BCD process, has been tested at different V_{in}, V_{out} and I_{out}. Results are shown in Fig. 7, confirming the effectiveness of the BP stage when the COT modulator saturates. The BP stage also contributes to improve the converter load-transient response, as depicted in Fig. 8. Under heavy load-step, it intervenes in the transient recovery time stretching the ON pulse duration. The RB-COT converter efficiency is measured at different V_{in} and V_{out} values, as shown in Fig. 9. The converter achieves a peak efficiency of 96%. The CR reaches 1 at no load, while it settles to 0.92 at full-load guaranteeing stability. A summary of RB-COT converter performances and its electrical characteristics is provided in Table II, with a state-of-the-art comparison.

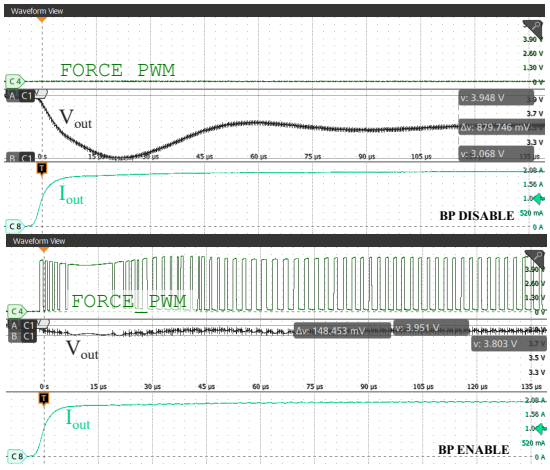

Fig. 8. Load transient response of the RB-COT converter in Fig. 1(a). Top: BP stage disabled. Bottom: BP stage enabled with $N = 2$.

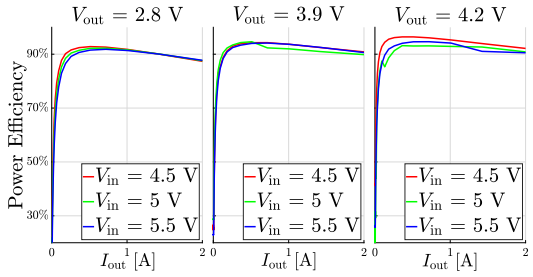

Fig. 9. Measured power efficiency of the proposed RB-COT converter.

V. Conclusion

A novel BP stage to be embedded in the feedback loop of RB-COT Buck converters is proposed. This solution addresses the voltage regulation limits arising when the converter operates at minimum OFF time. Here, the COT modulator saturates, and the output voltage regulation is lost. Simple algebraic equations are presented to theoretically validate the voltage regulation issue for both COT and ACOT controlled Buck converters operating in CCM. The effectiveness in recovering the output voltage regulation via the proposed BP stage has been demonstrated through both transistor-level simulation results and experimental results derived from an IC prototype.

TABLE II
Main Performances Summary and Comparison.

	[12]	[13]	[14]	**This work**
Technology	0.18 µm BCD	0.18 µm CMOS	0.18 µm CMOS	**0.18 µm BCD**
V_{in} Range [V]	5-36	3.3	2.2-5	**2.8-5.5**
V_{out} Range [V]	1-34	0.2-3	1.8	**2.8-4.2**
Max. I_{out} [A]	0.9	1	0.1	**2.3**
F_{sw} [MHz]	2.2	10-30	1.7	**2**
L_{out} [µH]	10	0.22	4.7	**1**
C_{out} [µF]	22	1	1	**44**
Max. Efficiency [%]	92	90.6	94	**96**
Load Step [A]	0.59	0.3	0.0219	**2**
Undershoot [mV]	42	50	28	**148**

References

[1] R. Redl and J. Sun, "Ripple-Based Control of Switching Regulators—An Overview," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2669–2680, 2009. doi: 10.1109/TPEL.2009.2032657

[2] M. Gobbi and A. Mariani, "Low drop-out cot buck converter without maximum duty cycle limitation due to minimum off-time," in *2020 AEIT International Annual Conference (AEIT)*, 2020, pp. 1–6. doi: 10.23919/AEIT50178.2020.9241198

[3] C.-H. Tsai, B.-M. Chen, and H.-L. Li, "Switching Frequency Stabilization Techniques for Adaptive On-Time Controlled Buck Converter With Adaptive Voltage Positioning Mechanism," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 443–451, 2016. doi: 10.1109/TPEL.2015.2405339

[4] L. Wong and T. Man, "Adaptive On-Time Converters," *IEEE Industrial Electronics Magazine*, vol. 4, no. 3, pp. 28–35, 2010. doi: 10.1109/MIE.2010.937931

[5] R. Redl and N. O. Sokal, "Frequency stabilization and synchronization of free-running current-mode-controlled converters," in *1986 17th Annual IEEE Power Electronics Specialists Conference*, 1986, pp. 519–530. doi: 10.1109/PESC.1986.7415603

[6] "Adaptive Constant On-Time (D-CAP™) Control Study in Notebook Applications," Texas Instrument, 2007, revised December 2007. [Online]. Available: https://www.ti.com/lit/an/slva281b/slva281b.pdf

[7] F. Bizzarri, P. Nora, and A. Brambilla, "Closed-Form Operational Boundaries for Buck Converters With Constant On-Time Control," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 10, pp. 3331–3335, 2021. doi: 10.1109/TCSII.2021.3068900

[8] "Buck Regulator 3 A, Constant On Time (COT), FAN53730," Semiconductor Components Industries, LLC, 2023, may, 2024 - Rev. 2. [Online]. Available: https://www.onsemi.com/download/data-sheet/pdf/fan53730-d.pdf

[9] G. D. Michele De Fazio, "Bypass Control in a DC-to-DC Converter," Patent US2013/0 193 941A1, Aug. 1, 2013. [Online]. Available: https://patents.google.com/patent/US20130193941A1/en

[10] "FAN5903 Buck Converter with Bypass Mode for 3G/3.5G/4G PAs,"Fairchild Semiconductor Corporation, 2008, rev. 1.0.9. [Online]. Available: https://www.onsemi.com/download/data-sheet/pdf/fan5903-d.pdf

[11] "Buck Converter with Bypass Mode for RF Power Amplifiers,"Semiconductor Components Industries, LLC, 2014, rev. 5. [Online]. Available: https://www.onsemi.com/download/data-sheet/pdf/ncp6361-d.pdf

[12] Z. Zhao, P. Luo, Z. Zhang, J. Fan, B. Zhang, and X. Chen, "A Peak-Valley Current-Mode Buck Converter With 3% to 95% Duty Cycle," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 72, no. 1, pp. 328–332, 2025. doi: 10.1109/TCSII.2024.3484449

[13] L. Yi, S. Yu, C. Tang, and X. Tang, "A 10-30 MHz Voltage-Mode Buck Converter With Linear Comparator-Free V2D controller," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 7, pp. 3278–3282, 2024. doi: 10.1109/TCSII.2024.3362252

[14] W. Park, G. Namgoong, E. Choi, B. Lee, H. Park, H. Ma, and F. Bien, "A 94% peak efficiency dual mode buck converter with fully integrated on-time-based mode control for implantable medical devices," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 11, pp. 4458–4462, 2022. doi: 10.1109/TCSII.2022.3194154

[15] Q. Huang, C. Zhan, and J. Burm, "A 30-MHz Voltage-Mode Buck Converter Using Delay-Line-Based PWM Control," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 11, pp. 1659–1663, 2018. doi: 10.1109/TCSII.2017.2764048

[16] "Selecting an Ideal Ripple Generation Network for Your COT Buck Converter," Texas Instrument, 2017, rev. A. [Online]. Available: https://www.ti.com/lit/an/snva776a/snva776a.pdf

[17] M. Lin, T. Zaitsu, T. Sato, and T. Nabeshima, "Frequency domain analysis of fixed on-time with bottom detection control for buck converter," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 481–485. doi: 10.1109/IECON.2010.5674981

[18] "LM5166 3 V to 65 V Input, 500 mA Synchronous Buck Converter With Ultra-Low IQ," Texas Instrument, 2016, revised December 2017. [Online]. Available: https://www.ti.com/lit/ds/symlink/lm5166.pdf

[19] D. M. Robert W. Erickson, *Fundamentals of Power Electronics*. Springer Cham, 16 August 2020.