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Physics-based Modelling for Stacked Power Amplifier design at Millimetre-Wave Frequency (*Invited*)

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***Abstract*—Physics-based TCAD simulations are the most accurate modelling approach for mm-wave power amplifier design, allowing extracting reliable device models, retaining the link to process parameters and including parasitic elements. We show, for the first time, the multi-harmonic physical TCAD simulations of a 10 dBm stacked power amplifier at 70 GHz in 22 nm FinFET technology. The stacked architecture is particularly challenging for TCAD analysis as it includes common gate stages acting as active loads. TCAD simulations can be then imported in CAD tools for circuit design through behavioral models, which, thanks to the physics-based approach, can be made dependent on specific technological or physical parameters, e.g. temperature.**

***Index Terms*—TCAD, device modeling, FinFET, stacked power amplifier**

I. INTRODUCTION

Device model reliability is the key for a successful design at microwave and millimeter-wave frequencies, where parasitic effects and process-induced variability play a crucial role in determining circuit performance. In particular, power amplifier design is one of the most demanding cases, requiring for large-signal models capable to accurately reproduce the non-linear behavior of the device in mild-to-deep compression.

Compared to compact circuit models, physics-based models obtained from Technology CAD (TCAD) simulations offer incomparably higher accuracy as well as a direct link to individual technological and physical parameters allowing for accurate and efficient statistical and thermal PA analyses [1,2]. Translation from TCAD environment to classical RF EDA tools can be easily done by means of the X-parameters [3] format obtaining a behavioral model that preserves all the large-signal information necessary for PA design [4, 5].

In this work we demonstrate how the TCAD approach can be profitably exploited for the design of a 70 GHz stacked-FET power amplifier in a 22 nm FinFET technology. The stacked PA is a very promising solution for power boosting of low-breakdown technologies at mm-wave frequencies [6, 7], but at the same time it is also a challenging example from the device modelling standpoint as it must use the device in pseudo-common gate configuration. The accuracy of the proposed TCAD simulations, based on a in-house developed code, for the common gate stage have been discussed in [8], adopting a simpler MESFET technology. While in [8] only single device simulations were considered, in this work we address how to exploit TCAD to simulate a full 2-FET stacked structure in an accurate way.

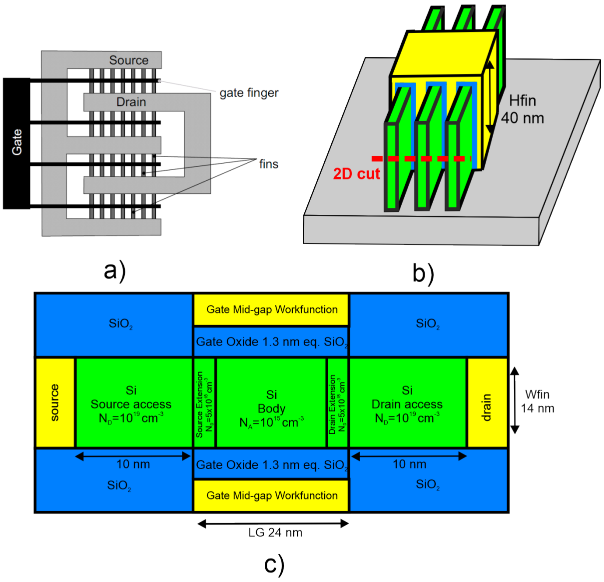

Fig. 1: 22 nm FinFET technology. a) Multi-finger parallel-fin layout, b) 3D view and c) 2D cut of the individual fin exploited for the TCAD analysis.

II. FINFET TECHNOLOGY

The growing interest in the mm-wave spectrum for telecommunications system (6G and beyond) is pushing technology suppliers to develop active devices capable of providing useful power densities at increasingly higher frequency. Both Si-based nanotechnologies and III-V-based (GaAs and GaN) ones are suited for mm-wave power amplifier (PA) design, depending on the specific application requirements. Even if GaN power density is incomparably higher than that of other technologies, its application to mm-waves is still mainly limited to sub-50 GHz range [9, 10], while GaAs dominates at higher frequencies [11, 12]. On the other hand, the use of large arrays, allowing for smaller individual-PA output power is opening the mm-wave market also to CMOS technologies. Among them, FinFETs have the wider success, thanks to their better scaling capabilities and immunity to short channel effects. FinFET PAs have been demonstrated at V- and W-band, providing up to 18 dBm of output power [13-16].

Individual FinFET cells used in PAs are characterized by a multi-finger layout with multiple paralleled fins, as shown in Fig. 1 (a-b). Due to the complexity of such a 3D structure, accurate non-linear models including technological spread and thermal effects are required [1, 2, 4]. Although TCAD simulations of 3D structures with multiple fins have been demonstrated [17], a complete TCAD simulation of the overall cell would be too numerically intensive, even if limited to the DC and small-signal AC analyses amenable in commercial simulators [18]. A mixed mode approach, where the intrinsic active device is coupled at the electrical level to other devices or to passive combining structures and/or to a thermal circuit, is more suitable for the simulation of a PA cell. To extract the device behavior in the actual operating conditions of PA circuits, we exploit the Harmonic Balance (HB) analysis: a unique technique that allows to simulate a semiconductor device with multiple external harmonic stimuli and harmonic loads. However, HB TCAD is even more numerically intensive than DC and AC analyses, since it must include multiple harmonics for each physical variable, therefore the mixed-mode analysis is even more required.

For the TCAD analysis of the stacked circuit, we exploit the in-house Harmonic Balance simulator, whose mixed-mode capability offers the necessary flexibility in defining independent transistor terminal and in creating multi-device structures [19, 20]. Despite, being currently limited to 2D analysis, successful application of this simulator to FinFET technology modelling have been presented in [1, 21] including thermal behavior and process variability.

In this work, we adopt a 22 nm FinFET technology, taking as reference geometry, doping and material properties the FinFET template available from the Synopsys distribution [18]. The details of the simulated structure (the 2D FinFET cross section and the physical parameters) are reported in Fig. 1 (c). Although more extrinsic regions could be added to the simulations, in this preliminary work the access source and drain regions are limited to the intrinsic device, to reduce the simulation burden. With this approach, most of the device parasitic resistances are correctly taken into account, while drain-gate and drain-source capacitances and lead inductances are underestimated. Reactive parasitics, though, are usually linear and can be easily added at circuit level. All the silicon material parameters (e.g. mobility, velocity saturation, temperature dependency etc.) of the in-house TCAD has been previously calibrated with Synopsys TCAD [1].

III. STACKED PA TCAD SIMULATIONS

A stacked power amplifier is composed of two or more devices AC and DC coupled in series [23], as shown in Fig. 2. The number of transistor that can be adopted is limited by the cut-off frequency, being the common gate stages acting as current followers [24, 25]. With respect to the more classical parallel combination, it shows several features: 1) increased output voltage swing, overcoming the breakdown limit of the single transistor, 2) gain boosting, 3) smaller footprint hence higher power density and 4) larger optimum load impedance. The first feature explains the wide use of such topology in low-breakdown technologies [6, 7], but the other ones make it a very interesting solution also for GaAs and GaN PAs [11, 26-28] given the typically low optimum impedance and MAG they show at mm-wave frequencies. Favorable impedance matching ratio in turns allows for wider bandwidth, provided that wideband stacking is feasible. In fact, at frequencies where the output parasitic reactance needs to be compensated, reactive inter-stage matching networks are required, where often a higher quality factor is accepted in exchange for network compactness and simplicity [26, 28].

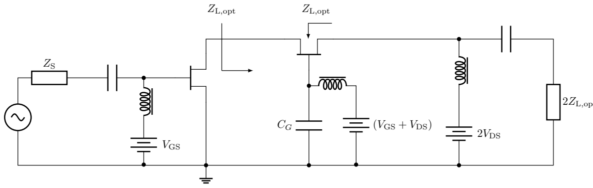

Fig. 2: Simulated stacked PA schematic. A classical common source (CS) stage is loaded by a pseudo-common gate (CG) transistor featuring a finite gate capacitance value at the operating frequency. The gate-source voltages are adjusted to accommodate for the same drain current in both stages, while the supply voltage is doubled with respect to a basic PA. If C_{G} is properly sized, both FETs provide maximum output power.

Stacked PA design requires non-linear device models with three terminals, not always available as compact models, capable of accurately reproduce the transistor behavior also in the pseudo-common gate configuration. Being compact models typically optimized for common source usage, the latter point highlights the advantage of resorting to a physics-based model. Moreover, the high power density achievable with a stacked solution also has the drawback of increasing the operating temperature of the stacked transistor with respect to parallelized ones [28], thus requiring also an accurate non-linear electro-thermal model, like the one that can be readily obtained with physical simulations including temperature dependence of transport and material properties.

A. *TCAD Simulation*

The very first step of a stacked PA design is to identify the characteristics of the common source stage alone. TCAD DC simulations are used to draw the device I/V characteristics and the AC analysis at 70 GHz to extract the small-signal parameters. The individual device fin currents are calculated taking into account the fin height of 40 nm. The individual fin current is scaled to model a unit cell with overall 300 fins (10 fingers with 30 fins each) for the evaluation of the overall DC current and PA power. In class-A bias condition, corresponding to 0.65 V drain voltage and 19.5 mA (65 μA/fin) drain current, the optimum load is $Z_{\mathrm{L,opt}} = 20\,\Omega$ (with negligible imaginary part due to our choice of neglecting inductive and capacitive parasitics), $Z_{\mathrm{S,opt}} = (1.9 + j61)\,\Omega$ and $g_{\mathrm{m}} = 87\,\mathrm{mS}$. Large-signal simulations show that, with the selected $Z_{\mathrm{L,opt}}$, the device can provide 5.5 dBm of output power at 1 dB compression and a 7.3 dBm saturated power with associated gain and efficiency of 12.7 dB and 40%, respectively.

The gate capacitance of the pseudo-common gate stage that provides power matching to the previous stage is [8]:

$$C_{\mathrm{G}} = \frac{C_{\mathrm{in}}}{g_{\mathrm{m}} R_{\mathrm{L,opt}} - 1} \tag{1}$$

An AC simulation in common source configuration with class-A bias is used to extract the value of C_{in}, which results around 27 fF, giving a C_{G} of 35 fF. The extracted value is of course heavily bias dependent and represents a coarse estimate based on linear analysis only: LS simulations are needed to validate the correct input matching of the two stages, both as a function of bias and when the PA enters compression. Any unbalance of the two stages may cause in fact unwanted early compression. To assess the impact of bias on the C_{G} choice, we will compare the stacked simulation results in class-A and in class-AB (20%).

Fig. 3 shows the TCAD-simulated stacked PA. Two devices as the ones of Fig. 1 are connected so that the drain of the CS FinFET is short-circuited to the source of the CG one. The overall simulation includes 7 terminals for the active devices and the embedding 7-port external circuit. Despite independent terminals are present for the two fin gates, the circuit is always operated with symmetric gate feed and loads, hence the two fin channels are identical. This effectively corresponds to the 3D device, where the gate metal is a unique contact. In this preliminary analysis, the CS FinFET input gate is unmatched and terminated by the the impedance of the source (50 Ω). The CG gate is terminated with the capacitance C_{G} calculated above (35 fF), while the drain of the CG stage is terminated with $2Z_{\mathrm{L,opt}}$ at the fundamental frequency and short-circuits at higher harmonics (tuned load). The bias is provided through ideal DC block and DC feed circuits. The drain bias of the CG FinFET is 1.2 V, i.e. double as that of the CS alone.

The HB simulation has been carried out with 6 harmonics + DC. This setup can be considered as a first demonstrator: further circuit components can be added to represent parasitics effects like capacitive coupling and metal resistances of the interconnections. The implemented simulation is extremely demanding from the TCAD standpoint. The two FinFETs share the same current since the common node of the two devices is terminated with a high resistance (1 MΩ/cm) not to perturb its voltage. The latter is entirely depending on the mixed-mode solution, where the CS FinFET is effectively terminated by an active load. Furthermore, the gate of the CG stage is only reactively matched, which again is a hard condition for the HB convergence. Nonetheless, a complete simulation of a power sweep for the stacked PA ($\sim$ 10K mesh nodes, 25 input powers, 6 harmonics) required roughly 3 hours CPU time.

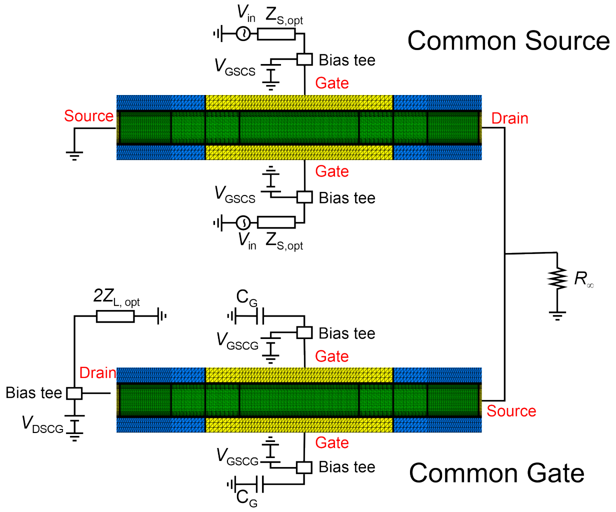

Fig. 3: Set-up of the TCAD stacked PA mixed-mode simulation. The external network is simulated by means of an equivalent 7-port linear circuit (4 gate terminals, 1 source, 1 drain, 1 common terminal which is kept virtually isolated by a high resistance termination R_{∞}).

IV. RESULTS AND DISCUSSION

Fig. 4 and Fig. 5 report the dynamic load lines at saturation of the two sub-stages in the class-A and class-AB case, respectively. TCAD analysis accurately predicts the time-domain waveforms at all device terminals, accounting for all parasitic effects, hence providing the designer a valuable insight on the device non-ideal behavior that guides in the optimization of the PA parameters. In the class-A case, where the large-signal C_{in} only slightly differs from the small-signal one, both stages see nearly the same load resistance, indicating that the selected value of C_{G} is close to the optimum. At the same time, it is clear form this results that there is a non negligible imaginary part that should be compensated. On the contrary, when biasing the stacked PA at 20% class-AB, the large-signal C_{in} differs much more from the small-signal value. Consequently, the loads seen by the two stages are different, the voltage swing does not split equally between the stages and the CG stage experiences earlier compression.

To confirm this analysis, we show in Fig. 6 the obtained large-signal (LS) input capacitance of the stacked pair compared to the value extracted with AC analysis and to the LS input capacitance of the CS stage alone. In the class-A case the difference is small, while in the class-AB one the actual input capacitance is only nearly 3/4 than the value adopted to size C_{G}, hence requiring optimization. Interestingly, in the stacked case the input capacitance variation with input power is much lower than in the CS alone case, since the load seen by the first stage is power-dependent.

Finally, the PA performance *vs* input power is shown in Fig. 7 and Fig. 8: power and gain boost are evident in both biasing cases. Saturated efficiency is 33% for the class-A stacked PA and 43% for the class-AB one.

V. CONCLUSION

Harmonic Balance TCAD simulation are the only way to investigate the physical behavior of semiconductor devices

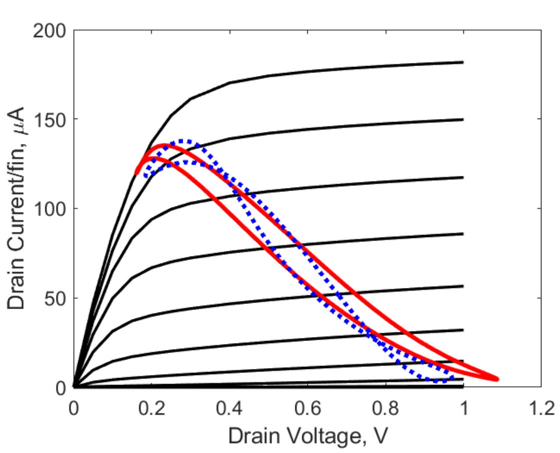

Fig. 4: Dynamic load lines of the stacked PA with class-A bias. CS (red solid line) and CG (blue dotted line) drain currents *vs* drain voltage at roughly 1 dB compression.

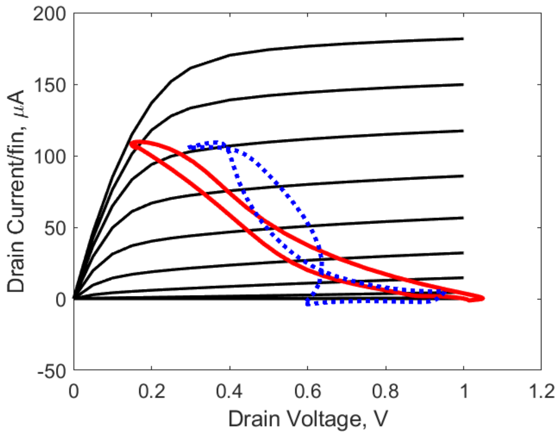

Fig. 5: Dynamic load lines of the stacked PA with 20% class-AB. Same notation of Fig. 4 applies. The available input power is the same as the class A stage. Contrary to the CS stage, CG exhibit early compression.

operated in nonlinear condition, thus representing a unique tool to simulate PA stages. On the other hand, mixed-mode simulations are especially challenging at the TCAD level when multiple active devices are connected. Contrary to the quasi parallel stage case (e.g. the Doherty configuration), the series connection adopted in the stacked PA architecture represents an even greater challenge, since the CG stage acts as an active load to the CS one. In this work, the TCAD simulation of a complete 2-FET stacked PA stage has been presented for the first time. The shown test case, based on 22 nm FinFET technology working at 70 GHz, demonstrates the potential utility of accurate physics-based models to the design of complex amplifiers at millimetre-wave frequencies. This work is a first step toward the development of an efficient behavioral model, allowing for design optimization in conventional CAD tools.

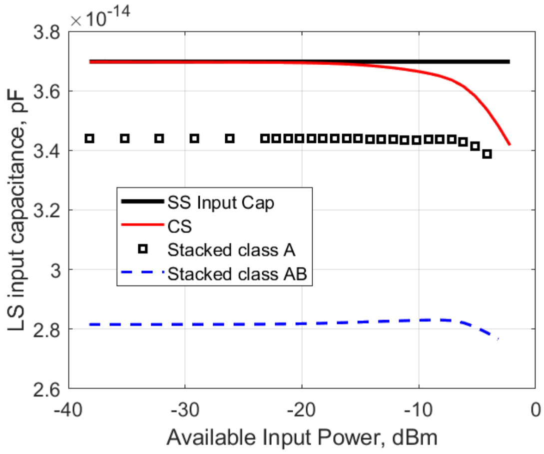

Fig. 6: Stacked PA LS input capacitance compared to the small signal value (solid black line). Single stage CS (red solid); stacked class-A (black symbol) and stacked class-AB (blue dashed).

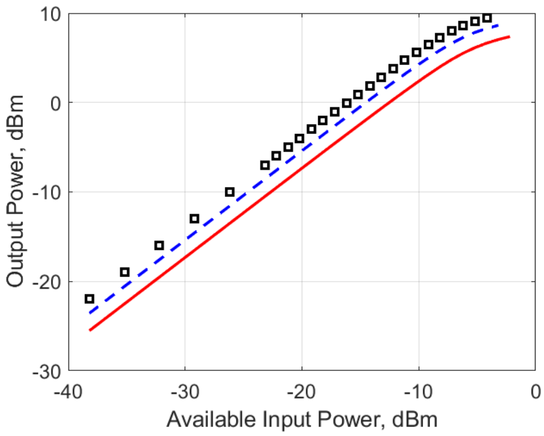

Fig. 7: Stacked PA output power. Comparison of class-A (black symbol) and class-AB (blue dashed) bias. The red solid line refers to the initial simulation of the CS stage alone biased in class-A, which is taken as reference.

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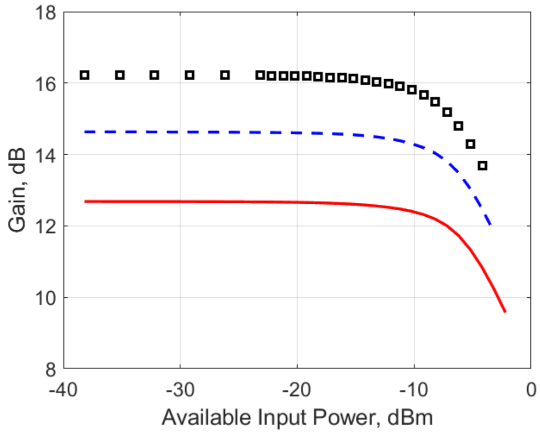

Fig. 8: Stacked PA power gain. Same notation of Fig. 7.

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