A Ka-band MMIC Power Amplifier in 100-nm GaN-on-Si technology for Space Applications

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***Abstract*—This contribution reports the design and preliminary on-wafer characterization of a Ka-band MMIC power amplifier (PA) for an earth observation application using a commercial 100-nm GaN-on-Si technology. Design solutions adopted to deal with constraints and challenges posed by space-grade requirements are discussed in detail. In particular, when adopting a Si substrate, thermal management becomes a major issue, requiring the design to be conceived for low power dissipation. Simulation results of the designed amplifier are in line with the state-of-the-art, with an output power in excess of 10 W in the 34 GHz to 37 GHz range, with associated PAE and gain close to 30% and 20 dB, respectively. On-wafer measurements in pulsed conditions confirm the output power capability, but also show some criticisms that need further investigation.**

***Index Terms*—GaN, MMIC power amplifier, earth observation, space derating**

I. Introduction

Recent advancements in sub-quarter-micron gate-length (100-200 nm) GaN HEMT processes are allowing solid-state power amplifiers (SSPAs) to be considered as the key technology for millimetre-wave (mmW) communication systems, as well as for radar and remote sensing applications in Ka-band [1], [2]. However, achieving high performance above 30 GHz is still challenging even for mature 150 nm technologies which are very close to their limit [3], [4]. Targeting the high-end portion of the Ka-band spectrum the OMMIC (now MACOM) D01GH GaN-on-Si process [5]–[7], featuring 100-nm gate-length, is, at present, the one of the shortest-gate-length European process commercially available.

Power amplifiers for space applications are particularly challenging to design due to the stressing environmental operating conditions and long-term reliability requirements, which in turn require supply derating, device over-sizing and limited device temperature [8]. In particular, thermal stress due to a high ambient temperature (75-85 °C) and difficult cooling, may become a major limiting issue when adopting a Si substrate, as it features a higher thermal resistance than SiC [9].

This work, developed in the framework of an ESA project for earth observation, aims at assessing the potential of the OMMIC technology for the design of a space-compliant SSPA with the highest possible output power. In particular, the design focuses on the development of a narrow-band MMIC working in the 35.2 GHz to 36 GHz range, targeting 6-10 W of saturated output power, suitable for a remote sensing altimeter application [10]. The targeted gain and efficiency are 20 dB and 20-25%, respectively. Thermal limitations, together with the additional requirements of power, gain and efficiency in pulsed regimes very close to CW condition, led to the choice of a deep-class-AB parallel-combined architecture with a very large active device periphery in the final stage. The combination of many devices in a compact MMIC working at high frequency requires extensive electromagnetic (EM) optimization to properly account for EM coupling between adjacent elements which may significantly change the behavior of passive networks with respect to circuit-level simulations [11].

Despite the limitations posed by space derating, the designed PA demonstrated in simulation an output power of nearly 12 W in the targeted bandwidth and larger than 10 W in the extended 34-37 GHz range. The associated power gain and PAE are above 19.6 dB and 29%, respectively: results that are well in line with the state-of-the-art at this frequency, as shown in Tab. I. The on-wafer small-signal (SS) and large-signal (LS) characterization of the fabricated MMICs, in pulsed conditions, confirm the capability of the designed PA to provide more than 10 W at Ka-band. However, they also showed an unexpectedly large spread, symptoms of instability and poor PAE, the subject of further investigation, likely due to threshold voltage variation impact at the low quiescent current density selected to minimize power dissipation in the RF-off state.

II. Design

The D01GH GaN-on-Si HEMT process from OMMIC features a 100 nm gate-length, hence showing useful available gain up to 50 GHz [5]. Despite a 50 V breakdown voltage, the maximum recommended drain supply voltage is only 15 V. According to space derating rules [8], the selected value is 11.25 V (75% of Absolute Maximum Range, AMR): this choice guarantees that, for a class-AB PA design, the instantaneous dynamic drain voltage of the devices reaches a peak value well below the maximum derated breakdown voltage. According to ESA's specification, the PA is expected to be operated with a constant DC and pulsed RF, thus a class-AB

TABLE I: Comparison of the present work (P.W.) with the literature. The † symbol indicates commercial processes. Due to performance spread the average values are reported for the P.W.

Ref.	Technology	Frequency GHz	P_{out} dBm	Gain dB	PAE %
[12]	0.15 GaN	32 – 38	38	33	NA
[13]	0.2 GaN/SiC†	34.5 – 36.5	37.7	25	41
[14]	0.15 GaN/SiC†	32 – 38	40.5 37.1	25 17.5	35 34
[15]	0.15 GaN/SiC	34 – 36	43	16	27
[16]	0.1 GaN/Si†	30 – 34	40	25	27
[3]	0.15 GaN/SiC†	29.5 – 36	39.5	19	20
[17]	0.1 GaN/Si†	34 – 38	36.4	30	29.5
[18]	0.15 GaN/SiC	33 – 38	30	13	17.5
[19]	0.15 GaN/SiC	31 – 36	33	NA	27
[20]	0.1 GaN/SiC	28 – 38	37.8	20	36.1
[21]	0.15 GaN/SiC	32 – 38	41.8	16	31
P.W.	0.1 GaN/Si†	35 – 36	39.5	24	18

bias is preferable to limit temperature when the RF is off. On the other hand, the on-time of the RF bursts specified by ESA is rather long compared to the device thermal time constants (equivalent duty cycle of 90%) hence continuous wave (CW) operating conditions (worst case) have been considered for computing the junction temperature according to the model discussed in [9]. A very low current density (deep class-AB) bias of roughly 35 mA/mm has been selected. Although potentially prone to small-signal performance variation and sensitivity to HEMT threshold dispersion, this bias point showed advantages in large-signal simulations in terms of maximum junction temperature and PAE, thus allowing for a higher output power density at the cost of a reduced small-signal gain and hence a marked gain expansion strongly dependent on AC/DC large-signal nonlinear conversion.

With the selected bias, the output power density is around 3.1 W/mm. Nevertheless, the achievable value reduces to roughly 2.5 W/mm when considering the given space-grade thermal limits, i.e. a 160 °C maximum junction temperature at 80 °C MMIC backside, which basically translates into a maximum allowable dissipated power of about 2 W/mm [9], [22]. The dissipated power limit strongly impacts on the available design space: as shown in Fig. 1, the thermal constraint confines the optimum load into an highly reflective impedance region, implying high transformation ratios and high sensitivity to phase variations for the output matching network.

The 4x100 μm device itself gives around 30 dBm, hence requiring the parallel combination of 16 devices to reach 10 W at MMIC level. The associated gain is 5.6 dB, hence requiring a 4-stage architecture to comfortably achieve the targeted large-signal gain of 20 dB. The full block diagram of the PA is shown in Fig. 2a and is designed to fit a 4.5x5 mm^2 footprint. To achieve a compact chip size, the via holes for source grounding are shared between adjacent devices in the final stage. As this may increase the equivalent inductance, large holes have been adopted. Another possible issue of shared via holes is a more limited thermal sink effect with respect

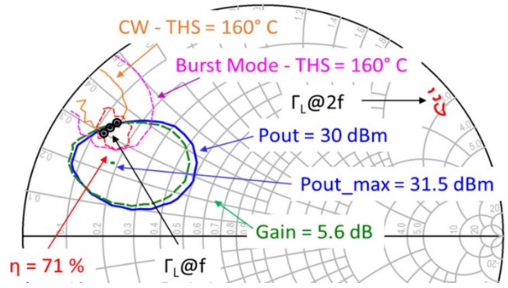


Fig. 1: Simulated load-pull contours at 36 GHz (4x100 μm device): the optimum load (black dots) must be selected according to the junction temperature limit (orange CW, pink 90%–duty-cycle pulsed), with output power penalty of 1.5 dB.

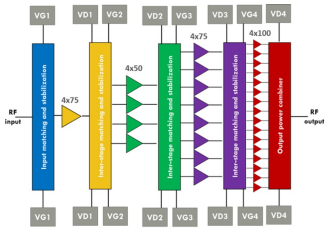
to separate ones, which is accounted for by using 3D-FEM thermal simulations to estimate the effective thermal resistance with cross-heating [9]. Finally, such a large number of devices implies a very dense layout and thus critical EM optimization of the passive structures [17].

All devices are made wideband unconditionally stable through the insertion of a parallel RC at their gate. The output power combiner minimizes the number of lumped components and hence losses and sensitivity to process variations. Unbalanced impedances, observed from EM simulations despite the geometrical symmetry, have been compensated with drain shunt connections, allowing small differential (odd) currents to flow, and pairing voltage levels. The other inter-stage matching networks have been designed in a similar manner. A driving margin of about 1 dB was taken in simulation between each stage as a good trade-off between PAE and design risk. The impedance step between the first and second stage is the highest one due to the 1 to 4 power splitting required, therefore a 3-step impedance transformer is adopted. Gate voltages are also balanced through shunt connections embedding also lumped resistances (10-20Ω) to prevent odd-mode oscillations.

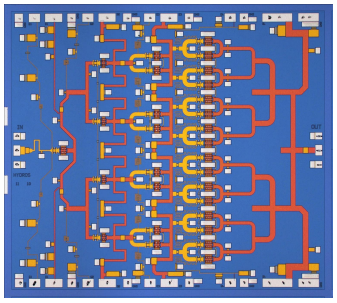
The gate bias networks adopt lumped spiral inductors or meandered high-impedance lines as RF chokes. The drain bias is supplied symmetrically at both sides of the MMIC, since the use of a single bias rail for feeding all the 16 devices would require too large lines. The fabricated MMIC HPA is shown in Fig. 2b, while the LS simulated performance in the 34-37 GHz range at 80 °C backside temperature is reported in Fig. 3. At the nominal operating point (NOP), the output power is above 11.9 W in the 35.2-36 GHz range, with associated PAE and gain above 29% and 19.6 dB, respectively, all with a fairly good flatness in the extended 34-37 GHz range. Device junction temperatures, verified through 3D-FEM thermal simulations, are all within 140 °C.

III. On-wafer Characterization

The on-wafer characterization for chip selection has been carried out by the OMMIC foundry with an automated test bench on all available samples. To avoid device over-heating, both SS and LS measurements were performed with pulsed

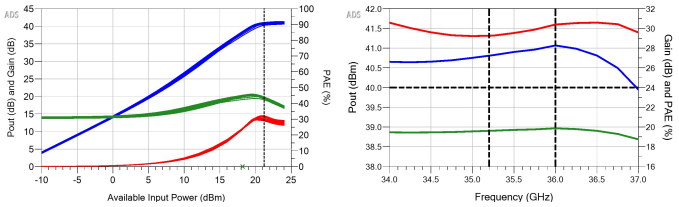


(a) PA architecture.



(b) Microscope picture of the MMIC.

Fig. 2: Developed MMIC power amplifier.

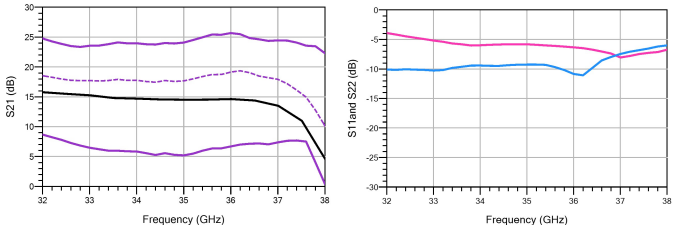


(a) Power sweep (dashed line = NOP). (b) In-band performance at NOP.

Fig. 3: Large-signal simulation results: output power (blue), power gain (green) and PAE (red).

bias (1% duty cycle and 10 μs). This approach allows room-temperature characterization with no need of thermal chuck, but is more prone to stability issues since relatively small bypass capacitances must be adopted in pulsed mode. Indeed, some samples showed a unstable bias current and, overall, quite a large dispersion in bias currents, and hence in performance, was found, as shown in Fig. 4 and Fig. 5. This unexpected spread can be ascribed to threshold voltage dispersion across the wafer and even within the chip, a hypothesis confirmed also by PCM results. In other words, it is likely that at the deep class-AB bias selected, some devices in the chip are almost off while others are correctly on, dramatically affecting the PA behavior, especially in SS, considering also the large number of devices adopted.

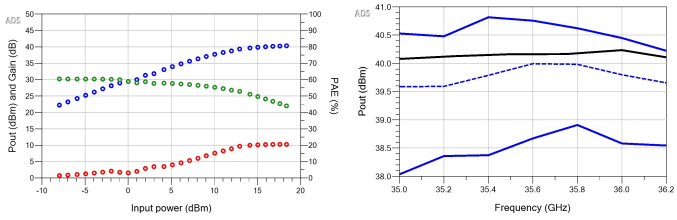
Nonetheless the measured performance can be still considered very promising, with 35 working samples showing average output power, gain and PAE respectively in excess of 9 W, 24 dB (LS) and 18% in the targeted frequency band. Among them, 12 samples exhibit more than 10 W output power. The sensibly higher gain found, both in SS and LS, with respect to simulations, as well as the higher drain current resulting in a PAE lower than expected, may indicate stability issues related to the on-wafer pulsed measurement set-up, but may also be due to device model and process variability issues, hence requiring further investigation. The hypothesis of model inaccuracy is corroborated also by the very different gain behavior *vs.* input power observed in measurements (compression) with respect to simulations (expansion).



(a) Small-signal gain: min. and max. curves (purple) compared to simulations (black); dashed line = average.

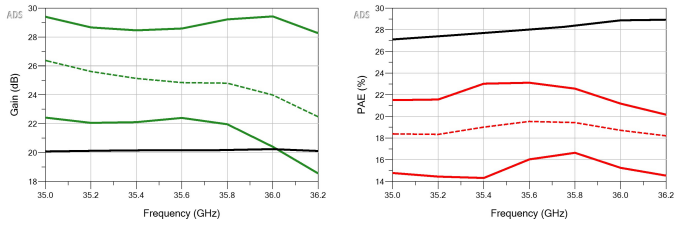
(b) Small-signal input (magenta) and output (cyan) return loss: worst case curves shown.

Fig. 4: Small-signal measurement results at fixed (V_G, V_D) bias (same for all chips).



(a) Power sweep of a slected sample (36.8 GHz).

(b) Saturated output power.



(c) Saturated power gain.

(d) Saturated PAE.

Fig. 5: Large-signal measurement results at fixed (V_G, V_D) bias (same for all chips). Minimum and maximum measured output power (blue), power gain (green) and PAE (red) compared to on-wafer simulations (black); dashed line = measurement average.

IV. Conclusion

The design and on-wafer characterization of a 10 W Ka-band power amplifier for space applications are reported and discussed: simulation results, remarkable for a space-grade PA, are confirmed by measurement results in terms of output power capability. However on-wafer characterization revealed some unexpected criticism, which require deeper investigation.

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