Monolithic GaN for a High-Efficiency Interleaved Boost Converter PFC in Automotive Applications

Filippo Scrimizzi
STMicroelectronics
Stradale Primosole, 50
95100 Catania
filippo.scrimizzi@st.com

Federica Cammarata
STMicroelectronics
Stradale Primosole, 50
95100 Catania
federica.cammarata@st.com

Giuseppe D'Agata
STMicroelectronics
Stradale Primosole, 50
95100 Catania
giuseppe.dagata01@st.com

Salvatore Musumeci
DENERG- Politecnico di Torino*)*
Corso Duca degli Abruzzi 24
10129 Torino
salvatore.musumeci@polito.it

Vincenzo Barba
DENERG- Politecnico di Torino*)*
Corso Duca degli Abruzzi 24
10129 Torino
vincenzo.barba@polito.it

Santi A. Rizzo
DIEEI Università di Catania
Viale Andrea Doria 6
95123 Catania
santi.rizzo@unicit.it

***Abstract*— The pollution-reducing effort is pushing the automotive market towards greener alternatives to the internal combustion engine, the main examples being mild/plug-in hybrid and full electric solutions. In this context, having increasingly small, light, and energy-efficient DC/DC conversion systems is crucial. This paper presents a dual-phase interleaved boost converter power factor correction system. Thanks to the emerging GaN technology and a microcontroller-based control loop approach, it achieves a peak efficiency of about 98% when switching at 300 kHz under a 1.5 kW output load. The proposed converter then raises the standard in terms of performance vs system dimensions and weight, with the added benefits of a fast and precise control loop thanks to the dedicated controller and an interleaved topology that provides almost-zero output current ripple, a crucial point for a charging system that can help in reducing the high voltage battery wear over time.**

Keywords*— *Gallium Nitride, Interleaved Converters, Automotive Application, Power Factor Correction, Efficiency.

I. INTRODUCTION

As the automotive market becomes increasingly environment-aware, Original Equipment Manufacturers (OEMs) are heavily investing in car electrification, with the goal of shifting production towards hybrid and full electric solutions. Power electronics play an important role in this process, as electric, vehicles need charging and DC/DC conversion systems with the best possible efficiency while containing their size and weight, thus maximizing the power density.

Wide bandgap materials, of which the main examples are Silicon Carbide (SiC) and Gallium Nitride (GaN), are very suitable for realizing devices capable of addressing these needs. Thanks to the higher critical field compared to Silicon, GaN High-Electron Mobility Transistors (HEMTs) can offer the same breakdown voltage in a smaller form factor, which leads to lower parasitic capacitances and, thus, better overall switching behaviour [1].

Fig. 1 shows the core structure of a GaN HEMT, based on the AlGaN/GaN hetero-structure, which exploits the conduction band energy level difference between the two materials, leading to the formation of the Two-Dimensional Electron Gas (2DEG) at the interface [2].

The 2DEG can be modelled as a layer of electrons which are free to move in the two directions parallel to the heterojunction but not in the perpendicular one. This allows electrons to have exceptionally high mobility values in this region (up to 1500 cm^2/Vs) [1], which allows HEMTs to have a significant improvement in terms of switching speed when compared to traditional Silicon MOSFETs.

Moreover, the lack of a body diode avoids the reverse recovery phenomenon, further enhancing their switching frequency capability and lowering the switching losses.

These features can be exploited in power conversion systems, with advantages in terms of speed, power density, and thermal characteristics.

The main drawback of this technology is the normally-on behaviour resulting from the heterostructure, which is not suitable for power applications, especially when dealing with high voltage and power levels. To overcome this problem, many solutions have been proposed, the main being the recessed gate structure, negative charge implantation in the GaN layer, or the p-GaN gate structure.

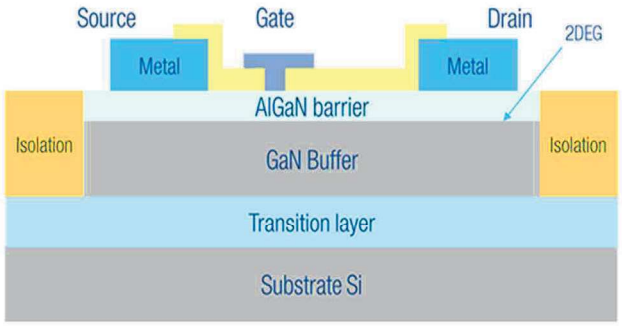

Fig. 1. Basic structure of a GaN High-Electron Mobility Transistor.

There are several examples in the literature of power conversion systems using the GaN technology, especially considering the electric mobility field [3]. For example, in [4], a 7.2 kW single-phase onboard charger has been built using a totem pole power factor correction input stage and a GaN-based full bridge LLC topology for the second and third stages. By connecting three of these modules to the three-phase grid, a 22 kW has been realized too. Thanks to the use of GaN devices, the system is able to reach 97% efficiency while shrinking its physical dimensions, allowing for a power density of up to 3.3 kW/L. As opposed to the SiC-based version of the same system, it is shown how the GaN-based charger achieves sensibly lower switching losses, reduces

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gate-drive power losses, and allows transformer shrinking and, therefore, a lower overall cost [5].

Another example of a high-frequency bi-directional battery charger for plug-in hybrid vehicles is given in [6], which operates at 500 kHz for both the full bridge AC/DC first stage and the dual active bridge (DAB) DC/DC stage. The high-frequency leg of the grid-side converter is built to replace Silicon MOSFETs with normally off cascode structure GaN devices, which reduces the switching losses by one-half, while the DAB stage is entirely GaN-based. In this way, it is possible to reach 97% efficiency for both stages, leading to 94.2% for the overall system. These examples show how the GaN technology can be disruptive in these applications and significantly boost performance. However, these can be further enhanced, as there are still minor power losses sources that mainly come from the gate drive and the reverse conduction losses during the dead time, which are worsened by the use of a negative voltage to turn off the switches, as this is usually the case when using discrete devices to avoid false turn-ons. However, these can be further enhanced, as there are still minor power losses sources that mainly come from the gate drive and the reverse conduction losses during the dead time, which are worsened by the use of a negative voltage to turn off the switches, as this is usually the case when using discrete devices to avoid false turn-ons.

To this extent, this paper presents a dual-phase interleaved boost converter power factor correction system that relies on an innovative, full GaN-based, monolithic technology. The integrated approach can offer several advantages when compared to the discrete equivalent: the driver-to-transistor interconnection can be minimized, with benefits both in terms of stray inductances and V_{gs} stability, increasing the device reliability from gate structure integrity and protection. Moreover, a zero-driving voltage can be used at turn-off, further reducing power losses when the HEMT is conducted in reverse mode.

Another innovative aspect lies in the use of an STM32 microcontroller. Thanks to features like the high-resolution timer, fast ADCs and op-amps, and a dedicated software algorithm, it allows to implementation of a precise and effective control loop.

Thanks to these features, it has been possible to drive the converter at a high switching frequency, maintaining a stable output voltage and achieving impressive efficiency results.

The paper is organized as follows. In section II the overall design process of the proposed converter is described, whilst in section III the experimental setup and the obtained results are presented. Conclusions are then summarized in section IV.

II. PFC Board Design

The overall design process of the proposed converter board, with a brief description of the used power module and the dimensioning of both the power stage and the control loop, is presented hereafter. The final schematic is included and described too, along with some preliminary software simulation results.

The basic working principle of a single-phase boost converter relies on the energy-storing capability of the power inductor, which is charged at the input voltage value during the switch on-time while supplying energy to the output load during the off-time.

A. Monolithic Power Stage

The converter proposed in this paper relies on the STi²GaN power device (standing for ST Intelligent and Integrated GaN), which combines into a monolithic solution the driving stage and a 30 mΩ, 650 V breakdown voltage power HEMT in a single, dual-side cooling package. The combination of the intrinsic features of GaN technology, the monolithic approach, and a package studied to bring the lowest possible parasitic contributions allows the device to manage up to 70 A of continuous current and to switch at a frequency as high as 1 MHz.

As can be seen from the simplified schematic in Fig. 2, this power device has the advantage of integrating protections from overcurrent and over-temperature events, both of which have a dedicated diagnostic pin, which can be read and managed by the external microcontroller. Moreover, it offers the possibility to tune the turn-on dV/dt, ranging from 60 to 100 V/ns, which can help limit electromagnetic interferences (EMIs), if needed. The monolithic solution features robustness and improved reliability, also thanks to the internal voltage regulator, which gives a precise supply voltage for the internal driver. In this way, the power HEMT is driven with a stable gate-source voltage with no overshoots, which can be a cause for concern in p-GaN gate technology-based HEMTs. Thanks to all these features, a compact design of both the system power stage and driving circuit is possible.

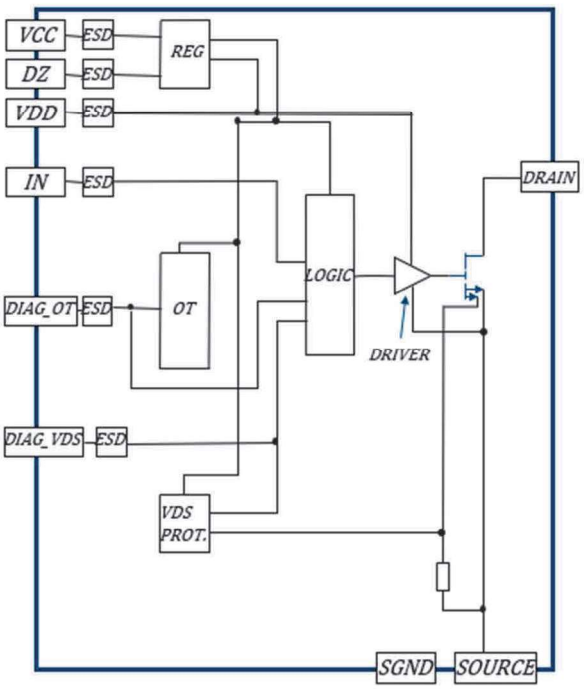

Fig. 2. Simplified block diagram of the STi²GaN power device.

B. PFC Circuit System for Automotive Application

In the specific case of an automotive PFC application, the system is expected to work at 200 V input voltage while outputting 400 V DC, therefore being driven at D = 0.5 when working in continuous or critical conduction mode. Considering the design constraints, a dual-phase interleaved topology has been chosen. The interleaved topology contributes to the overall increase in system power density, allowing the dimension of each stage for a fraction of the total output power and reducing the output current ripple, whose behaviour is shown in Fig. 4 for single, dual, and three-phase

systems as a function of the switches on-time. For a dual-phase converter driven at D = 0.5, its amplitude drops ideally to zero [7].

The main characteristics of the board power stage are summarized in Table 1. It has been designed to withstand a maximum output load of 3 kW and to operate in critical conduction mode at this load condition. The average current considered for each phase is then equal to 7.5 A, with an inductor current variation, ΔI_L (equal to the peak value), of 15 A.

TABLE I. MAIN CHARACTERISTICS OF THE PFC CONVERTER

Parameter	Value
Input voltage	200 V
Output voltage	400 V
Maximum output power	3 kW
Switching frequency	300 kHz
Phase inductors	20 µH
$\Delta I_{L,max}$	7.5 A
MCU Board	NUCLEO-STM32G474RE

The switching frequency of the converter has been chosen as a compromise between fully exploiting the performance and advantages given by the STi^{2}GaN devices and limiting the switching losses, as these obviously increase with frequency and can negatively impact the efficiency and thermal performance of the system. Therefore, the value has been fixed to 300 kHz. This yields a power inductor value of ≈ 22.2 µH, so the final choice has then relapsed on a custom-made 20 µH inductor with a saturation current of 22 A. The output capacitance has been fixed to 470 µF to smoothen the output voltage and minimize the ripple, as well as ensure to supply of the load when both switches are off, that is, when the microcontroller regulates the duty cycle to a value lower than 50% [8].

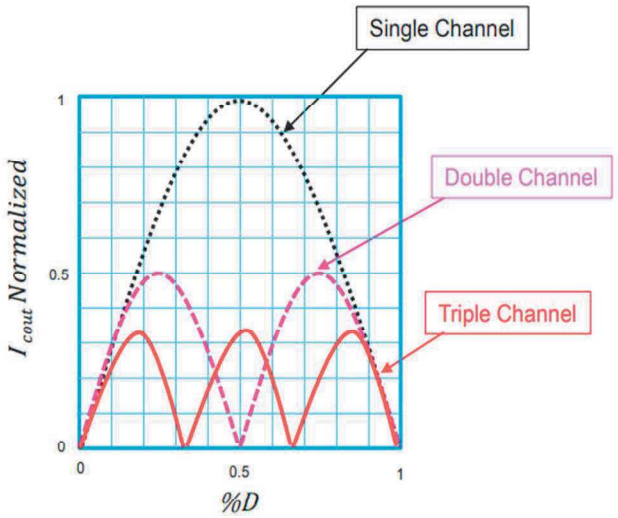

Fig. 3. Output current ripple amplitude for single, dual, and triple phase systems as a function of the duty cycle.

C. PFC Control and Protection Circuits Issues

The control loop relies on the STM32 microcontroller board to regulate the duty cycle and, thus, the output voltage via a software PID algorithm. Thanks to the embedded high-resolution timer, the timing parameters such as the switching period, the phase shift and the duty regulation can be very precise, with a resolution of 184 ps. To enhance safety, the output and input voltage are both sensed by means of two optocouplers to isolate the high voltage from the MCU input pins. The optocoupler's input is connected to the high-voltage section through a resistor, allowing current to flow through the input LED. Consequently, a proportional current is produced on the collector of the output BJT, which is connected to a 3.3 V point – given by the STM32G474RE MCU board – through a load resistor. The voltage signal on the output collector is then read by the ADC of the MCU and is given by:

$$V_c = 3.3 - i_c R_c$$

In this way, the optocoupler's output is inversely proportional to the input voltage, which gives an additional safety measure to protect the microcontroller. The load current is also sensed via a 5 mΩ shunt resistor. The microcontroller software includes a soft start function, which avoids the in-rush current at the start-up of the converter by slowly and gradually increasing the duty cycle until the output voltage reading matches the set reference value [9]. Additionally, some protection functions from overcurrent and/or load short circuit events have been included, as well as an input voltage check function to ensure that the output target can be reached.

D. Schematic circuit implementation and simulation validation

Fig. 4 shows the full block schematic of the board. An auxiliary 15 V supply is used to power the STi2GaN modules and a voltage regulator, providing a stable 7 V output to power the STM32 microcontroller board. A NOR logic gate IC is also interposed between the PWM output of the MCU and the input pin of the STi^{2}GaN module to shift the level of the driving signal from 3.3 V to 5 V. An input-to-output diode has been added to pre-charge the output capacitor which helps to avoid in-rush current at startup. To validate the design, the system has been simulated using LTSpice software. To achieve the best possible simulation accuracy, a model of a GaN HEMT with 650 V breakdown voltage and 30 mΩ $R_{ds(on)}$ was used, as well as a realistic model for all discrete components, so as to consider losses due to parasitic resistances and stray inductances [10]. The two devices are driven by two ideal voltage generators setting two square waves at 300 kHz and shifted by a half-period. The simulation has been performed by setting a transient analysis with a duration of 20 ms, which allowed us to analyze both the startup and steady-state behaviour of the converter. The used time-step resolution is 10 µs, as the best compromise between simulation speed and accuracy. Fig. 5 shows a single simulated switching period, which highlights how the converter correctly reaches the target voltage and how the dual-phase topology eliminates the ripple on the load current.

I. EXPERIMENTAL INVESTIGATION

The system has been experimentally tested using a prototype board (Fig. 6). This section reports and describes the experimental setup and the waveforms acquired during the process. An efficiency plot versus output power is also included.

To supply the input voltage, a TDK-Lambda GEN600-5.5 DC power supply has been used, which can provide a maximum of 600 V and 5.5 A DC.

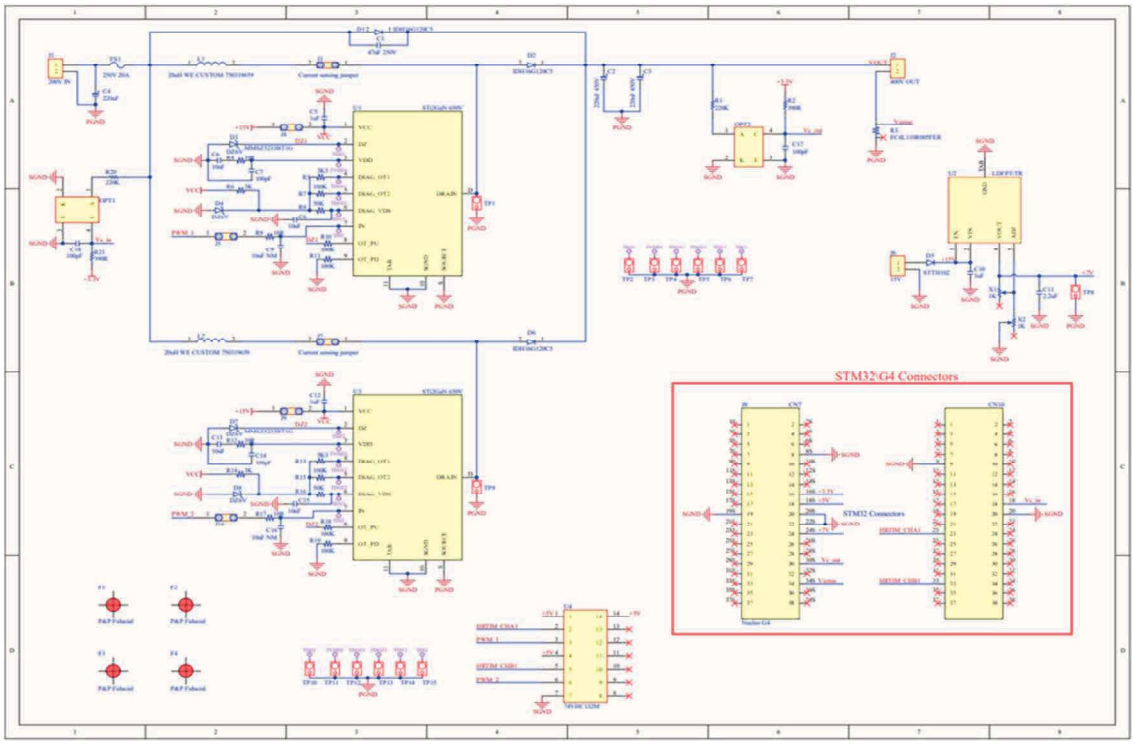

Fig. 4. Complete schematic of the proposed PFC solution.

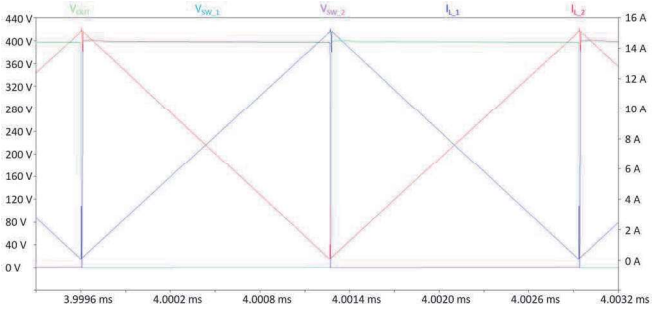

Fig. 5. Detail of a single switching period result from simulation. The green trace is the output voltage, cyan and pink are the two switching nodes, and blue and red traces are the inductor currents.

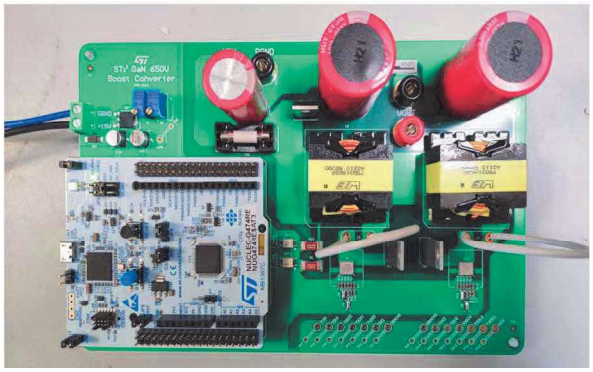

Fig. 6. Picture of the final PFC demo board.

Due to the high input current needed, two power supplies have been used in parallel in a master-slave configuration, allowing to double its nominal current output. The ITECH IT8322 regenerative DC electronic load has been used in constant resistance configuration to set the loading current value of the converter and its power delivery performance and to run the efficiency measurements. As for this point, two Yokogawa WT310EH digital power meters have been inserted, respectively, into the input and the output of the converter. Finally, the auxiliary 15 V input voltage has been provided by the low-voltage DC power supply GW Instek GPD-3303D. At the same time, all the waveforms have been measured using a Teledyne-LeCroy HDO8058A 500 MHz high-definition oscilloscope, using six of its eight analog channels. To minimize the measurement oscillations and interferences, the demo board adopted testing points specifically designed for passive probes with pig-tail ground contact. The board layout has been optimized to minimize the length of the testing point traces in order to reduce stray inductances.

A preliminary test at low output voltage and power (about 80 V, 25 W) has allowed to verify the correct switching of the power devices and the effectiveness of the MCU algorithm.

As the power devices are still early engineering samples, it has been decided to perform further tests in a 150 V input – 300 V output voltage configuration and up to a maximum of 1.5 kW output power as a safety measure. By setting the electronic load in constant-resistance mode and gradually varying the load resistance value, various tests have been performed, with 100 W steps from one test to the other. For each test, measurements of the input and output power using the two power meters have been performed to evaluate the efficiency as a function of the output load. Fig. 7 shows the waveforms for the two switching nodes, the phase currents, and the driving PWM signals taken at Pout = 500 W. The converter is deeply working in discontinuous current mode, with oscillations on both the switching nodes and the phase currents after the zero-crossing.

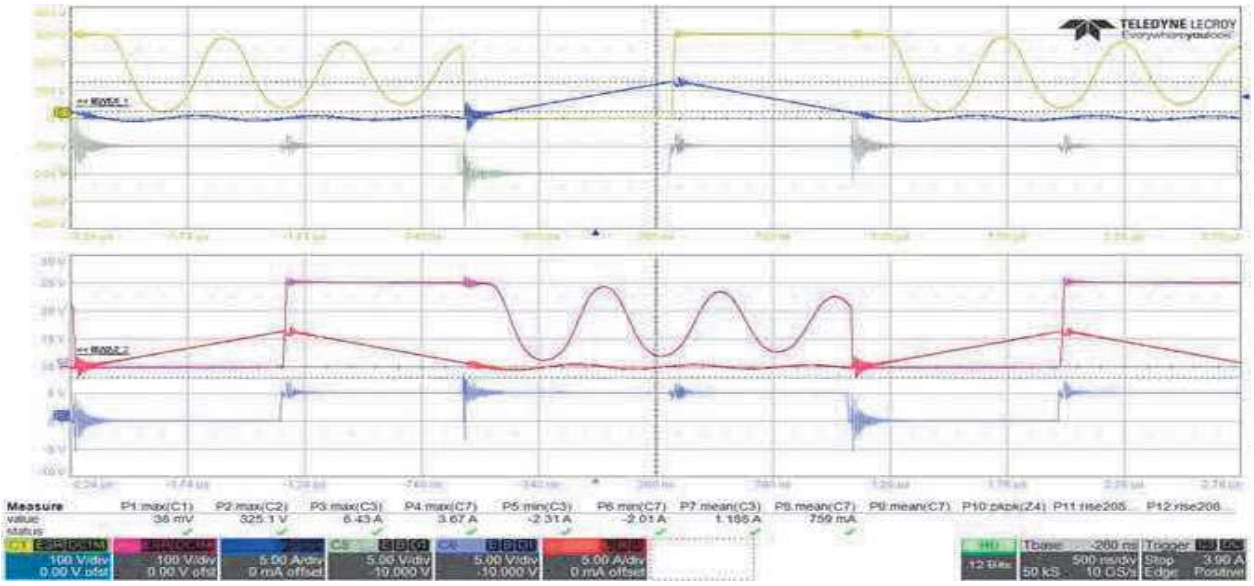

Fig. 7. Waveforms taken at 500 W output power. Yellow and purple traces are, respectively, the VDS of the two power devices, red and blue traces are the inductors currents I_L, grey and light blue traces are the two PWM signals

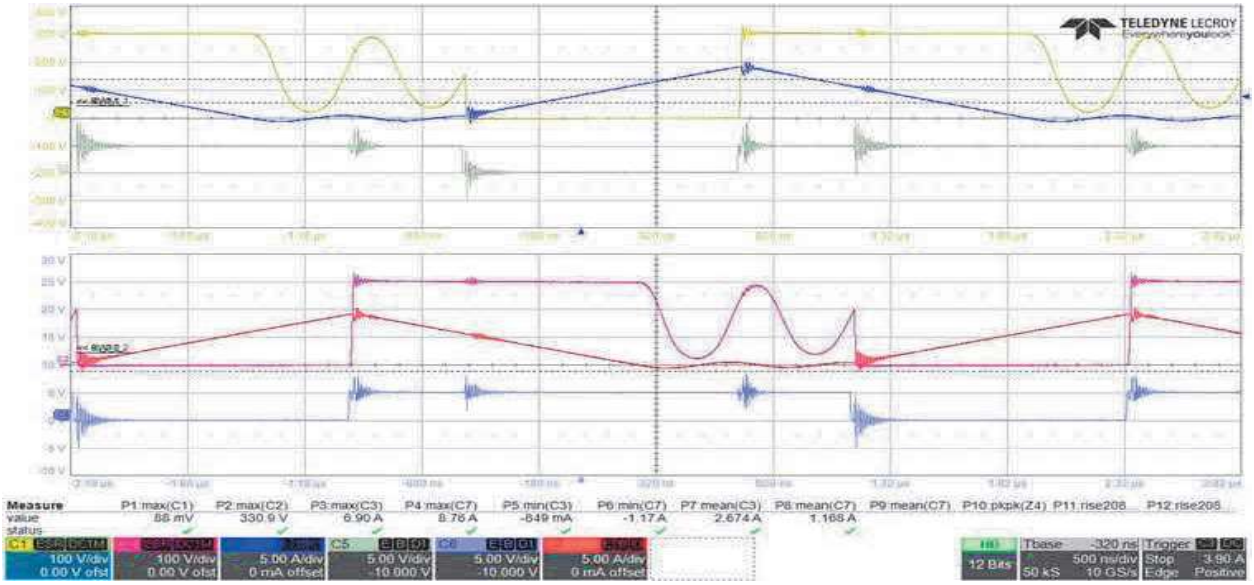

Fig. 8. Waveforms taken at 1 kW output power. Yellow and purple traces are, respectively, the V_{DS} of the two power devices, red and blue traces are the inductors currents I_L, grey and light blue traces are the two PWM signals.

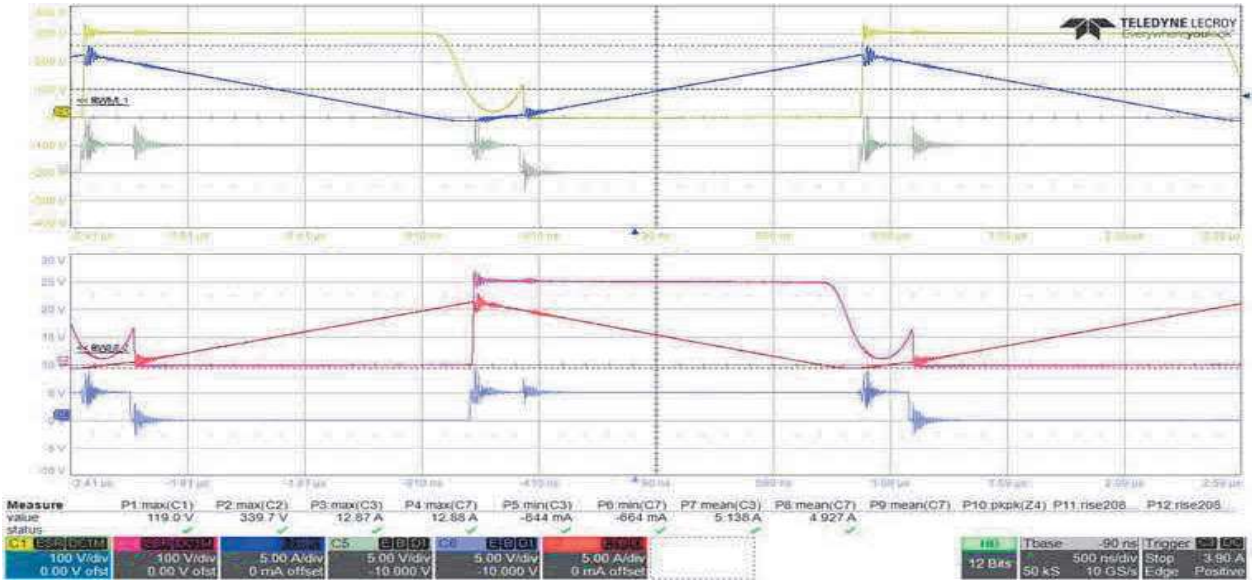

Fig. 9. Waveforms taken at 1.5 kW output power. Yellow and purple traces are, respectively, the V_{DS} of the two power devices, red and blue traces are the inductors currents I_L, grey and light blue traces are the two PWM signals.

It should be noticed that each phase current leads to the corresponding switching node voltage, suggesting that the discharging of the output capacitance of the power device triggers this behaviour. The current deriving from this process is then forced to flow on the phase inductor because the diode is in the off state, causing a temporary rise in VL, which in turn tends to charge the capacitor again, triggering a resonance phenomenon with an amplitude that decreases over time. Moreover, due to the large dv/dt, ringing is observed in the phase currents at the turn-on of the power devices. The commutation of each phase also causes coupling-induced disturbs on the driving PWM signals. Waveforms for the test at 1 kW output power, reported in Fig. 8, show similar behaviour with reduced resonance ringing due to the wider on-time of the power devices. Ringing on the two PWM signals is still present but not worsened by the heavier load conditions. An estimation of the V_{DS} ringing frequency for the two power devices has been obtained using the oscilloscope, yielding a value of 65.8 MHz. Hence, the board stray inductances are some tens of nH considering an output capacitance in the tens of nF range. Voltage overshoot has been quantified too at slightly higher than 11%.

At 1.5 kW output power (Fig. 9), the converter is very close to the critical conduction mode, with a mean current per phase equal to ≈ 5 A. Even under this load condition, the converter shows the same behaviour seen in the two previous cases, thus working as expected.

Fig. 10 shows the efficiency of the converter, plotted against the output power. At low load conditions, the combined effect of the switching losses and the resonance-induced switching node fluctuations has a big effect on the dissipated power, thus causing a drop in efficiency. As the output power increases, their impact becomes less influential, while conduction losses are limited thanks to the low $R_{DS(on)}$ of the two power devices. This allows for reaching a peak efficiency of 97.94% at 1.5 kW output power.

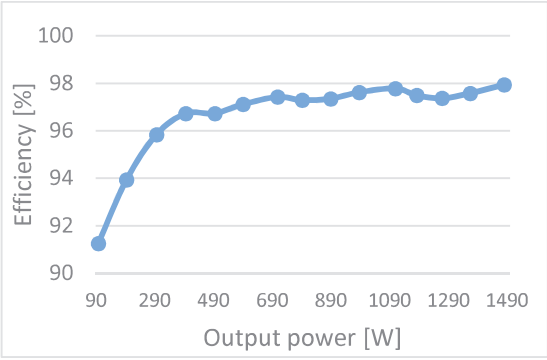

Fig. 10. Plot of the measured efficiency vs output power.

II. Conclusions

This paper presents an interleaved, dual-phase boost converter PFC based on the emerging GaN technology. The proposed solution has been designed, realized, and tested up to 1.5 kW output power. Thanks to the interleaved topology, the output current ripple is strongly reduced, which provides a big advantage in battery charging systems, as this helps augment the lifespan of the high-voltage battery.

Furthermore, the use of GaN devices allows the reduction of system size without any significant concerns, giving a contribution to realizing smaller and more lightweight On-Board Charging blocks. Despite the high switching frequency and the asynchronous rectification, the converter is still able to reach a peak efficiency up to 98% under the fully tested output power, further demonstrating the effectiveness of Gallium Nitride-based solutions in power conversion applications. Future work will include further tests up to the 3-kW target once the STi^{2}GaN power devices are fully mature and a partial redesign of the converter to achieve synchronous rectification and reach even higher efficiency values.

Early tests using a new version of the STi^{2}GaN power devices are already ongoing. As this new cut is designed to be more robust to withstand both higher drain-source voltages and hard switching conditions, the 3-kW target appears to be a realistic one. In fact, it has already been possible to test the converter at the full 200-400 V voltage target and reach 2 kW output power with the same mean output current and achieve similar results in terms of efficiency. To further increase the output power, however, correct management of the dissipated heat is mandatory.

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