

Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3

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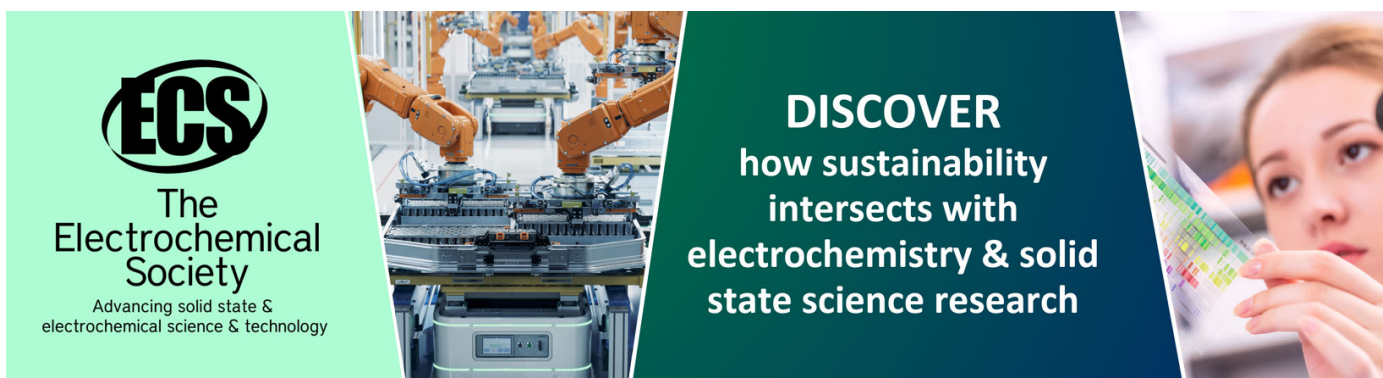
# Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3

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## Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3

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**ABSTRACT:** During the next Long Shutdown (LS3) of the LHC, planned for 2026, the innermost three layers of the ALICE Inner Tracking System will be replaced by a new vertex detector composed of curved ultra-thin monolithic silicon sensors. The R&D initiative on monolithic sensors of the CERN Experimental Physics Department, in cooperation with the ALICE ITS3 upgrade project, prepared the first submission of chip designs in the TPSCo 65 nm technology, called MLR1 (Multi Layer Reticule). It contains four different test structures with different process splits and pixel designs. These proceedings illustrate the first validation of the technology in terms of pixel performance and radiation hardness.

**KEYWORDS:** Particle tracking detectors; Radiation-hard detectors; Timing detectors; Front-end electronics for detector readout



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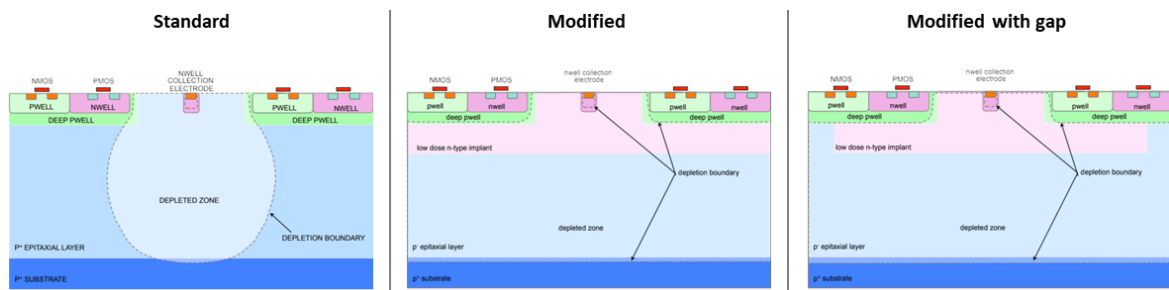
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## 1 Introduction

The ALICE Inner Tracking System upgrade (ITS3), planned for the LHC Long Shutdown 3 (2026–2028), will feature the substitution of the three inner layers of the current Inner Tracker (ITS2) in favour of three truly cylindrical sensors. The technology identified as a leading candidate to meet the requirements of the ITS3 is the TPSCo 65 nm process [1]. The reasons behind this choice are the fact that the ITS3 detector design foresees wafer-scale O ( $10\text{ cm} \times 30\text{ cm}$ ) sensors and the necessary wafer size is available in this technology node, giving access to large stitched sensors [2]. Furthermore, the sensors can be thinned down to  $< 50\text{ }\mu\text{m}$  and bent to 19, 25.2 and 31.5 mm curvature radius. In this technology, sensor optimization plays a crucial role, as already applied in the 180 nm CMOS imaging technology [3, 4].

The main sensor features are the presence of an octagonal-shaped  $n$ -well collection electrode with  $1.14\text{ }\mu\text{m}$  diameter and of a high-resistivity  $p$ -type epitaxial layer with a thickness  $\sim 10\text{ }\mu\text{m}$ , grown on top of a low-resistivity  $p$ -doped substrate. Full CMOS circuitry is located on devoted  $n$ -wells and  $p$ -wells, shielded by a deep  $p$ -well. Three different implant geometries were designed: standard, modified, and modified-with-gap, illustrated in figure 1. Because of the spherical shape of the  $pn$  junction, in the standard process it is very difficult to deplete the epitaxial layer over its full width, while in the modified one, by means of an additional low dose  $n$ -type implant, the  $pn$  junction from which the depletion starts is shifted more in depth in the sensor, allowing to reach a uniform and complete sensor depletion. The application of a higher reverse bias increases the depletion volume, keeping at the same time the collection electrode small, preserving a low capacitance. In the modified-with-gap process, a gap in the additional  $n$ -layer has been introduced near the pixel edge, in order to speed up the charge collection process thanks to an increased lateral electric field.

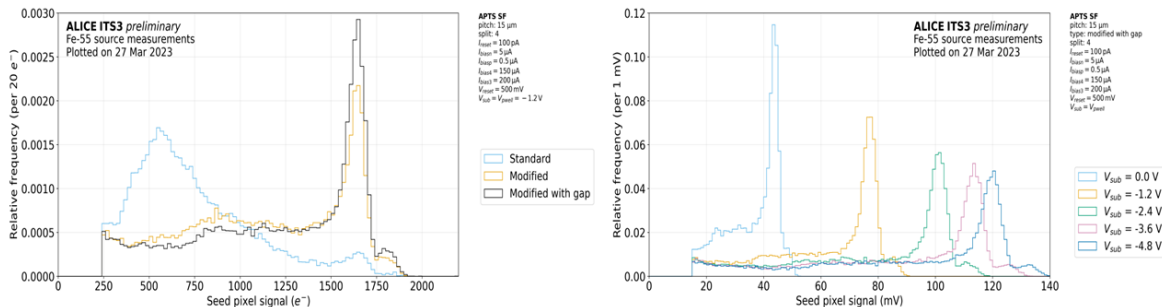


**Figure 1.** Three process variants implemented in the MLR1 chips.



modified-with-gap processes. In these process modifications, the charge is mainly collected by a single pixel, as it clearly appears from the Mn- $K_{\alpha}$  peak located  $\sim 1640$  e.

The effect of different applied reverse bias voltages can be observed in figure 3 (right), showing spectra for the modified-with-gap process. As a consequence of the increased reverse bias, the amplitude progressively increases as well, as can be noticed from the shift of the Mn- $K_{\alpha}$  peak, translating into a reduction of the input capacitance.



**Figure 3.** Distribution of collected charge for the standard, modified and modified-with-gap implant geometry (left) and collected charge distributions for the modified-with-gap process at different reverse biases (right).

#### 4 In-beam measurements

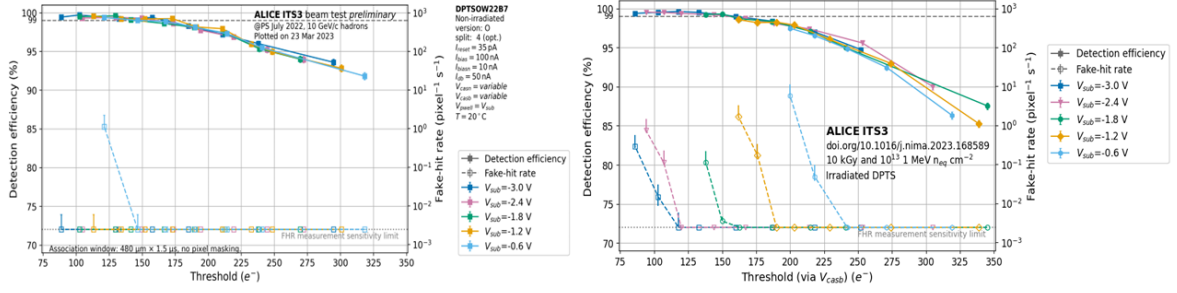
The second part of the characterization was performed at test beam facilities with minimum ionizing particles. The analysis is based on a reconstruction software [5] that fits General Broken Lines to clusters on the reference planes and, subsequently, by interpolating the tracks to the DUT,<sup>1</sup> associates or discards the tracks. Plenty of test beam campaigns have been completed starting from 2021 with the goal of measuring the detection efficiency and the fake-hit-rate<sup>2</sup> (FHR). Furthermore, also the sensor spatial and temporal resolutions were measured.

In-beam measurements conducted on the DPTS prototypes allowed the detection efficiency measurement for both non-irradiated and irradiated chips. In particular, figure 4 (left) shows the detection efficiency of a non-irradiated chip at different thresholds and considering a set of different reverse biases. Only for the lowest reverse bias of 0.6 V, a FHR above the measurement sensitivity limit is observed for a low threshold. This result ensures a wide operational range of the sensor featuring a detection efficiency above 99%.

By considering the detection efficiency of the chip irradiated to a combination of an ionizing dose of 10 kGy (TID) and a non-ionizing dose of  $1 \times 10^{13} \text{ 1 MeV n}_{\text{eq}} \text{ cm}^{-2}$  (NIEL) on figure 4 (right), it is possible to observe that by increasing the reverse bias, the onset of the measured FHR is offset to lower thresholds. This results in the preference of larger reverse bias voltages when operating the sensor at lower thresholds, with a wide operational margin at about 99% detection efficiency [6]. The aforementioned irradiation levels are of particular interest since they represent the posed requirements of the ALICE ITS3 project.

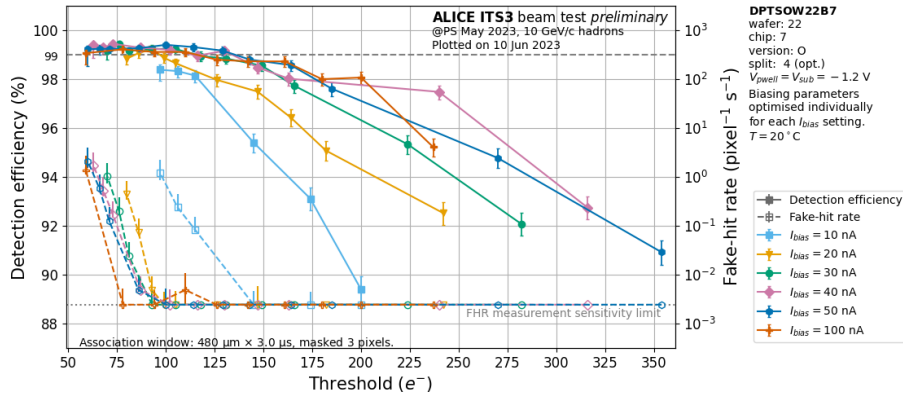
<sup>1</sup>Device under test.

<sup>2</sup>Number of hits per pixel and second in absence of external stimuli.



**Figure 4.** Detection efficiency and fake hit rate for a non irradiated DPTS chip (left) and for an irradiated DPTS at 10 kGy (TID) and  $1 \times 10^{13}$  1 MeV  $n_{eq}$   $cm^{-2}$  (NIEL) (right) as a function of the threshold. Different colors refer to different reverse bias voltages ( $V_{sub}$ ).

A relevant study carried out on the DPTS chip is related to the chip performance at different power consumption regimes. Figure 5 shows the DPTS detection efficiency with different  $I_{bias}$  currents and, as a consequence, with a different power consumption, being the  $I_{bias}$  current the main biasing current of the front-end [7]. Except for the  $I_{bias} = 10$  nA case, the efficiency reaches 99% or more for all the  $I_{bias}$  values and the power consumption estimation remains better than the target for the ALICE ITS3 (power consumption  $\sim 15$  mW  $cm^{-2}$  with  $I_{bias} = 30$  nA).

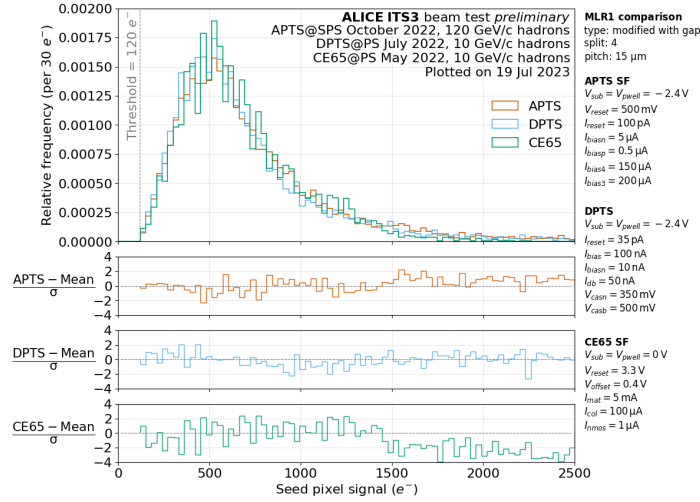


**Figure 5.** DPTS detection efficiency as a function of the threshold with different  $I_{bias}$  currents in the front-end circuit.

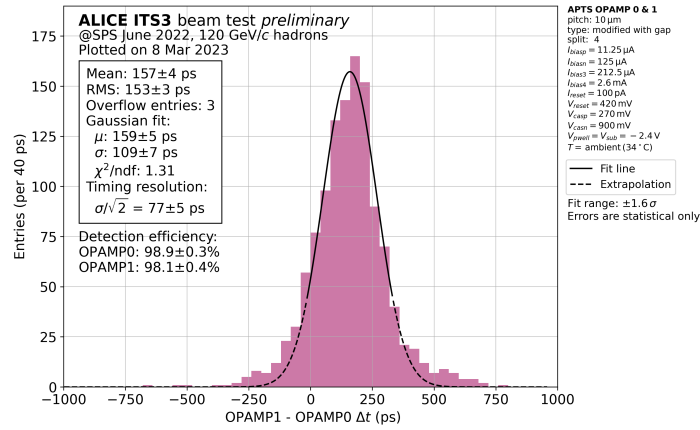
A comparison of three different prototypes belonging to the MLR1, tested with in-beam measurements is shown in figure 6. It illustrates the seed pixel signal distribution, in electrons, for APTS, CE65 and DPTS, all of them with a pixel pitch of 15  $\mu m$  and for the modified-with-gap process. One can observe that all the spectra are in agreement. In order to evaluate their compatibility, the difference among each test structure and their mean has been computed. The differences, divided by the uncertainty, provide a quantitative comparison (figure 6 bottom panels), leading to the conclusion of sensors compatibility within 2 sigma for APTS and DPTS and within 4 sigma for CE65 at high seed pixel signal.

The timing performance of the APTS-OA test structure was evaluated with in-beam measurements of two APTS-OA. Figure 7 shows the time residual distribution of the two sensors by applying a CFD technique with 10% threshold.

From the sigma of the gaussian fit, a timing resolution of  $(77 \pm 5)$  ps was determined.



**Figure 6.** Distributions of collected charge deposited by charge particles during in-beam measurements for APTS (red), DPTS (blue) and CE65 (green). Bottom plots show the difference between each DUT and the mean of the three, in units of sigma.



**Figure 7.** Time residual distribution of two APTS-OA with a superimposed gaussian fit to extract the timing resolution.

## 5 Conclusions

The TPSCo 65 nm technology has been validated for particle detection in terms of charge collection efficiency, detection efficiency, and radiation hardness. Extensive test campaigns were carried out with a  $^{55}\text{Fe}$  source on different prototypes and demonstrated a better charge collection performance for the modified-with-gap process, which suppresses charge sharing. Multiple in-beam measurements showed a detection efficiency above 99% for a wide range of working points and a radiation hardness within the requirements of the ALICE ITS3. Finally, a timing resolution  $\sim 77\text{ ps}$  was measured for the APTS-OA sensor.

## Acknowledgments

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## References

- [1] Tower Partners Semiconductor Co., <http://www.towersemi.com/>.
- [2] L. Musa, *Letter of Intent for an ALICE ITS Upgrade in LS3*, CERN-LHCC-2019-018, LHCC-I-034, CERN, Geneva (2019) [DOI:10.17181/CERN-LHCC-2019-018].
- [3] W. Snoeys et al., *A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance*, *Nucl. Instrum. Meth. A* **871** (2017) 90.
- [4] M. Munker et al., *Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance*, *2019 JINST* **14** C05013 [arXiv:1903.10190].
- [5] J. Kröger, S. Spannagel and M. Williams, *User Manual for the Corryvreckan Test Beam Data Reconstruction Framework, Version 1.0*, arXiv:1912.00856.
- [6] G.A. Rinella et al., *Digital pixel test structures implemented in a 65 nm CMOS process*, *Nucl. Instrum. Meth. A* **1056** (2023) 168589 [arXiv:2212.08621].
- [7] F. Piro et al., *A Compact Front-End Circuit for a Monolithic Sensor in a 65-nm CMOS Imaging Technology*, *IEEE Trans. Nucl. Sci.* **70** (2023) 2191.