On the Damping of Ringing Affecting Power Transistors by Means of Active Gate Drivers

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Erica Raviola, *Member, IEEE*, Franco Fiori, *Member, IEEE*

***Abstract*—Fast power transistors require a tight control of their switching trajectory to exploit them at full speed, without degrading reliability and delivered electromagnetic emission figures of merit. By using active gate drivers in place of conventional ones, the switching trajectory can be shaped to reduce current and voltage overshoots, as well as the amplitude of oscillations. However, the tuning of such drivers is still an open issue. This paper investigates the damping of oscillations by means of active gate drivers, and proposes a method to tune them *a-priori*. The target switching waveforms are evaluated by means of non-linear damping elements in simulation, easing the tuning procedure. The proposed method was assessed on a digital active gate driver, providing the initial set-point for the adaptive controller. The convergence time measured experimentally was found to be as low as $50\,\mu s$ for the overall load current range, whilst not affecting the conversion efficiency of the dc-dc converter exploited as test case.**

***Index Terms*—Active Gate Driver, AGD tuning, optimization, switching waveforms, oscillations, power transistor.**

I. Introduction

Efforts in technological processes have been made to increase the switching speed of power transistors. With the rapid uptake of fast power switches, figures of merit such as efficiency, reliability and Electro-Magnetic Emission (EME) are severely affected by phenomena taking place during switching transients [1]. In hard-switched power converters, the commutations of such fast transistors are typically triggered by a digital controller through a pulse width modulator. As the modulator itself may not be able to drive the power transistor, gate drivers are usually placed in between the controller and the power switch. In such a way, the modulator-generated pulses are matched with the gate-source voltage required to turn on and turn off the power switch. Both research and commercial gate drivers presented in the last years included more and more features to optimize and protect the driven switches. Optimal dead-time tracking, shoot-through protection, advanced crosstalk suppression, active clamping module are some of the functions gate drivers are nowadays provided with [2]–[5].

As far as fast power switches are concerned, their fast commutations may result in overshoots affecting the drain current and the drain-source voltage, worsening both the EME and the reliability figures of merit. Moreover, oscillations can be superimposed onto the switching waveforms, resulting in peaks in the frequency spectra [6]. As the switching current and voltage waveforms are usually considered the primary source of EME, such peaks are found in the spectra of conducted and radiated emission as well [7]. Such an issue can be mitigated only in part by increasing the gate resistance of conventional drivers (CGDs) to limit dv/dt and di/dt, which results in some reduction of overshoots and oscillations [8].

To have a better control over the switching trajectory of power transistors, Active Gate Drivers (AGDs) have been proposed to overcome the limitations of CGDs. AGDs can modulate their driving strength, e.g., the output resistance, to slow down and/or speed up some portions of the transients. As a result, the drain current and the drain source voltage waveforms can be shaped by intervening at the gate and source terminals of the power transistor. Neither extra components in series with nor in parallel to the driven switch are therefore required, nor the layout of power components has to be modified. Several beneficial outcomes from using AGDs were reported, amongst which controlled slew-rate [9], overshoots and EME reduction [10], [11], mitigation of the gate-source ringing in GaN transistors [12], frequency-selective EME reduction [13] and crosstalk suppression [14]. Even though AGDs were not primarily intended to damp oscillations, they were found to reduce the ringing effectively in several works [15]–[17].

An open issue when dealing with AGDs is their tuning, meaning to find the modulation profile which optimizes the switching trajectory of the driven transistor. Indeed, the modulation profile determines how the strength of the AGD changes during transients, both in terms of amplitude and timing. Such a profile is usually identified by a set of variables, which are referred to as AGD parameters. A non properly tuned AGD may degrade significantly the switching performance of the driven transistor, as reported in [18]. Focusing on digital AGDs, i.e., drivers in which the modulation profile is a constant-piecewise function disciplined by a digital controller, several solutions have been proposed in literature to address their tuning. In [19], [20], the modulation profile is obtained by a model estimator, i.e., a set of equation describing the switching trajectory, which is combined with the parameters of the driven transistor. Solutions based on extensive measurement campaigns [21] and pre-extrapolated relations [22] were reported as well. These methods address AGDs in which the modulation profile can be finely adjusted, meaning that the search space is characterized by a large number of combinations, but they may not be effective when applied in practical cases due to the spread of physical parameters of the driven transistor.

Conversely, adaptive AGDs, such as [23]–[25], can cope with the issue of parameter spread and operating condition variations. In such kind of drivers, the values of the AGD

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parameters are iteratively adapted by an on-board controller on the basis of measured fed-back quantities. Reference [24] exploited a PI controller, whether [25] used a microcontroller implementing the steepest descend minimization algorithm. Although adaptive AGDs are a promising solution, some aspects need to be throughly addressed to enable their widespread application in practical cases. Indeed, adaptive AGDs require an initial guess of the AGD parameters to allow the optimization method to converge within a short time. This aspect is crucial, especially when exploiting local optimization methods, as an initial set-point too far from the minimum may result in a high convergence time, or, in the worst case, in not finding a solution. According to the authors' knowledge, a strategy to determine the modulation profile of AGDs *a-priori*, thereby avoiding time-consuming trial and error approaches, has not yet been presented. Furthermore, the use of AGDs to damp oscillations triggered by fast power transistors has not been investigated. This aspect requires further clarification, as oscillations degrade both the EME and reliability figures of merit, while preventing the exploitation of power transistors at their full speed.

This work proposes a method to tune the modulation profile of AGDs with the aim of avoiding oscillations. To this purpose, a non-linear model is firstly presented, in which oscillations can be avoided by inserting a virtual non-constant dissipative element in place of the power transistor. This allows one to get the switching trajectory the transistor should follow to critically damp oscillations triggered by its fast commutations. Then, a method to tune the AGD is presented in simulation, which allows one to get the switching trajectory previously obtained. With respect to previous works dealing with the ringing issue, in this work the power transistor itself is exploited as a non-linear dissipative element, allowing one to damp oscillations with a non-constant virtual resistance. Moreover, the proposed method eases the tuning of the AGD parameters, as it provides the target voltage and current waveforms a-priori.

The remainder of the paper is organized as follows: in Sect. II, a theoretical analysis is presented, and virtual non-linear components are introduced. Section III validates the previous analysis in simulation, and a method to determine the initial set of AGD parameters is presented in Sect. IV. Experimental results are given in Sect. V, and concluding remarks are in Sect. VI.

II. Circuit damping

This section discusses the ringing issue affecting hard-switched power transistors, and presents an equivalent model to analyze the oscillations triggered at the turn on and at the turn off of power transistors. An analytical analysis is then carried out to determine the conditions under which oscillations can be damped by virtual dissipative elements in place of the power transistor. The results obtained from such an analysis will be later exploited by the proposed AGD tuning method.

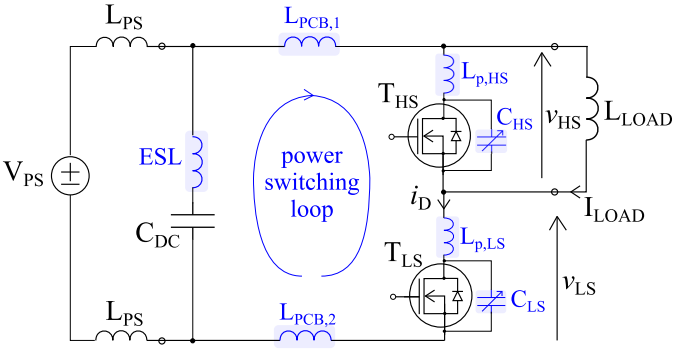

Fig. 1. Hard-switched half bridge with an inductive load used to analyze the oscillations at the turn on and the turn off of transistor $T_{\rm LS}$. Parasitic inductances and capacitances included in the power switching loop have been enclosed by boxes to be found at glance.

A. Background

The circuit shown in Fig. 1 can be exploited to analyze the oscillations triggered by fast power transistors without loss of generality. The high side ($T_{\rm HS}$) and the low side ($T_{\rm LS}$) transistors are switched on and off complementary to provide the load ($L_{\rm LOAD}$) with the current $I_{\rm LOAD}$. This circuit is supplied by an external $V_{\rm PS}$, and it includes one or more input capacitors ($C_{\rm DC}$), which are placed close to the hard switched transistors, to provide the high-frequency current during transients. With the load current flowing as shown in Fig. 1, i.e., $I_{\rm LOAD} > 0$, the fast commutations of the low side transistor may cause the stray inductance of the power switching loop to resonate with the output capacitance of $T_{\rm HS}$ ($T_{\rm LS}$) at the $T_{\rm LS}$ turn on (turn off). Conversely, with $I_{\rm LOAD} < 0$, the commutations of the high side transistor may trigger the resonance between the stray inductance and the $T_{\rm HS}, T_{\rm LS}$ output capacitances [26]. The corresponding oscillations are typically slightly damped, meaning that voltage and current waveforms are affected by significant overshoots. The values of parasitic inductance and capacitances, as well as those of the load current and of the supply voltage, affect the frequency, the amplitude, and the conditions under which oscillations are damped.

Besides the aforementioned passive and active devices, Fig. 1 is complemented with the parasitic inductances and capacitances included in the power switching loop. As far as the stray inductance of the power loop is concerned, it is related to the interconnections between $T_{\rm HS}$, $T_{\rm LS}$ and $C_{\rm DC}$, as well as to the packaging of such components. With $2L_{\rm PS} >> ESL$, the overall parasitic inductance can be approximated as

$$L_{\rm LOOP} \approx L_{\rm PCB,1} + L_{\rm PCB,2} + ESL + L_{\rm p,HS} + L_{\rm p,LS}, \quad (1)$$

where $L_{\rm PCB,1-2}$ are the stray inductance due to PCB connections, which can be estimated either by analytical formula or by a 2D/3D EM solver [27], ESL is the equivalent series inductance of $C_{\rm DC}$, and $L_{\rm p,LS}, L_{\rm p,HS}$ are those of the transistor packaging. Regarding the output capacitances of the switches, i.e., $C_{\rm LS}$ and $C_{\rm HS}$, their are typically non linear, meaning that their values depend on the voltage applied. For instance, with the high-side switch being a power transistor as shown in Fig. 1, $C_{\rm HS}$ is the MOSFET drain–source capacitance in parallel to

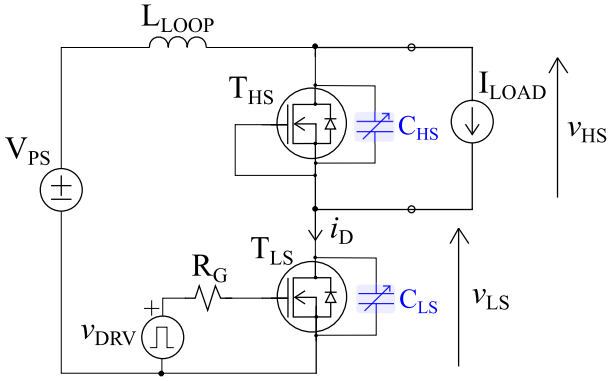

Fig. 2. Simplified model of the half bridge shown in Fig. 1 which is exploited to analyze the $T_{\rm LS}$ commutations.

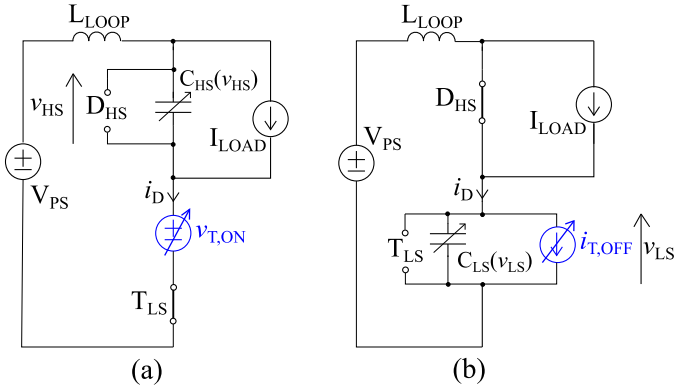

Fig. 3. On the left (right), model of the circuit in Fig. 2 once the oscillations at the $T_{\rm LS}$ turn on (turn off) are triggered. The non-linear $v_{\rm T,ON}$ ($i_{\rm T,OFF}$) source is included to damp the $L_{\rm LOOP}-C_{\rm HS}$ ($L_{\rm LOOP}-C_{\rm LS}$) resonance.

the body diode capacitance. The value of such a capacitance follows an exponential relation, which depends on the barrier potential and on the applied reverse voltage [28].

The analysis of ringing is usually carried out referring to a second-order equivalent model, with constant values of inductance and capacitance. In addition, previous works assume $T_{\rm LS}$ to be in deep triode for the oscillations taking place at its turn on, and to be switched off for those at its turn off [29]. In both cases, the transistor does not provide any damping to the corresponding resonance. Although such a simplified model is accurate enough to estimate the oscillation frequency and to size the snubber components, it may not be suited when tuning the modulation profile of an AGD. For the sake of simplification, the analysis presented in the remainder of this Sect. neglects the $T_{\rm LS}$ contribution, and discusses the oscillations damping by means of non-linear dissipative elements in place of the power transistor. Then, in Sect. III, the $T_{\rm LS}$ contribution to the oscillation damping is accounted for, and the target switching trajectory of $T_{\rm LS}$ can be obtained. In such a way, the presented analysis is independent from the type (Si, SiC or GaN) and the physical parameters of the actual power transistor.

The circuit shown in Fig. 1 can be simplified in the model shown in Fig. 2 to discuss the $T_{\rm LS}$ turn on and the turn off. The input supply network, including the DC-link, has been replaced by the ideal voltage source $V_{\rm PS}$, which is connected in series with the overall parasitic inductance of the power loop ($L_{\rm LOOP}$), evaluated as given in (1). This simplification is justified as high frequency components of the switching current are provided by $C_{\rm DC}$. Additionally, the load inductance $L_{\rm LOAD}$ from Fig. 1 is substituted with a constant current source ($I_{\rm LOAD}$) in Fig. 2, as variations in load current are much slower than the phenomena observed during transients. Regarding the $T_{\rm LS}$ commutations, the high side transistor is driven off steadily to prevent cross-conduction. Consequently, the gate of $T_{\rm HS}$ is tied to its source in the simplified model. The output capacitances $C_{\rm LS}$ and $C_{\rm HS}$ of the power switches have been highlighted in model to be identified at a glance.

B. Series circuit (turn on)

Referring to the simplified model in Fig. 2, the turn on of $T_{\rm LS}$ is triggered by a positive voltage step of $v_{\rm DRV}$. When the gate source voltage of $T_{\rm LS}$ exceeds its threshold value, a positive drain current $i_{\rm D}$ begins to flow. However, as long as $i_{\rm D} < I_{\rm LOAD}$, the load current flows through the body diode of the high-side transistor, meaning that $T_{\rm HS}$ is recirculating. When the current in $T_{\rm LS}$ reaches $I_{\rm LOAD}$, the body diode of $T_{\rm LS}$ turns off. Consequently, the model shown in Fig. 2 can be further simplified in that shown in Fig. 3(a). With the $T_{\rm HS}$ body diode turned off, only the non linear voltage-dependent capacitance $C_{\rm HS}$ is considered. Assuming the low side transistor to be entirely turned on by the time $i_{\rm D} = I_{\rm LOAD}$, its channel resistance is neglected and $T_{\rm LS}$ is substituted with a short circuit in Fig. 3(a). As the voltage drop across $C_{\rm HS}$ increases from 0 V to $V_{\rm PS}$, the $C_{\rm HS}-L_{\rm LOOP}$ resonant circuit can be excited. The behavioral voltage source, denoted as $v_{\rm T,ON}$ in Fig. 3(a), is here introduced to damp the $C_{\rm HS}-L_{\rm LOOP}$ resonance. Such a virtual non-linear component, which is connected in series with $L_{\rm LOOP}$ and $C_{\rm HS}$, damps the resonance without affecting the circuit behavior once the transient has ended. To this purpose, $v_{\rm T,ON}$ is defined as

$$v_{\rm T,ON}(t) \widehat{=} R_{\rm X}(v_{\rm HS}(t)) \cdot (i_{\rm D}(t) - I_{\rm LOAD}). \tag{2}$$

The virtual resistance in (2) is a function of $v_{\rm HS}$, meaning that the $R_{\rm X}$ value changes as $C_{\rm HS}$ charges to $V_{\rm PS}$. Depending on the $R_{\rm X}(v_{\rm HS}(t))$ expression, the resulting $i_{\rm D}$ and $v_{\rm HS}$ waveforms can vary. Therefore, the function $R_{\rm X}$ can be thought as a degree of freedom at disposal to attain a given commutation speed whilst damping oscillations. It is worth noting that once the transient has ended, $i_{\rm D}(+\infty) = I_{\rm LOAD}$ and therefore $v_{\rm T,ON} = 0$, provided that $R_{\rm X}(V_{\rm PS})$ takes a finite value. The system shown in Fig. 3(a) can be described by two first-order non-linear differential equations. By choosing as state variables ($\boldsymbol{x}$) the current flowing in $L_{\rm LOOP}$ ($i_{\rm D}$) and the voltage drop across the high side capacitance ($v_{\rm HS}$), it results

$$\begin{cases} \frac{\partial i_{\rm D}(t)}{\partial t} &= \frac{V_{\rm PS}}{L_{\rm LOOP}} - \frac{v_{\rm HS}(t)}{L_{\rm LOOP}} - \frac{R_{\rm X}(v_{\rm HS})(i_{\rm D}(t)-I_{\rm LOAD})}{L_{\rm LOOP}} \\ \frac{\partial v_{\rm HS}(t)}{\partial t} &= \frac{i_{\rm D}(t)}{C_{\rm HS}(v_{\rm HS})} - \frac{I_{\rm LOAD}}{C_{\rm HS}(v_{\rm HS})} \end{cases}. \tag{3}$$

The system starts from $(i_{\rm D}, v_{\rm HS}) = (I_{\rm LOAD}, 0)$ and converges to the unique equilibrium point, which is $\boldsymbol{x_{0,ON}} = (I_{\rm LOAD}, V_{\rm PS})$. The analysis of non-linear dynamic systems, as (3), can be carried out referring to the linearized approximation

around the equilibrium points, provided that the component functions of the system are continuous and have continuous partial derivatives everywhere [30]. In this case, the type of equilibrium points, i.e., saddle, sink or source nodes, which in turn determines the trajectories of the state variables in the phase plane, is determined by the eigenvectors and the eigenvalues of the Jacobian matrix evaluated in the critical points.

The Jacobian matrix ($\boldsymbol{J}$) of (3) at $\boldsymbol{x_{0,ON}}$ is equal to

$$\boldsymbol{J}(\boldsymbol{x_{0,ON}}) = \begin{pmatrix} -\frac{R_{\rm X}(V_{\rm PS})}{L_{\rm LOOP}} & -\frac{1}{L_{\rm LOOP}} \\ \frac{1}{C_{\rm HS}(V_{\rm PS})} & 0 \end{pmatrix}. \tag{4}$$

Indeed, the terms $dR_{\rm X}/dv_{\rm HS}$ and $dC_{\rm HS}/dv_{\rm HS}$ do not appear in $\boldsymbol{J}$ as $i_{\rm D} = I_{\rm LOAD}$ at $\boldsymbol{x_{0,ON}}$. The $\boldsymbol{J}$ eigenvalues ($\lambda_{1,2}$) can be evaluated from the roots of the characteristic polynomial, i.e.,

$$\lambda^2 + \frac{R_{\rm X}(V_{\rm PS})}{L_{\rm LOOP}} + \frac{1}{L_{\rm LOOP}C_{\rm HS}(V_{\rm PS})} = 0. \tag{5}$$

To have a sink improper node, which would correspond to a critical damping condition in a linear system, it should be $\lambda_1 = \lambda_2 < 0$, resulting in

$$R_{\rm X}(V_{\rm PS}) = 2\sqrt{\frac{L_{\rm LOOP}}{C_{\rm HS}(V_{\rm PS})}}. \tag{6}$$

This result states that, even though $R_{\rm X}$ and $C_{\rm HS}$ may not be constant along the trajectory, as they depend on $v_{\rm HS}$, it is sufficient that the equivalent damping resistance is equal to (6) around a neighborhood of $\boldsymbol{x_{0,ON}}$. This result extends that of a classic RLC series circuit, meaning that oscillations can be damped by a non-constant resistance as well.

C. Parallel circuit (turn off)

Referring to the circuit in Fig. 2, the $T_{\rm LS}$ turn off is triggered by driving $v_{\rm DRV}$ low. During this transient, $v_{\rm LS}$ increases, and when it reaches $V_{\rm PS}$, the high side diode turns on, therefore short circuiting the load current source and its output capacitance $C_{\rm HS}$. For the analysis of oscillations triggered at the $T_{\rm LS}$ turn off, the circuit shown in Fig. 2 can be further simplified in the model reported in Fig. 3(b). The low side transistor is assumed to be off when $v_{\rm LS} = V_{\rm PS}$, and it is substituted with its output capacitance $C_{\rm LS}$. Indeed, $C_{\rm LS}$ is already charged to $V_{\rm PS}$, but the parasitic inductance should discharge from $I_{\rm LOAD}$ to 0 A, as the load current is now flowing through the high side diode. Therefore, the oscillations at the turn off are triggered by the $i_{\rm D}$ current step. To damp the $L_{\rm LOOP} - C_{\rm LS}$ resonance, the behavioral current source $i_{\rm T,OFF}$ was inserted in parallel to the low side output capacitance, as shown in Fig. 3(b). Such current source is defined as

$$i_{\rm T,OFF}(t) \widehat{=} \frac{v_{\rm LS}(t) - V_{\rm PS}}{R_{\rm Y}(i_{\rm D}(t))}, \tag{7}$$

where $R_{\rm Y}$ is the non-linear damping resistance. As for $v_{\rm T,ON}$, $i_{\rm T,OFF}$ is intended to damp oscillations with a non-constant resistance, whose value change as $i_{\rm D}$ decreases from $I_{\rm LOAD}$ to zero. Also in this case, the contribution of $i_{\rm T,OFF}$ is nulled once the turn off transient has ended, i.e., $v_{\rm LS}(t) = V_{\rm PS}$.

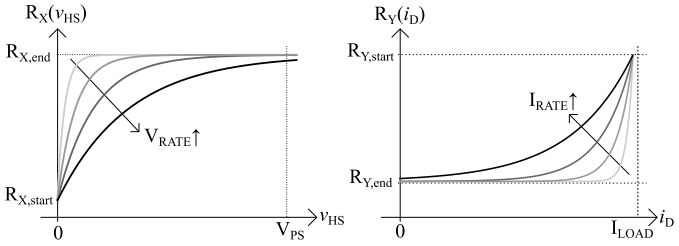

Fig. 4. Exponential functions $R_{\rm X}(v_{\rm HS})$ (on the left) and $R_{\rm Y}(i_{\rm D})$ (on the right) exploited to damp oscillations with a non-constant virtual resistance.

The resulting non linear system can be fully described by choosing as state variables the current in $L_{\rm LOOP}$ ($i_{\rm D}$) and the voltage across $C_{\rm LS}$ ($v_{\rm LS}$), as

$$\begin{cases} \frac{\partial i_{\rm D}(t)}{\partial t} &= \frac{V_{\rm PS}}{L_{\rm LOOP}} - \frac{v_{\rm LS}(t)}{L_{\rm LOOP}} \\ \frac{\partial v_{\rm LS}(t)}{\partial t} &= \frac{i_{\rm D}(t)}{C_{\rm LS}(v_{\rm LS})} - \frac{(v_{\rm LS}(t) - V_{\rm PS})}{R_{\rm Y}(i_{\rm D})C_{\rm LS}(v_{\rm LS})} \end{cases}. \tag{8}$$

This system evolves from $(i_{\rm D}, v_{\rm LS}) = (I_{\rm LOAD}, V_{\rm PS})$ to the equilibrium point $\boldsymbol{x_{0,OFF}} = (0, V_{\rm PS})$. The Jacobian of the linearized system around the critical point $\boldsymbol{x_{0,OFF}}$ is therefore

$$\boldsymbol{J}(\boldsymbol{x_{0,OFF}}) = \begin{pmatrix} 0 & -\frac{1}{L_{\rm LOOP}} \\ \frac{1}{C_{\rm LS}(V_{\rm PS})} & -\frac{1}{R_{\rm Y}(0)C_{\rm LS}(V_{\rm PS})} \end{pmatrix}, \tag{9}$$

and the corresponding eigenvalues can be evaluated as

$$\lambda_{1,2} = -\frac{1}{2R_{\rm Y}(0)C_{\rm LS}(V_{\rm PS})} \pm \frac{1}{2}\sqrt{\frac{1}{R_{\rm Y}^2(0)C_{\rm LS}^2(V_{\rm PS})} - \frac{4}{C_{\rm LS}(V_{\rm PS})L_{\rm LOOP}}} \tag{10}$$

By imposing $\lambda_{1,2}$ to be purely real, equal and negative, i.e., the critical point is a sink improper node, it results

$$R_{\rm Y}(0) = \frac{1}{2}\sqrt{\frac{L_{\rm LOOP}}{C_{\rm LS}(V_{\rm PS})}}. \tag{11}$$

Similar to the $R_{\rm X}$ case, the final value of $R_{\rm Y}$ should be that in (11) to avoid the triggering of oscillations. Also in this case, this result extends the classic theory for linear RLC parallel circuit, meaning that the damping resistance is not required to be constant to avoid ringing at the turn off of $T_{\rm LS}$.

D. How to choose the $R_{\rm X}, R_{\rm Y}$ functions

From the previous analysis, some constrains the functions $R_{\rm X}(v_{\rm HS})$ and $R_{\rm Y}(i_{\rm D})$ need to satisfy to damp the oscillations can be pointed out. Such functions should both belong to $\mathbb{C}^1$ to linearize the non-linear systems (3) and (8) around their respective equilibrium points. Moreover, it was found that $R_{\rm X}(v_{\rm HS})$ and $R_{\rm Y}(i_{\rm D})$ should equal (6) and (11) in a neighborhood of $\boldsymbol{x_{0,ON}}$ and $\boldsymbol{x_{0,OFF}}$, respectively. By denoting with $R_{\rm X,end}$ and $R_{\rm Y,end}$ the right-hand side of (6), (11), one can choose $R_X = R_{\rm X,end}$ and $R_Y = R_{\rm Y,end}$. In such a way, the virtual damping resistance is constant, as for classic linear RLC circuits. Alternatively, one could also exploit non-constant R_X, R_Y values to attain non oscillating

waveforms. However, not every $\mathbb{C}^1$ function meeting (6) or (11) is suitable. The candidate function models a dissipative element, meaning that it should be $R_{\rm X}(v_{\rm HS}) \geq 0, \forall v_{\rm HS} \geq 0$ and $R_{\rm Y}(i_{\rm D}) \geq 0, \forall i_{\rm D} \geq 0$ to avoid the energy bouncing from $L_{\rm LOOP}$ and the parasitic capacitance. To minimize the sensitivity of $R_{\rm X}, R_{\rm Y}$ functions to $R_{\rm X,end}$ and $R_{\rm Y,end}$ around their respective critical points, it should be

$$\left.\frac{\partial R_{\rm X}}{\partial v_{\rm HS}}\right|_{V_{\rm PS}} = 0, \qquad \left.\frac{\partial R_{\rm Y}}{\partial i_{\rm D}}\right|_{0} = 0. \tag{12}$$

Regarding the turn on, with $R_{\rm X} < R_{\rm X,end}$ for $v_{\rm HS} << V_{\rm PS}$, the rise time of $v_{\rm HS}$ will be lower than that with constant $R_{\rm X}$, as the transient is speed up in the first part. Similarly, with $R_{\rm Y} > R_{\rm Y,end}$ for $i_{\rm D} >> 0$, the fall time of $i_{\rm D}$ will be lower than that with constant $R_{\rm Y}$ as well.

Amongst the several functions satisfying the above constrains, this work focuses on exponential functions as those shown in Fig. 4. More precisely, the analytical expression for R_X is

$$R_{\rm X}(v_{\rm HS}) = R_{\rm X,end} + (R_{\rm X,start} - R_{\rm X,end})e^{-\frac{v_{\rm HS}}{V_{\rm RATE}}}, \tag{13}$$

and that for R_Y is

$$R_{\rm Y}(i_{\rm D}) = R_{\rm Y,end} + (R_{\rm Y,start} - R_{\rm Y,end})e^{-\frac{I_{\rm LOAD}-i_{\rm D}}{I_{\rm RATE}}}. \tag{14}$$

The selected constrains are met by (13) and (14), and the shaping of the switching waveforms can be achieved by selecting proper values for $R_{\rm X,start}, V_{\rm RATE}$ and $R_{\rm Y,start}, I_{\rm RATE}$. Indeed, a certain switching trajectory is identified once those parameters are fixed, meaning that switching speed and overshoots can be adjusted whilst damping the oscillations. It is worth noticing that not each $R_{\rm X,start}, V_{\rm RATE}$ combination is suitable, as high $V_{\rm RATE}$ values may prevent R_X for reaching $R_{\rm X,end}$ at $v_{\rm HS} = V_{\rm PS}$. By imposing $R_X(V_{\rm PS}) \geq R_{\rm X,end} - \Delta R$, with ΔR equals to a few percent of $R_{\rm X,end}$, one can get

$$\frac{V_{\rm PS}}{V_{\rm RATE}} \geq \ln(R_{\rm X,end} - R_{\rm X,start}) - \ln(\Delta R). \tag{15}$$

A similar condition can be derived for $R_{\rm Y}$ by posing $R_Y(0) \leq R_{\rm Y,end} - \Delta R$.

III. Circuit analysis

The analysis presented so far is based on the assumption that the low side power transistor is in deep triode at the triggering of the turn on oscillations, and that it is switched off when the ringing at the turn off occurs. This means that the actual switching trajectory of the low-side transistor was neglected, as $T_{\rm LS}$ was not providing any damping to the LC resonance. However, depending on the load current, the supply voltage, and the values of $L_{\rm LOOP}, C_{\rm HS}$, and $C_{\rm LS}$, $T_{\rm LS}$ can be still in saturation when oscillations are triggered [26]. Consequently, the power transistor itself may provide some damping in the form of dissipated power before the dynamic systems at the turn on (see (3)) and at the turn off (see (8)) reach their respective equilibrium points. To account for the damping provided by the low side transistor itself when it is in saturation, the virtual dissipative voltage source at the turn on should be modified as

$$v'_{\rm T,ON}(t) = v_{\rm T,ON}(t) - v_{\rm DS}(t), \tag{16}$$

where v_{DS} is the voltage drop across the low side transistor. Similarly, at the turn off, the current source should account for the channel current in the transistor, which can be evaluated as the total current entering the drain terminal minus that flowing in the output capacitance. Therefore, the expression for $i_{\rm T,OFF}$ should be modified as

$$i'_{\rm T,OFF}(t) = i_{\rm T,OFF}(t) - \left(i_{\rm D}(t) - C_{\rm LS}(V_{\rm PS})\frac{dv_{\rm DS}(t)}{dt}\right). \tag{17}$$

By modifying (2), (7) in (16), (17), the power transistor is treated like a black box, meaning that it is not required to know its physical parameters or models. In such a way, the proposed method is independent also from the type, i.e., Si, SiC or GaN, of the power transistor.

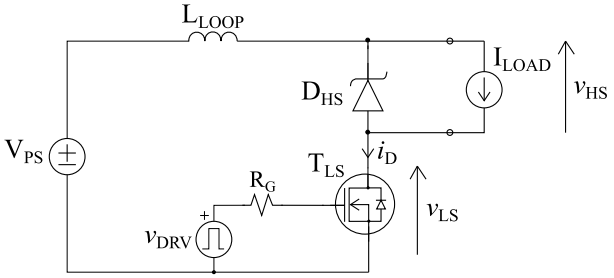

Fig. 5. Simulation setup exploited as test case. The models of the high side diode and of the low side power transistor are those provided by the manufacturer.

TABLE I
Parameters of the simulated circuit

Parameter	Value
Parasitic inductance ($L_{\rm LOOP}$)	16 nH
Input supply voltage ($V_{\rm PS}$)	48 V
Load current ($I_{\rm LOAD}$)	5 A
Gate resistance ($R_{\rm G}$)	10 Ω
High side output capacitance ($C_{\rm HS}$) at $V_{\rm PS}$	1.2 nF
Low side output capacitance ($C_{\rm LS}$) at $V_{\rm PS}$	0.9 nF

In order to discuss the implementation of (16) and (17), as well as the AGD tuning method, the circuit shown in Fig. 5 is considered as test case. Such power circuit can be exploited to simulate the $T_{\rm LS}$ commutations, and it is characterized by the parameters reported in Table I. Such values are those of the DC-DC converter exploited later to validate the proposed AGD tuning method experimentally. Simulations were carried out considering the spice models provided by manufacturers for the low side power transistor and for the high side Schottky diode. The parasitic inductance $L_{\rm LOOP}$ was estimated according to (1). The nominal values of the $C_{\rm LS}, C_{\rm HS}$ parasitic capacitances, which were obtained from the data-sheet of [31] for $T_{\rm LS}$ and [32] for $D_{\rm HS}$, are reported in Table I as well.

To include $v'_{\rm T,ON}$ and $i'_{\rm T,OFF}$ defined as (16) and (17) in

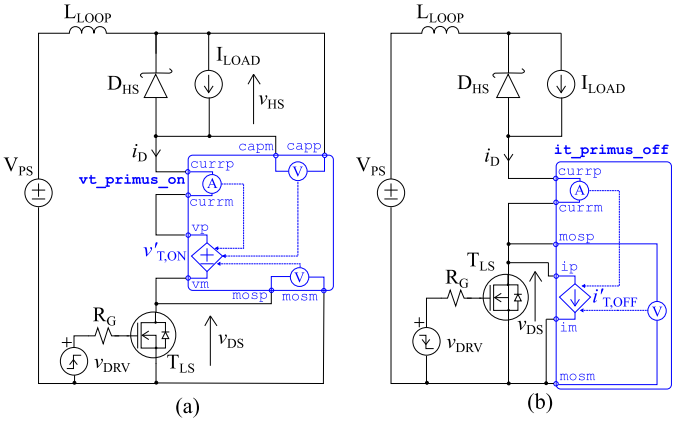

Fig. 6. Circuit shown in Fig. 5 complemented with (a) the behavioral block `vt_primus_on`, and with (b) the behavioral block `it_primus_off`.

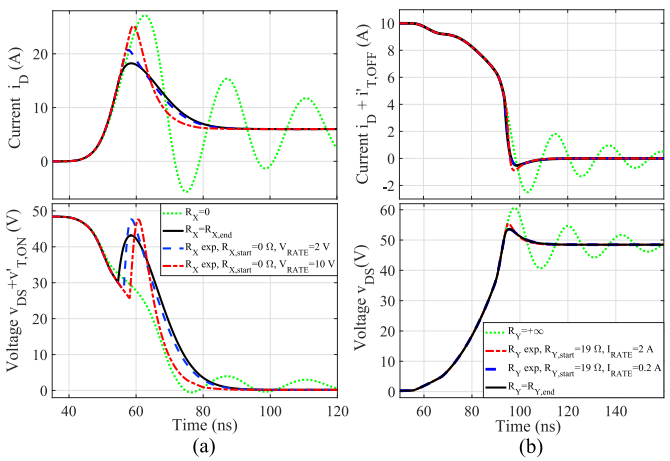

Fig. 7. Waveforms obtained from a time domain simulations of the circuit shown in Fig. 6 with (solid, dashed and dot-dashed) and without (dotted lines) the controlled sources for (a) the turn on and (b) the turn off. Oscillations are effectively damped, and the corresponding waveforms are slightly different depending on the values of $V_{\mathrm{RATE}}, R_{\mathrm{start}}$.

a circuit simulator, a behavioral analog description language, i.e., Verilog-A [33], should be exploited to describe such nonlinear components. Verilog-A was preferred as it allows for declaring instances which can be customized by using parameters, for probing the voltage across and the current flowing into ports, as well as for conditional statements. Two verilog-A modules, named `vt_primus_on` and `it_primus_off` have been inserted the circuit shown in Fig. 5 as shown in Fig. 6(a) and (b) to damp oscillations at the turn on and turn off, respectively. The netlists of such behavioral components and a flowchart depicting the algorithm executed in such blocks are reported in Appendix I. Regarding the T_{LS} turn on (see Fig. 6(a)), the `vt_primus_on` module is provided with three inputs ports, which are denoted with voltmeter or ammeter symbols, and one output port, which is identified by a dependent voltage source. More precisely, port `capp-capm` senses the v_{HS} voltage, port `currp-currm` the i_{D} current and port `mosp-mosm` the v_{DS}. The voltage source $v'_{T,ON}$, which is defined as (16), is placed in series with the power transistor. Regarding the turn off transient, the circuit including the `it_primus_off` module is shown in Fig. 6(b). The input port `currp-currm` senses the i_{D} current, port `mosp-mosm` the v_{DS} voltage, and the $i'_{\mathrm{T;OFF}}$ current source is described by port `ip-im`, and it is placed in parallel to the power transistor. Such blocks can be customized by changing the values of parameters $R_{\mathrm{X,start}}, R_{\mathrm{X,end}}$ and V_{RATE} to adapt to the particular power circuit to be simulated. Such blocks are independent from the type of power transistors, as they exploit the sensing ports to detect automatically the triggering of oscillations and to estimate the damping required.

The effectiveness of such modules in damping the oscillation was assessed using Spectre, a spice-like simulator [34]. The T_{LS} transistor is driven in Fig. 6(a) and (b) by the equivalent Thevenin model of a conventional gate driver, which includes a pulse voltage source v_{DRV} stepping from 0 V to 10 V and the gate resistance R_{G}. With the Verilog-A modules not inserted (see Fig. 5), the resulting switching waveforms are shown in Fig. 7 in dotted lines for (a) the turn on and (b) the turn off of T_{LS}. It is worth noting that they are affected by oscillations superimposed onto i_{D} and v_{DS}. The oscillation frequency was found to be f_{ON}=36 MHz at the turn on and f_{OFF}=30 MHz at the turn off, in agreement with the values reported in Tab. I. From Fig. 7(a), at t=50 ns, i.e., i_{D}=3 A, the v_{DS} voltage is approximately equal to 35 V, meaning that the transistor is still in saturation when the oscillations are triggered. Regarding the turn off (see Fig. 7(b)), the simulations was carried out with I_{LOAD}=10 A, rather than 3 A reported in Table I, to increase the amplitude of oscillations.

The Verilog-A modules were then included in the schematic to be simulated as shown in Fig. 6. The values of $R_{\mathrm{X,end}}, R_{\mathrm{Y,end}}$ were obtained from (6), (11), resulting in 7 Ω and 1.9 Ω, respectively. At first, it was set $R_{\mathrm{X}}(v_{\mathrm{HS}}) = R_{\mathrm{X,end}}$ ($R_{\mathrm{Y}}(i_{\mathrm{D}}) = R_{\mathrm{Y,end}}$), i.e., the damping resistance is constant, resulting in the solid lines shown in Fig. 7(a) (7(b)). As can been seen from the graphs, oscillations are no longer superimposed onto i_{D} and v_{DS} neither at the turn on nor at turn off. By considering the sum of v_{DS} and $v'_{\mathrm{T,ON}}$ at the turn on, this waveform experiences a non monotonic behavior. Similarly, at the turn off, the insertion of $i_{\mathrm{T,OFF}}$ slightly increases the current flowing in the parasitic inductance, i.e., $i_{\mathrm{D}} + i'_{\mathrm{T,OFF}}$, counterbalancing the i_{D} decrease.

Finally, R_{X} and R_{Y} took the expressions in (13) and (14), resulting in the dashed and dashed-dot curves shown in Fig. 7. As for the constant resistance case, oscillations are no longer superimposed, in accordance with the theoretical analysis previously reported. Depending on the values of $R_{\mathrm{X,start}}$ and V_{RATE}, the resulting switching waveforms are slightly different. Referring to the turn on, by posing $R_{\mathrm{X,start}} = 0\,\Omega$ and V_{RATE}=10 V (dashed dot lines), one can get the fastest non-oscillating transient amongst those reported, but with the highest current peak. Indeed, with $V_{\mathrm{RATE}} = 10\,\mathrm{V}$, R_{X} will increase to $R_{\mathrm{X,end}}$ more slowly than with $V_{\mathrm{RATE}} = 2\,\mathrm{V}$ (dotted lines), thus the equivalent damping resistance will be smaller for a longer time during the transient. A similar result was obtained at the turn off when I_{RATE} was increased from 0.2 A to 2 A. What emerges from Fig. 7(a) is that

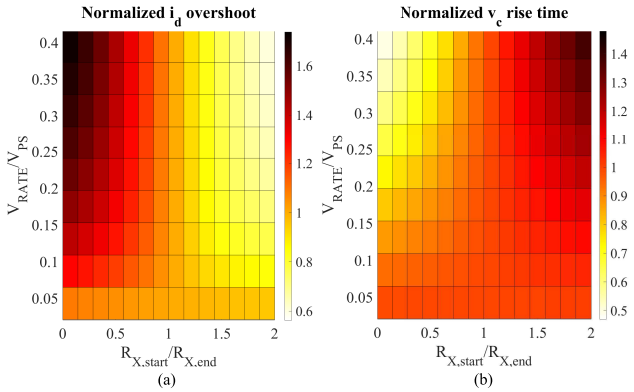

Fig. 8. Impact of $R_{\mathrm{X,start}}$ and V_{RATE} on (a) the i_{D} current peak and (b) v_{HS} rise time.

the choice of the $R_{\mathrm{X,start}}$ and V_{RATE} parameters affects the current and voltage switching waveforms. Even though the R_{X} function provides some degrees of freedom, an intrinsic trade-off between the voltage rise time and the current overshoot exists at the T_{LS} turn on. Indeed, with $i_{\mathrm{D}} \geq I_{\mathrm{LOAD}}$, the total charge to be provided to C_{HS} can be evaluated as

$$\int_{t_0}^{t_0+t_{\mathrm{rise}}} (i_{\mathrm{D}}(t) - I_{\mathrm{LOAD}})dt = C_{\mathrm{HS}}(V_{\mathrm{PS}})V_{\mathrm{PS}}, \qquad (18)$$

where t_{rise} is the time required by v_{HS} to increase from 0 V to V_{PS}. As the right-side of (18) is constant, t_{rise} may not be decreased at will, without increasing the i_{D} overshoot as well. To investigate further the impact of $R_{\mathrm{X,start}}$ and V_{RATE} on such performance, parametric simulations were performed on the circuit shown in Fig. 6(a) by sweeping $R_{X,start}$ from 0 to $2R_{\mathrm{X,end}}$, and V_{RATE} from 1 V to 20 V. For each combination, the overshoot of the drain current and the rise time of the v_{HS} voltage were monitored, as shown in Fig. 8 normalized to the $R_{\mathrm{X,start}} = R_{\mathrm{X,end}}$ case. With R_{X} constant, a balanced trade-off is achieved, with t_{rise}=18 ns and a 6 A overshoot. By decreasing $R_{\mathrm{X,start}}$ ($R_{\mathrm{X,start}}/R_{\mathrm{X,end}} \leq 1$) and increasing V_{RATE}, the v_{HS} rise time decreases up to halve (upper left region of Fig. 8(a),(b)), but the peak current is up to 1.7 times the initial one. On the contrary, by setting $R_{\mathrm{X,start}} = 2R_{\mathrm{X,end}}$ and $V_{\mathrm{RATE}} = 0.4V_{\mathrm{PS}}$, the current overshoot halves and the voltage rise time increases by 50 % (upper right region of Fig. 8(a),(b)) with respect to the constant resistance case. Finally, with small V_{RATE} values, the switching performance are those of the constant resistance case, as $R_{\mathrm{X}} \approx R_{\mathrm{X,end}}$ for most of the v_{HS} transient.

In summary, the choice of $R_{\mathrm{X,start}}$ and V_{RATE} should account for the target commutation speed, the voltage slope and the maximum current overshoot. As a result, one could start by setting R_{X} equal to $R_{\mathrm{X,end}}$, resulting in a balanced trade-off between the aforementioned figures of merit. The values of $R_{\mathrm{X,start}}$ and V_{RATE} can be then tailored depending on the particular application.

IV. Proposed AGD tuning method

Controlled sources $v'_{\mathrm{T,ON}}$ and $i'_{\mathrm{T,OFF}}$ were found to be effective in damping the oscillations. However, such elements

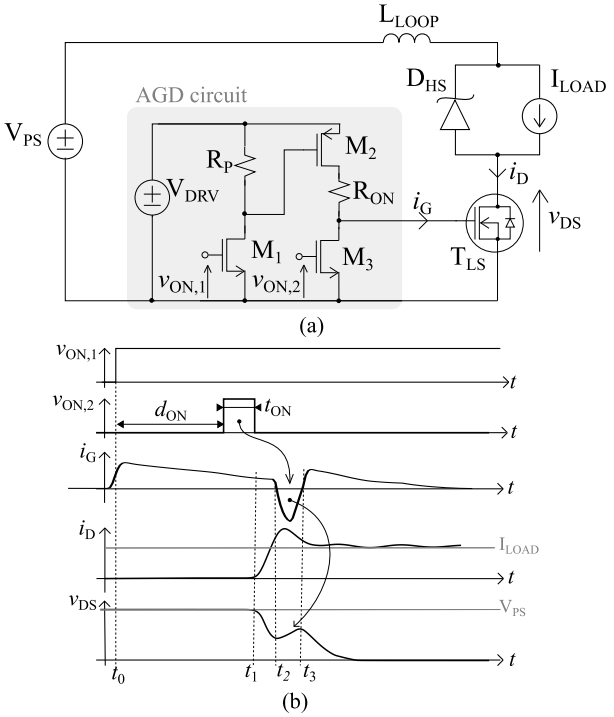

Fig. 9. In (a) circuit of the active gate driver included in the circuit shown in Fig. 5. In (b), the corresponding waveforms at the T_{LS} turn on. The AGD parameters defining the modulation profile are d_{ON} and t_{ON}.

are not intended to be directly implemented as extra components in the switching loop. With $v'_{\mathrm{T,ON}}$ and $i'_{\mathrm{T,OFF}}$ included in the circuit to be simulated, the target switching waveforms, which should be attained by an AGD-driven power transistor at last, can be evaluated. In such a way, the switching trajectory of the power transistor is shaped to damp oscillations with minimum power losses on T_{LS}. By denoting with $v_{\mathrm{DS,AGD}}$ and $i_{\mathrm{D,AGD}}$ the drain source voltage and the drain current of an AGD-driven power transistor, the AGD should be driven such that

$$v_{\mathrm{DS,AGD}}(t) = v_{DS,TRG}(t) = v_{\mathrm{DS,CGD}}(t) + v'_{\mathrm{T,ON}}(t) \quad (19)$$

at the turn on, and

$$i_{\mathrm{D,AGD}}(t) = i_{\mathrm{D,TRG}}(t) = i_{\mathrm{D,CGD}}(t) + i'_{\mathrm{T,OFF}}(t) \qquad (20)$$

at the turn off. With the target waveforms defined as (19) and (20), a tuning of the modulation profile can be performed in simulation. Such a procedure should account for the actual AGD circuit, meaning that the tuning method should be tailored on the basis of the parameters defining the modulation profile. As AGD previously introduced in [25] will be exploited later as a test case, the corresponding circuit is briefly recalled in what follows to identify the actual parameters to be tuned.

A. AGD circuit

The considered AGD, which is effective in damping the oscillations at the T_{LS} turn on, is shown in Fig. 9(a). More precisely, the AGD circuit has been included in the circuit shown in Fig. 5. The exploited AGD strategy is based on the

activation of $v_{\mathrm{ON},2}$ during the turn-on transient, resulting in the output switching waveforms (i_{D} and v_{DS}) to be shaped to avoid oscillations.

The effectiveness of such an AGD can be discussed referring to the time domain waveforms shown in Fig. 9(b). At $t = t_0$ the T_{LS} turn-on is triggered by setting $v_{\mathrm{ON},1}$ high. As a consequence, transistors M_1, M_2 switch from interdiction to triode, and a positive gate current (i_{G}) flows. When the gate-source voltage overcomes the threshold voltage at $t = t_1$, T_{LS} enters the saturation region, and its drain current increases. Meanwhile, v_{DS} decreases because of the voltage drop across the parasitic inductance L_{LOOP}. The control signal $v_{\mathrm{ON},2}$ is activated after a delay d_{ON} from the turn-on triggering, leading to the turn on of M_3 after some delay. With M_3 in triode, the gate current decreases, until it becomes negative at t_2. With T_{LS} still in the Miller region, it is

$$\frac{dv_{\mathrm{DS}}(t)}{dt} = -\frac{i_{\mathrm{G}}(t)}{C_{\mathrm{gd}}}, \tag{21}$$

meaning that with the gate current negative, the v_{DS} slightly increases ($t_2 < t < t_3$). With the local v_{DS} increase occurring when the $L_{\mathrm{LOOP}} - C_{\mathrm{HS}}$ resonance is triggered, T_{LS} is exploited in place of `vt_primus_on` to damp the oscillations.

The signal $v_{\mathrm{ON},2}$ is set high for a t_{ON} time interval, meaning that once the oscillations have been damped, M_3 turns off and i_{G} increases. With the gate current again positive ($t > t_3$), T_{LS} enters the triode region eventually.

The v_{DS} shape resulting from the activation of $v_{\mathrm{ON},2}$ is close to that of $v_{\mathrm{DS}} + v'_{\mathrm{T,ON}}$ reported in Fig. 7(a), meaning that the proposed AGD strategy can shape the T_{LS} trajectory to damp oscillations. The effectiveness of such a driving circuit in avoiding the triggering of oscillations, provided that proper $d_{\mathrm{ON}}, t_{\mathrm{ON}}$ values are exploited, was experimentally assessed in [25], [35].

B. Tuning procedure

The aim of the tuning procedure is to determine the values of the AGD parameters to achieve the same switching waveforms obtained with the Verilog-A behavioral blocks. As the modulation profile is determined by the values of $d_{\mathrm{ON}}, t_{\mathrm{ON}}$ in the considered test case, the proposed tuning procedure determined for which $d_{\mathrm{ON}}, t_{\mathrm{ON}}$ values (19) is attained. Before the algorithm can be executed, it is required to simulate the power circuit with the non-linear `vt_primus_on` inserted, as discussed in Sect. III. By considering the $v_{\mathrm{DS,TGR}}$ defined as (19), the curve shown in Fig. 11 in dashed line is obtained for the considered test case. Such a curve was obtained by exploiting the AGD as a CGD, i.e., by not activating $v_{\mathrm{ON},2}$, and by posing V_{RATE}=10 V and $R_{\mathrm{X,start}}$=5 Ω. It is possible to identify two time instances $t_{\mathrm{A,TRG}}, t_{\mathrm{B,TRG}}$, which correspond to the $d^2 v_{\mathrm{DS,TGR}}/dt^2 = 0$, and the $v_{\mathrm{DS,TGR}}$ value at $t_{\mathrm{B,TRG}}$ ($V_{\mathrm{B,TRG}}$), i.e., the local maximum. It is worth noting that $t_{\mathrm{A,TRG}}$ ($t_{\mathrm{B,TRG}}$) corresponds to t_2 (t_3) in Fig. 9(a). The flowchart reporting the proposed tuning method is shown in Fig. 10. Although it refers to the turn on transient, the same steps can be applied to the turn off one as well. The procedure is based on iterative simulations of the circuit shown in Fig. 6(a), where the `vt_primus` is not inserted and the CGD is replaced by the AGD shown in Fig. 9(a). In order for the algorithm to stop when (19) is attained, the values of $t_{\mathrm{A,i}}, t_{\mathrm{B,i}}, V_{\mathrm{B,i}}$ are monitored during the execution. In such a way, depending on the conditions met, the algorithm moves between steps 4 to 8, and it stops when the absolute difference between $t_{\mathrm{B,i}}$ ($V_{\mathrm{B,i}}$) and $t_{\mathrm{B,TRG}}$ ($V_{\mathrm{B,TRG}}$) is within Δt_{B} (ΔB).

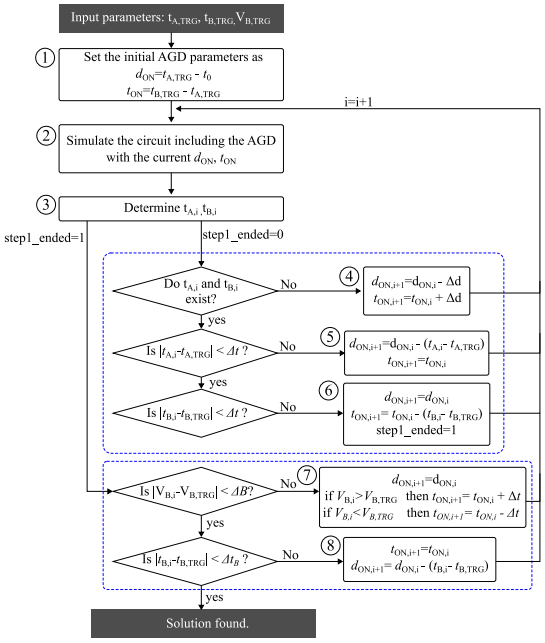

Fig. 10. Flowchart of the proposed AGD tuning method.

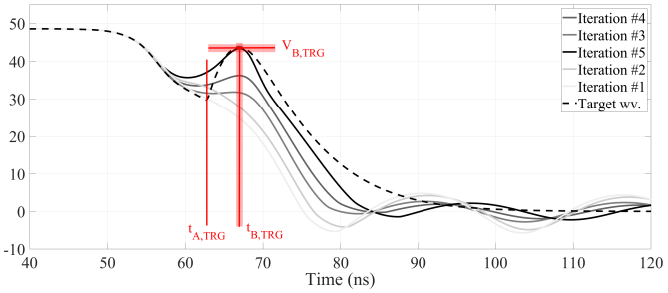

Fig. 11. Waveforms obtained during the execution of the algorithm reported in Fig. 10. The target switching waveform (dashed line) is achieved at the fifth iteration (darkest solid line).

On the basis of $t_{\mathrm{A,TRG}}, t_{\mathrm{B,TRG}}$, the algorithm set the initial AGD parameters (step 1), and run a simulation of the circuit including the power stage and the AGD itself (step 2). For the considered test case, $v_{\mathrm{DS,AGD}}$ is shown in Fig. 11(a) in the lightest solid line. The values of $d_{\mathrm{ON}}, t_{\mathrm{ON}}$ during the algorithm iterations have been reported in Fig. 12 for comparison. With the initial values of $d_{\mathrm{ON}}, t_{\mathrm{ON}}$, the v_{DS} voltage is not monotonic, thus the algorithm increases (decreases) t_{ON} (d_{ON}) by Δd (step 4) twice. At the third iteration, the obtained waveform is characterized by a non monotonic behavior, with $t_{A,i}$ and $t_{B,i}$ close to $t_{\mathrm{A,TRG}}$, $t_{\mathrm{B,TRG}}$. The `step1_ended` flag is therefore asserted, and the algorithm moves to verify whether $V_{\mathrm{B,TRG}}$ is met. As the value of $v_{\mathrm{DS,AGD}}$ close to the local maximum is much lower than $V_{\mathrm{B,TRG}}$, t_{ON} is

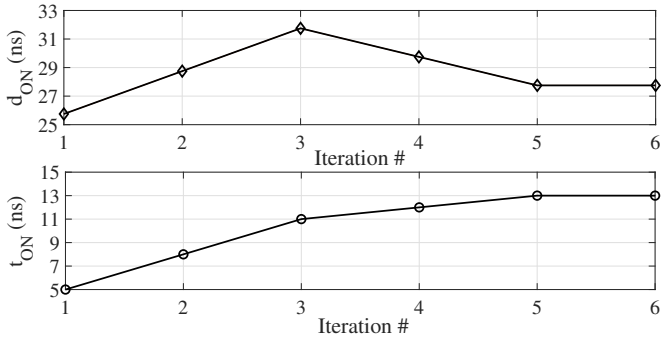

Fig. 12. The AGD parameters during the algorithm iterations are reported.

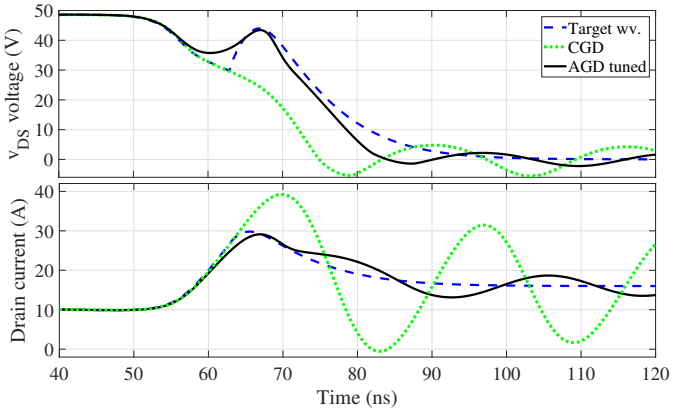

Fig. 13. Waveforms of i_{D} current and v_{DS} voltage without the insertion of the `vt_primus_on` block (dotted), with the Verilog-A block inserted (dashed) and after the AGD tuning (solid lines).

increased (step 7) from iteration nro. 3 up to nro. 5. Finally, the algorithm converges at the fifth iteration. The resulting switching waveforms are shown also in Fig. 13 in solid lines. As expected, the tuning algorithm results in a drain current and v_{DS} voltage close to those obtained by the insertion of the `vt_primus_on` block (dashed lines). The waveforms resulting from the AGD exploited as a CGD are shown for comparison in dotted lines in Fig. 13. It is worth noting that the proposed method is effective in damping the oscillations which are superimposed onto the v_{DS} and i_{D} waveforms.

C. Sensitivity analysis

With the AGD tuned in simulation, parametric simulations were performed to address the parameter spread issue. Variations of the T_{LS} threshold voltage (V_{TH}), of the ambient temperature, and of the T_{LS} internal gate resistance ($R_{\mathrm{G,int}}$) were considered. The variation ranges for such parameters are in accordance with the values declared by the manufacturer of the T_{LS} transistor [31], i.e., V_{TH} between 2 V and 4 V and operating temperature range between -55 °C and 155 °C. Regarding the internal gate resistance, it was varied between $1\,\Omega$ and $5\,\Omega$. Finally, the stray inductance L_{LOOP} was modified by ± 5 nH around its nominal value reported in Table I. These parameters were chosen as they all affect the switching trajectory of T_{LS}, and they are affected by spreading, meaning that their actual values may not be exactly known *a-priori*. It is worth noting that the switching frequency governs

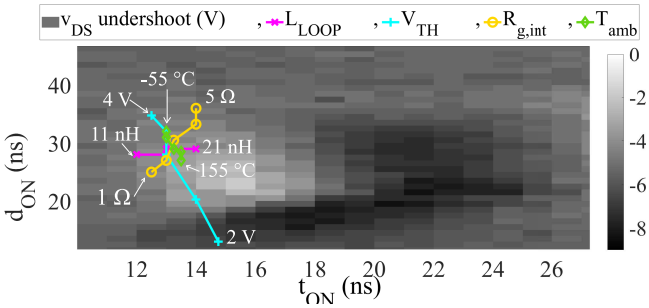

Fig. 14. With the power circuit affected by parameter spread, the proposed algorithm results in different set of AGD parameters. Variations of the threshold voltage (plus), internal gate resistance (circle), ambient temperature (diamond) and loop inductance (cross markers) were considered. In all these cases, the identified AGD parameters are close to a local minimum (lightest region).

the repetition rate of the T_{LS} commutations, but it does not affect the phenomena taking placing during the transients. The considered parameters were swept one at the time, and the algorithm depicted in Fig. 10 was run several times. The resulting tuned $(d_{\mathrm{ON}}, t_{\mathrm{ON}})$ have been stored and then plot altogether in Fig. 14. As it can be noticed, each of the considered parameter affect $(d_{\mathrm{ON}}, t_{\mathrm{ON}})$. As these parameters are affected by uncertainty, the proposed method can only provide a guess of the AGD parameters, but a finer tuning is required on-the-fly to account for the spread issue. The simulation results were then compared against experimental measurements performed on the AGD discussed in Sect. IV-A. Indeed, by sweeping the $d_{\mathrm{ON}}, t_{\mathrm{ON}}$ parameters, the v_{DS} undershoot, which is an indirect measure of the oscillation amplitude at the turn on, was measured are reported as background of Fig. 14. Although the parameter spread results in a spread of $d_{\mathrm{ON}}, t_{\mathrm{ON}}$ in simulation, it should be noticed that the results are all close to the left-most lightest region, which corresponds to a region of low undershoot and low power switching losses [25]. This means that, although in practice the AGD parameters obtained with the proposed method may not be exactly those of the damping solution, they are close enough for a on-the-fly minimization algorithm to converge.

V. Experimental validation

With the initial AGD parameters obtained, experimental measurements were performed to assess the validity of what presented so far. To this purpose, the adaptive low-complexity AGD presented in [25] was exploited to assess whether the method proposed in this paper is effective in determining the initial set of AGD parameters.

A. Adaptive AGD system

The block-level view of the adaptive AGD used for validation is shown in Fig. 15. The undershoot affecting the drain source voltage is measured at each T_{LS} turn-on transient by means of a sensing circuit, which comprises a peak detector and a differential amplifier to adapt the signal to the ADC input range. The amplifier output ($v_{\mathrm{ADC,N}}$) is sampled by an ADC, whose output is fed to an tracking algorithm to finely adjust the

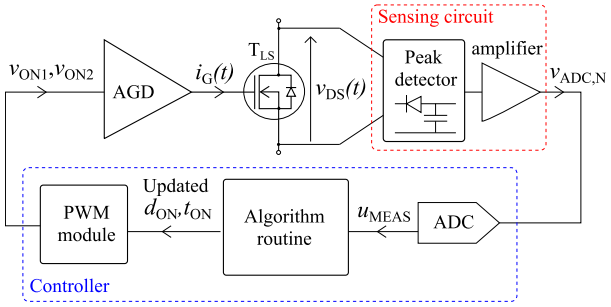

Fig. 15. Architecture of the adaptive AGD exploited to validate the proposed method experimentally.

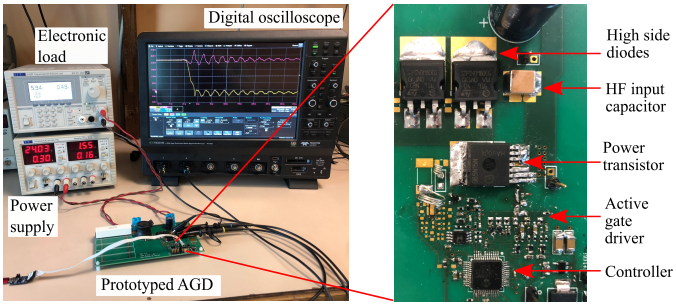

Fig. 16. Experimental test bench and, on the right, a photograph of the PCB board comprising the power stage, the AGD and the controller.

AGD parameters, i.e., $d_{\rm ON}$ and $t_{\rm ON}$. Such a tracking algorithm is based on the steepest descend gradient method, which is implemented by means of a software Finite State Machine. In such a way, the adaptive AGD can cope with operating condition variations and parameter spread. The updated AGD parameters are effective on the timing of $v_{\rm ON,1}, v_{\rm ON,2}$ at the next switching transient. The AGD circuit is that previously discussed in Sect.IV-A. In order for the optimization algorithm to converge the $v_{\rm DS}$ undershoot minimum shown in the color-map of Fig. 14, an initial guess of $d_{\rm ON}$, $t_{\rm ON}$ sufficiently close to the local minimum must be known. A brute force approach was initially exploited, which consisted in sweeping $d_{\rm ON}$ and $t_{\rm ON}$ with a coarse step after the controller is powered on, and by identifying the pair resulting in the lowest undershoot.

The discussed adaptive AGD was implemented in an ad-hoc printed circuit board. The driven power transistor is comprised in a low-side asynchronous buck converter. The dc-dc converter steps down a 48 V input to a 12 V output voltage, and it can provide the load with a 5 A maximum current. A photograph of the experimental test bench is shown in Fig. 16 on the left, where the lab instruments have been labeled to be identified at a glance. The layout of the PCB has been zoomed and it is shown on the right.

B. Experimental results

With the initial set of AGD parameters identified as discussed in Sect. IV, $v_{\rm DS}$ waveforms were acquired before and after the execution of the tracking method based on the steepest gradient descend, through the digital oscilloscope shown in Fig. 16. The corresponding results are shown in Fig. 17. It is worth noting that the initial set of AGD parameters

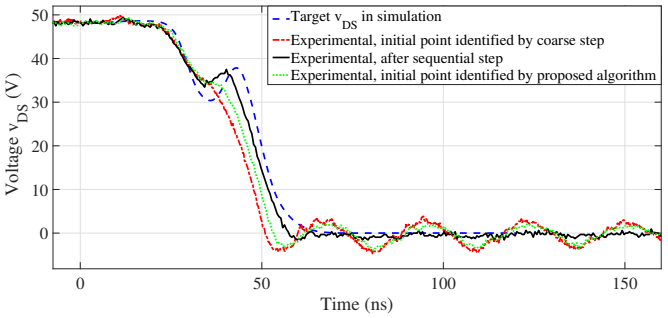

Fig. 17. Experimental $v_{\rm DS}$ obtained from the initial set of AGD parameters (dotted), and after the tracking algorithm (solid line). The target waveform obtained in simulation is in dashed line for comparison.

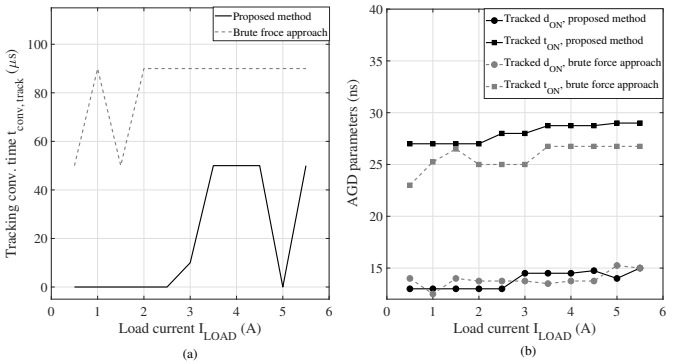

Fig. 18. Comparison between the (a) the convergence time and the final set of AGD parameters for a 0.5- to 5-A load current variation with the method proposed in this paper (solid) and the coarse sweep approach (dashed lines).

identified in simulation ($d_{\rm ON}, t_{\rm ON}$)=(28,13) ns with a 3 A load current results in slightly oscillating waveforms (dotted line) at the turn on of the power transistor. Then, the AGD controller applies the steepest descend method, and refines the initial set in (28, 14.5) ns. As a result, the $v_{\rm DS}$ voltage is that shown in Fig. 17 in solid line, in which oscillations are not longer superimposed onto. The impact of the AGD modulation on power switching losses was found to be negligible, as previous measurements resulted in the same conversion efficiency of the dc-dc converter with $T_{\rm LS}$ driven by a CGD (oscillating case) or by the tuned AGD (solid line in Fig. 17). The target waveform obtained in simulation by means of the $v'_{\rm T,ON}$ is also plotted in dashed line for comparison. Solid and the dashed curves are not monotonic during the $v_{\rm DS}$ falling edge, as expected from theory, and they are not affected by oscillations. Indeed, the dotted line only shows a small hump, which is not sufficient to damp the oscillations. As previously discussed in Sect. IV, discrepancies between the simulation and experimental setup, which are accountable to parameter spread, result in different set of AGD parameters. Finally, the waveform obtained from the brute force approach proposed in [25] is reported in dashed-dot line. It can be noticed that, although the very same gradient method is able to modify the dashed curve in the solid one, the time required will be higher than in case of the dotted line, as the initial set of AGD parameters is farther from the left-most minimum.

To address this point more in details, the time required by

the tracking algorithm was measured for several values of load current. With the method proposed in this paper, the algorithm depicted in Fig. 10 was run several times for different values of I_{LOAD}. The resulting set of initial points, obtained by simulations, were then refined by the AGD controller on-the-fly. This operation lasted from 0 to 50 μs, as shown in Fig. 18(a) by solid line. Indeed, for load current lower than 3 A, the simulated parameters were suited as they were. On the contrary, with the brute force approach, the time required for the tracking phase was higher, as shown in Fig. 18(a) by dashed line. It should be noticed that the method proposed in this paper not only decreases the convergence time of the tracking phase, but it also avoids the initial sweep, which required 3.4 ms. Although the initial points identified by the proposed method may differ from those obtained by the brute force approach, the final AGD sets are in good agreement, as shown in Fig. 18(b).

VI. Conclusion

A tuning method for active gate drivers has been presented in this paper to avoid oscillations during the switching transients. The proposed technique is based on the insertion of non-linear dissipative elements, which have been implemented by Verilog-A modules, in the power circuit to simulate. The resulting switching waveforms can be exploited as those to be attained by the AGD-driven transistor, allowing one to determine the AGD parameters *a-priori*. It was found that the tuning procedure, which was tailored for the AGD circuit at disposal, required five iterations to find a suitable set of AGD parameters. Then, the proposed method was assessed experimentally on an adaptive AGD to provide it with the initial set of parameters. The values identified by the tuning method allowed the adaptive controller to converge in 10 µs with a 3 A load current. It is worth noting that this time is nine times lower than that required by the adaptive controller without exploiting the proposed method. A similar result was obtained for the overall range of load current, meaning that the technique presented in this paper is well suited for finding the initial parameters in adaptive AGDs.

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Appendix A

The $v'_{\mathrm{T,ON}}$ described by (16) and shown in Fig. 6(a), was implemented in Verilog-A as a standalone components as follows.

```
1  `include "constants.vams"
2  `include "disciplines.vams"
3
4  module vt_primus_on(vp, vn, capp, capm, mosp, mosm, currp
     , currm);
5  inout vp, vn;
6  input capp, capm, mosp, mosm, currp, currm;
7  electrical vp, vn, capp, capm, mosp, mosm, currp, currm;
8
9  parameter real Vrate=10;
10 parameter real Rend=10.4;
11 parameter real Iload=5;
12 parameter real Rstart=0;
13
14 real temp;
15 real r_t;
16
17 branch (currp,currm) iD;
18 analog begin
19 temp=1m;
20
21 if (I(iD)>Iload) begin
22   r_t=Rend+((Rstart-Rend)*exp(-V(capp, capm)/Vrate));
23   temp=((I(iD)-Iload)*r_t)-V(mosp, mosm);
24   if (temp<0) begin
25     temp=1m;
26   end
27 end
28 V(vp, vn) <+ transition(temp, 0, 100p);
29 end
30 endmodule
```

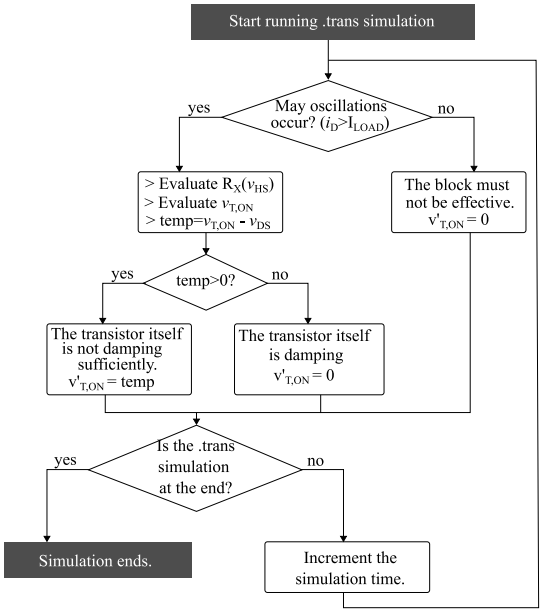

Fig. 19. Flowchart of the algorithm implementing the `vt_primus_on` Verilog-A block.

Instances of such a Verilog-A module can be parametrized in terms of $V_{\mathrm{RATE}}, R_{\mathrm{X,start}}$ and $R_{\mathrm{X,end}}$, and load current. In such a way, the Verilog-A code is independent from the particular circuit it is inserted in, and it can be tailored for different values of L_{LOOP} inductance and C_{HS} capacitance by selecting $R_{\mathrm{X,end}}$ in accordance with (6). To discuss the behavior of the `vt_primus_on`, the Verilog-A listing is complemented by the flowchart shown in Fig. 19. During the transient simulation, the Verilog-A block waits for the triggering of the turn-on oscillation, i.e., $i_{\mathrm{D}} > I_{\mathrm{LOAD}}$ (row 21). Up to that time, the voltage across the output port (`vp, vn`) is zero (row 19), meaning that the Verilog-A block does not affect the transient waveforms. As far as $i_{\mathrm{D}} > I_{\mathrm{LOAD}}$, the instantaneous value of R_X is evaluated at row 22 in accordance with (13). Based on that, the $v'_{\mathrm{T,ON}}$ is computed (row 23) and assigned to the provisional variable `temp`. As $v'_{\mathrm{T,ON}}$ is an extra dissipative element, it should only be outputted in case T_{LS} does not provide sufficient damping, i.e., $v'_{\mathrm{T,ON}} > 0$. As the voltage across output port can not be set inside conditional blocks, the actual assignment is at row 28, where a 100 ps transition time is included to avoid convergence issues.

Regarding the current source $i'_{\mathrm{T,OFF}}$ included in Fig. 6(b),

the corresponding netlist is

```
1  `include "constants.vams"
2  `include "disciplines.vams"
3
4  module it_primus_off(mosp, mosm, currp, currm, vp, vm);
5  input mosp, mosm;
6  output vp,vm;
7  input currp, currm;
8  electrical mosp, mosm, currp, currm, vp, vm;
9
10 parameter real Coss=1e-9;
11 parameter real Vps=48;
12 parameter real Irate=0.1;
13 parameter real Rstart=100;
14 parameter real Rend=10;
15
16 branch (currp,currm) iD;
17 real startCurrent;
18 real temp, rt;
19 real ichannel;
20
21 analog initial begin
22 startCurrent=-1;
23 end
24
25 analog begin
26 temp=1m;
27 ichannel=I(iD)- ddt(Coss*(V(mosp,mosm)));
28 if (V(mosp,mosm)>Vps) begin
29   if(startCurrent<0) begin
30     startCurrent=I(iD);
31   end
32   rt=Rend+(Rstart-Rend)*exp(-(startCurrent-I(iD))/Irate);

33   temp= ((V(mosp,mosm)-Vps)/rt)-ichannel;
34   if (temp<0) begin
35    temp=1m;
36   end
37 end
38 I(vp, vm) <+ temp;
39 end
40 endmodule
```

As for vt_primus_on, the it_primus_off module can be customized by setting parameters $I_{\mathrm{RATE}}, R_{\mathrm{Y,start}}$ and $R_{\mathrm{Y,end}}$. Moreover, the V_{PS} value, and that of the output capacitance of the AGD-driven transistor for $v_{\mathrm{DS}} = V_{\mathrm{PS}}$ should be provided as well. The operation is similar to that discussed for the turn-on block. Indeed, this Verilog-A module allows one to implement (14) and (17) (see rows 34-35) when the turn off oscillations are triggered, i.e., $v_{\mathrm{DS}} > V_{\mathrm{PS}}$ (row 28).

It is worth noticing that such modules can be modified to implement $R_{\mathrm{X}}, R_{\mathrm{Y}}$ functions different from the exponential ones exploited in this work.

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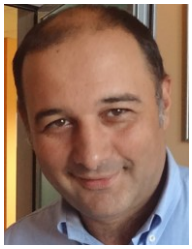

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