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03 November 2026

A Fully Depleted CMOS Sensor Prototype for HEP Timing Applications

Stefano Durando
On behalf of the ARCADIA collaboration

***Abstract*—The ARCADIA project at INFN is developing Fully Depleted Monolithic Active Pixel Sensors (FD-MAPS). FD-MAPSs collect the charge mainly by drift, which allows for a faster collection time, and a better time resolution.**
In this context, a 2 x 2 mm^2 pixel array optimized for a time resolution better than 100 ps has been fabricated. The individual collection diode has a size of 50 x 50 μm^2. Eight diodes are grouped together and read out by a dedicated front-end channel composed of a charge sensitive amplifier and a discriminator with self-compensation of the offset. To maximize the uniformity of the electric field the electronics is located at the matrix periphery.
The sensor is implemented in a 110 nm CMOS technology with 3.3 V and 1.2 V transistors, and 6 metal layers.
The different terms that contribute to the system time resolution have been estimated with electronics computer-aided design (ECAD) tools, and optimized to target a time resolution below 100 ps.

I. Introduction

THIS summary presents a prototype of a fully depleted CMOS sensor targeting sub-100 ps time resolution.
Monolithic CMOS sensors are becoming an attractive solution for tracking applications in High Energy Physics (HEP) experiments, as it is confirmed by their recent implementation in different experiments [1], [2], [3]. They integrate in the same silicon wafer both the sensor and the readout electronics, with standard fabrication processes, allowing for a strong reduction in the material budget and costs compared to the hybrid technology.
In the recent past, different works have shown that silicon sensors can be a competitive solution also for timing applications in the field [4], [6], targeting sub-50 ps time resolution. In this context, the development of a CMOS sensor for fast timing is of interest. However, state-of-the-art CMOS sensors do not compete with the available hybrid solutions, and best results achieved are above 100 ps [5].
This work is part of the ARCADIA project at INFN, which aims to develop a novel CMOS sensor platform with low noise, fast charge collection and low power readout in a quadruple well 110 nm technology node [7].

II. Time Resolution

The design has been focused on the optimization of the time resolution for time of flight detectors.

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Key blocks of such systems are the sensor, the preamplifier, the discriminator and the Time to Digital Converter (TDC). The resulting time resolution can be partitioned into different terms, as it is reported in the following expression.

$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{Distortion}^2 + \sigma_{TimeWalk}^2 + \sigma_{Jitter}^2 + \sigma_{TDC}^2 \quad (1)$$

The Landau term is due to the physics of the charge generation process in the sensor. The Distortion term is related to the weighting field non-uniformity and the non saturated velocity of the drifting charge in the sensor. The Time-Walk effect is due to the fact that signals with equal shapes but with different amplitudes cross the constant threshold of the discriminator at different times, this is related to the ionization process in the sensor and to the constant threshold. The Time-Walk is a deterministic effect, and can be corrected with different techniques, such as amplitude or Time over Threshold (ToT) corrections. The electronics Jitter is mainly due to the amplifier jitter and can be expressed as the ratio between the r.m.s. of the electronic noise and the slew rate of the signal.
Finally, the TDC affects the resolution with the r.m.s. quantization noise, equal to bin-size/$\sqrt{12}$. With a bin size of few tens of picoseconds the TDC contribution si negligible with respect to the target requirements.
The time resolution limit is at the sensor front-end interplay.

III. The ARCADIA Sensor

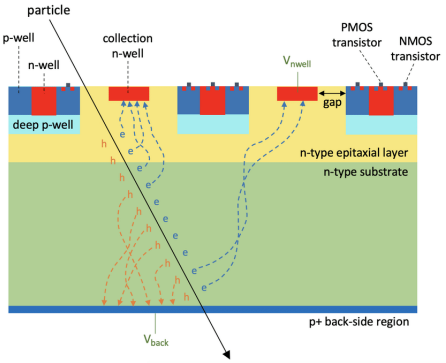


Fig. 1. ARCADIA sensor scheme [8]

The ARCADIA sensor has an n-on-n structure [7], [9]. A high resistivity n-type substrate provides an active volume. N-well electrodes collect the electrons, while the deep p-wells shield the embedded electronics.
The potential barrier in the deep p-well region is controlled

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with a lower resistivity epitaxial layer in between the high resistivity substrate and the deep p-well.
The sensors are fully depleted by applying a negative voltage to the p+ backside layer, reaching a depletion thickness of 50 μm for the thinnest prototype. Prototypes with larger active thicknesses have been also fabricated. For the present prototype, the diode is $\simeq$ 50 x 50 μm^2 large, with large area electrodes for a better uniformity of the weighting field.

IV. Front-End Electronics

The sensing diodes are DC coupled to the front-end electronics.
The first stage is a charge sensitive amplifier (CSA), implemented with a cascode topology with split bias current as the core amplifier. The use of 3.3 V transistors allows for a self biasing of the input node higher than 1.2 V, resulting in a faster charge collection time.
The preamplifier output can be read by two branches, FE0 and FE1.
As shown in Fig. 1, FE0 is the main branch of the channel. The first stage is connected via a coupling capacitor to a leading-edge discriminator. The latter is designed with 1.2 V transistors, and it is composed of three cascaded tri-state inverters. Each inverting stage is connected to the next one with a 20 fF capacitor. The correction of the discriminator offset is carried out with a discrete-time self-compensation technique. At every readout cycle, the input and the output of the inverters are connected by closing a switch. Then, the unity gain feedback allows for storing the offset on the coupling capacitors at the input of each inverting stage, with an error proportional to the offset and inversely proportional to 1 + A, with A open loop gain of the stage. A dedicated

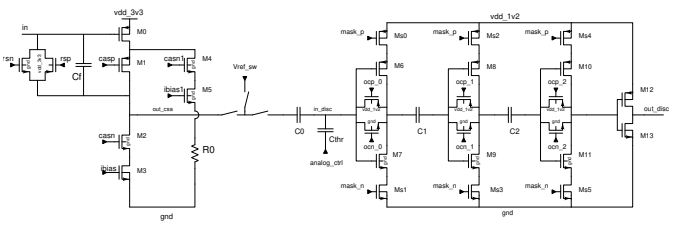


Fig. 2. FE0 transistor level scheme

circuit is used to inject a threshold at the input node of the discriminator, and to discharge the node linearly to obtain the signal ToT proportional to its amplitude. A voltage ramp is generated by discharging with a constant current a capacitor. The resulting voltage is buffered and fed to a 2 fF momcap (C_{thr}) which is coupled to the input node of the discriminator. FE1 implements a Sample and Hold, which allows to measure the analog signal at the preamplifier output.

Sensor simulations show that large area diodes have better timing performances due to the better uniformity of the weighting potential. As a consequence, the available deep p-well area on the pixel is significantly reduced. Therefore, the front-end electronics is implemented outside the pixels region, at the end of the column.

Each channel reads 8 parallel diodes and the resulting total capacitance is expected to be $\simeq$ 280 fF .
The prototype has 48 channels grouped into 24 columns. Every 4 neighbouring columns outputs are fed to an OR gate and sent out of the chip, for a total of 12 output lines.

V. Simulation Results

The sensor performance has been studied with Monte Carlo simulations. The best results are expected for the thinnest sensors with an intrinsic time resolution below 50 ps[1][10].

The main contributors to the time resolution in the readout electronics are the jitter and the time-walk.
The former is estimated with ac noise simulations and transient simulations as rms$_{Jitter}$ = rms$_{noise}$/slew-rate. The jitter value has a strong dependence from the collected charge. For a MIP crossing 50 μm of the detector, the most probable value of the charge collected is $\simeq$ 0.58 fC
For values greater than 0.5 fC, the jitter contribution is estimated to be below 100 ps, and below 50 ps for 1 fC. In Fig. 3 the jitter is studied as a function of the collected charge.

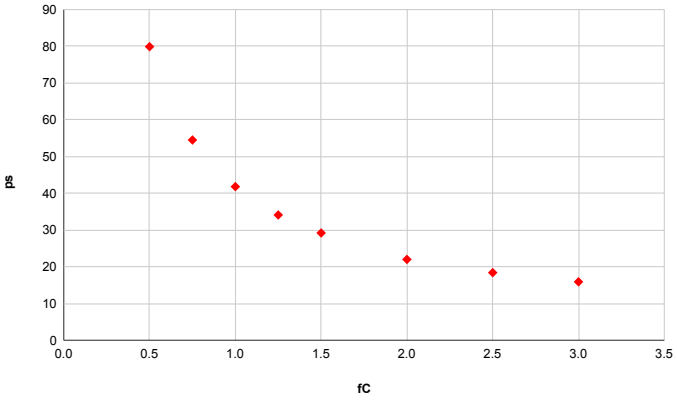


Fig. 3. Jitter vs collected charge

To estimate the time-walk contribution, the electronics chain response has been studied with a large set of signals simulated with the Monte Carlo method. The sensor simulations consider 200 MeV Muon like particles with Monte Carlo extraction of the angle of incidence and of the generated charge.
A sample of the signals is then used in the CAD tool to simulate the current signals fed into the electronics chain. Transient simulations are run and a calibration curve is defined by fitting a small set of Time of Arrival and Time over Threshold (ToA, ToT) combinations. These values are calculated from the output files of the CAD simulator. Then, the time-walk correction is carried out as:

$$\sigma_t = rms_{\Delta t_{out}} = \sqrt{\frac{\sum((t_{out_i} - t_{tw_cal_i}) - < t_{out} >)^2}{N}} \quad (2)$$

$t_{tw_cal_i}$ is the value obtained by using the calibration curve. The correction reduces the contribution down to 70 ps. This

[1]The intrinsic time resolution takes into account both the Landau and the Distortion terms

is the result of different contributions which affect the time resolution of the system: the sensor components and the time walk corrected component.
The yield of the circuit for process and mismatch variations has been estimated with Monte Carlo simulations. The circuit shows a good discrimination, with a yield above 99 % for the minimum collected charge simulated (0.4 fC). To improve the circuit robustness against process variations degeneration resistors implemented with MOS devices have been added in the inverter stages.
The layout of the prototype is shown in Fig. 4.
Tests of the prototype are ongoing in the INFN laboratory in Torino.

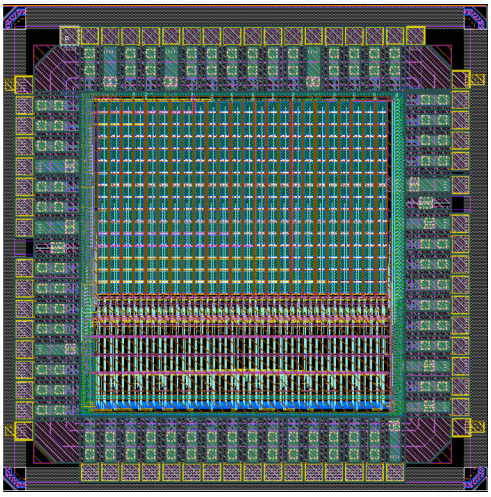


Fig. 4. Layout of the prototype

VI. Conclusions

A first prototype of a Fully Depleted CMOS sensor optimized for good timing resolution has been developed in a quadruple well 110 nm CMOS technology. The active thickness is 50 μm.
Simulations show that a time resolution below 100 ps can be achieved for a MIP particle crossing the sensor. In the present design the resolution is dominated by the residual time-walk and the amplifier jitter component.
The chip has been delivered by the foundry, and the test activities are started.

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