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# A Novel Quasi-Resonant Battery Charger for Photovoltaic Applications

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**Abstract**—This work presents the analysis, design, PCB implementation and testing of a quasi-resonant low-voltage battery charger intended to be supplied by a photovoltaic (PV) module. The proposed battery charger exploits the Discontinuous Voltage Mode operation to transfer to the load a controlled and discrete amount of energy, alternately stored and released by two half-bridge capacitors. A small resonant inductance is added to assist the soft commutation of all the converter MOSFETs. The mathematical description of the operating principle and the main design equations of the converter are reported. Based on experiments, a 100 W prototype of the proposed battery charger achieves a flat conversion efficiency higher than 92 % over the wide 20 W – 95 W power range, with a peak of nearly 94 % at 40 W.

**Index Terms**—Quasi-resonant converter, battery charger, photovoltaic, soft-switching, Zero-Voltage Switching.

## I. INTRODUCTION

Sustainable Development Goal (SDG) 7 of the 2030 Agenda of the United Nations, by promoting the extension of affordable, reliable and sustainable energy systems, addresses the need to increase the Renewable Energy Sources (RES) inside the countries energy mix [1]. Beside generation, a consistent effort should be devoted to more reliable and efficient conversion and distribution systems. Among the photovoltaic (PV)-fed applications, increasing attention is devoted to battery charging, especially for stand-alone systems [2]. Battery chargers for PV-fed applications should be designed to achieve a high efficiency over a wide range of operating powers, to address the intrinsic variability of RES.

To achieve a high efficiency conversion, resonant power converters have become a promising alternative to conventional Pulse-Width Modulated (PWM) converters, thanks to the possibility to reduce or eliminate the switching losses, reduce the Electromagnetic Interference (EMI) and increase the power density [3].

While extensive attention is devoted to resonant power converters for photovoltaic-to-grid applications [4], fewer works are devoted to resonant PV-fed low-voltage battery chargers. Most of the low-voltage battery chargers exhibit buck-derived topologies endowed with auxiliary resonant networks to achieve the soft commutation of their switches. The quasi-resonant buck-derived converter in [5] includes an additional  $LC$  resonant network to achieve the Zero-Voltage Switching (ZVS) of the main MOSFET. However, a resonant peak across

the main MOSFET requires to double its voltage rating, and the measured peak and average charging efficiencies of the proposed converter are 87 % and 84 % respectively. Another buck-derived topology is presented in [6], which achieves the Zero-Current Switching (ZCS) turn-OFF of the main switch thanks to an additional  $LC$  tank and an auxiliary switch. However, the large current peak on the input MOSFET, the large voltage peak on the output diode and the 90.3 % peak efficiency remain the main issues of this converter. A PV-fed dual-stage converter is presented in [7], where a PWM boost-stage responsible for the Maximum Power-Point Tracking (MPPT) is followed by a half-bridge parallel-loaded resonant converter. Despite the desirable integration of MPPT, the relatively large component count and the adoption of a passive full-bridge rectifier results in a 88.7 % average and 92 % peak charging efficiency.

Aiming to achieve high conversion efficiency over a wide power range, a new PV-fed quasi-resonant converter is presented in this work. The topology is based on the grid-supplied constant power charger previously proposed in [8], but modified and optimized for a PV source. Differently from the above-mentioned topologies, the converter presented here exploits the parasitic capacitances of its switches to obtain soft commutation with an increase in power density. The rest of the paper is organized as follows: Section II describes the topology and operation of the converter. In Section III, the design of the converter is discussed in details. In order to validate the proposed approach, a 100 W prototype is built and the experimental results are presented in Section IV, while Section V draws the conclusions of this work.

## II. ANALYSIS

### A. Operating principle

This work explores the possibility to apply the operating principle adopted in the constant-power charger described in [8] to a different topology optimized for a PV-sourced application. The topology, illustrated in Fig. 1, consists in a quasi-resonant, frequency-modulated half-bridge inverting stage (MOSFETs  $M_1$  and  $M_2$  and capacitors  $C_1$  and  $C_2$ , with  $C_1 = C_2 = C$ ) followed by an active rectifier stage.

The input MOSFETs are controlled with 180° phase shift and nearly 50 % duty cycle, so as to generate a pure AC

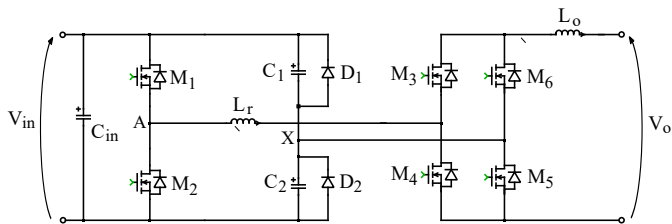


Fig. 1: Proposed quasi-resonant battery charger.

voltage between nodes  $A$  and  $X$ . Unlike conventional half-bridge converters, in which the capacitances are selected to be large enough to maintain a stable voltage at node  $X$ ,  $C_1$  and  $C_2$  are designed here to be alternately charged and discharged between  $0\text{ V}$  and the input voltage. The output current is responsible for the charge and discharge of the half-bridge capacitances.

Clamping diodes  $D_1$  and  $D_2$  are added in anti-parallel connection to avoid charging  $C_1$  and  $C_2$  above  $V_{in}$  or discharging them below  $0\text{ V}$ . This principle, denoted in [8] by Discontinuous Voltage Mode (DVM), allows to generate a triangular voltage across each capacitor and to transfer to the output a discretized amount of energy at each switching cycle.

An input capacitor  $C_{in}$  is added to the input port to stabilize the working point of the PV module.

The step-down transformer originally present in the grid-fed topology in [8] is here removed because of the lower input voltage of the targeted PV-fed application. A typical crystalline-Silicon PV module (with 48 up to 72 cells), indeed, exhibits Maximum Power Point voltages ( $V_{MPP}$ ) around few tens of volts, which do not need significant step-down to the low-voltage batteries.

An active rectifier, consisting of MOSFETs  $M_3$ ,  $M_4$ ,  $M_5$  and  $M_6$ , provides a full-wave rectification of the intermediate AC voltage. The choice of an active rectifier, despite the additional gate driving complexity, allows to eliminate the forward voltage drops of a passive diode-based rectifier. By considering, for instance, a  $12\text{ V}$  battery and Schottky diodes with  $0.4\text{ V}$  forward voltage, indeed, the diode conduction losses alone would imply almost  $7\%$  efficiency loss. Low  $R_{DS,ON}$  transistors are required to limit the influence of conduction losses on the conversion efficiency.

The additional small resonant inductor  $L_r$ , connected to the switching node  $A$  between the half-bridge MOSFETs, is specifically added to assist the ZVS turn-ON of  $M_1$  and  $M_2$ .

An inductor  $L_o$  filters the high-frequency harmonics of the output current  $I_o$  to provide a smooth charging of the output battery.

### B. Analysis of a switching cycle

This section provides the analysis of the main converter voltage and current waveforms through a switching period. Since the operation of the converter is symmetric, the description only considers a half period.

The mathematical analysis of a switching period presented here is based on the following assumptions:

- the input capacitor  $C_{in}$  is assumed to keep a constant DC input voltage  $V_{in}$ ;
- the output filter inductor  $L_o$  is assumed to keep a constant DC output current  $I_o$ ;
- the half-bridge MOSFETs  $M_1$  and  $M_2$  are ideal, except for their output parasitic capacitance  $C_s$ ;
- the forward voltage drops of the clamping diodes and MOSFETs body diodes are neglected;
- the reactive components  $C_1$ ,  $C_2$ ,  $L_r$  and  $L_o$  are lossless and ideal.

The working operation of the converter in a half switching period can be subdivided into 3 phases that are illustrated in Fig. 2.

1) *Power transfer phase (PT, Fig. 2a)*: During this phase,  $M_1$ ,  $M_3$  and  $M_5$  conduct the output current  $I_o$ , whereas  $M_2$ ,  $M_4$  and  $M_6$  are turned OFF. At node  $X$ ,  $I_o$  splits equally, gradually charging  $C_2$  and discharging  $C_1$ .  $V_x$  increases linearly from  $0\text{ V}$  to  $V_{in}$ , as shown in Fig. 3:

$$V_x(t) = \frac{I_o}{2C}t. \quad (1)$$

During this phase,  $L_r$  is connected in series to  $L_o$ . As a consequence, since  $I_o$  is assumed to be constant, no voltage drop appears across it. The rectifier primary voltage  $V_p$  assumes a triangular behaviour:

$$V_p(t) \approx V_A - V_x = V_{in} - \frac{I_o}{2C}t. \quad (2)$$

The secondary voltage  $V_s$  temporarily coincides with  $V_p$ . This phase ends when  $V_x$  has reached  $V_{in}$ .

2) *Current circulating phase (CC, Fig. 2b)*:  $M_1$ ,  $M_3$  and  $M_5$  are still ON. When  $V_x$  has reached  $V_{in}$ , the bypass diode  $D_1$  gets forward biased and clamps  $V_x$ , as shown in Fig. 3. The rectifier primary voltage  $V_p$  becomes zero and forces the body diodes of  $M_4$  and  $M_6$  to turn-ON, which start sinking current from  $M_3$  and  $M_4$ . A free-wheeling path for  $I_o$  is created and no power is temporarily transferred to the battery.

3) *Crossover resonant phase (CR, Fig. 2c-2e)*: This phase begins when  $M_1$  is turned OFF. During the dead-time,  $L_r$  starts resonating with the output parasitic capacitances of  $M_1$  and  $M_2$  ( $C_{s1} = C_{s2} = C_s$ ), as shown in Fig. 2c, pushing  $V_A$  below  $0\text{ V}$ , as illustrated in Fig. 3. This behaviour only occurs if the energy stored in the tank inductor  $L_r$  is sufficient to completely charge  $C_{s1}$ . This condition translates into a lower boundary for  $L_r$ :

$$L_r > \frac{2C_s V_{in}^2}{I_o^2}. \quad (3)$$

Once  $V_A$  reaches  $0\text{ V}$ , the body diode of  $M_2$  gets forward-biased and conducts the  $L_r$  current  $i_{L_r}$ , as shown in Fig. 2d. The voltage  $V_x$  (almost constant during this phase) appears across  $L_r$  and forces  $i_{L_r}$  to a linear decrease:

$$i_{L_r} = I_o - \frac{V_{in}}{L_r}t. \quad (4)$$

The difference between  $i_{L_r}$  and  $I_o$  flows through the body diodes of  $M_4$  and  $M_6$ .

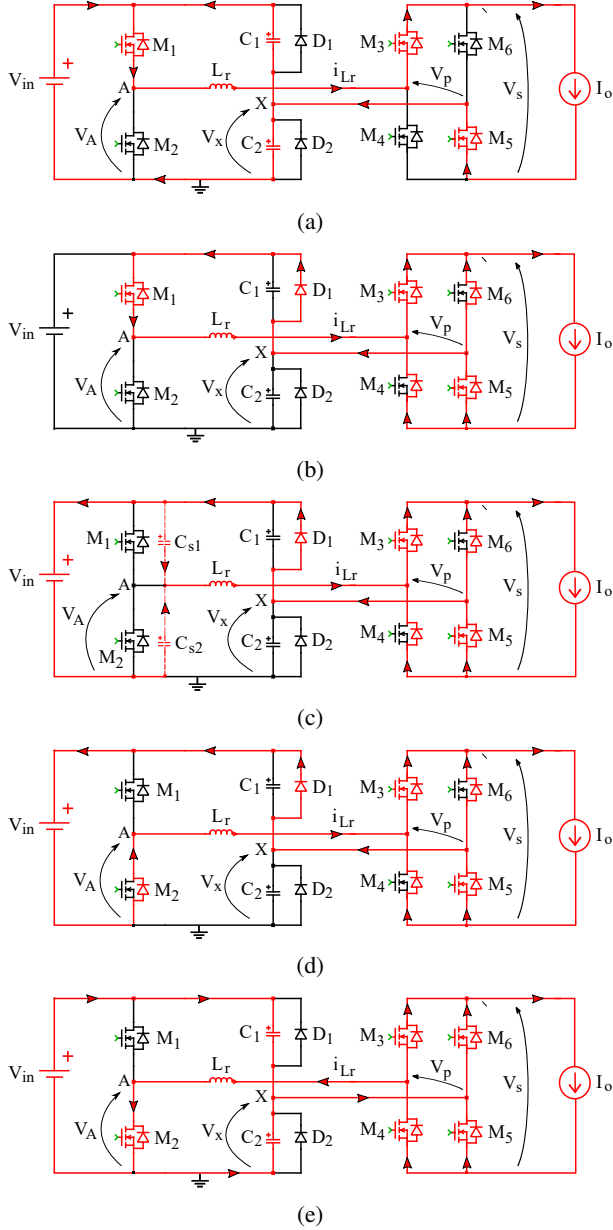


Fig. 2: Operation of the converter during a half switching period: (a) PT phase; (b) CC phase; (c) CR phase:  $L_r$  resonates with  $C_{s1}$  and  $C_{s2}$ ; (d) CR phase: the body diode of  $M_2$  starts conducting; (e) CR phase:  $M_2$ ,  $M_4$  and  $M_6$  turn-ON at zero voltage, and  $i_{L_r}$  inverts its polarity.

After a deadtime  $t_{dead}$ ,  $M_2$  is turned ON, as shown in Fig. 2e. If its body diode is still conducting, the commutation occurs at zero voltage, as schematically represented in Fig. 3. In this case, the energy stored in the parasitic capacitance of the turned-OFF MOSFET, instead of being dissipated, is recovered at the input. The maximum allowed deadtime  $t_{dead,max}$  to achieve ZVS is limited by the time required by the parasitic output capacitance  $C_{s2}$  of  $M_2$  to be fully discharged (denoted by  $t_1$ ), and by  $i_{L_r}$  to become null: when it inverts its polarity, indeed,  $L_r$  starts resonating again with the output

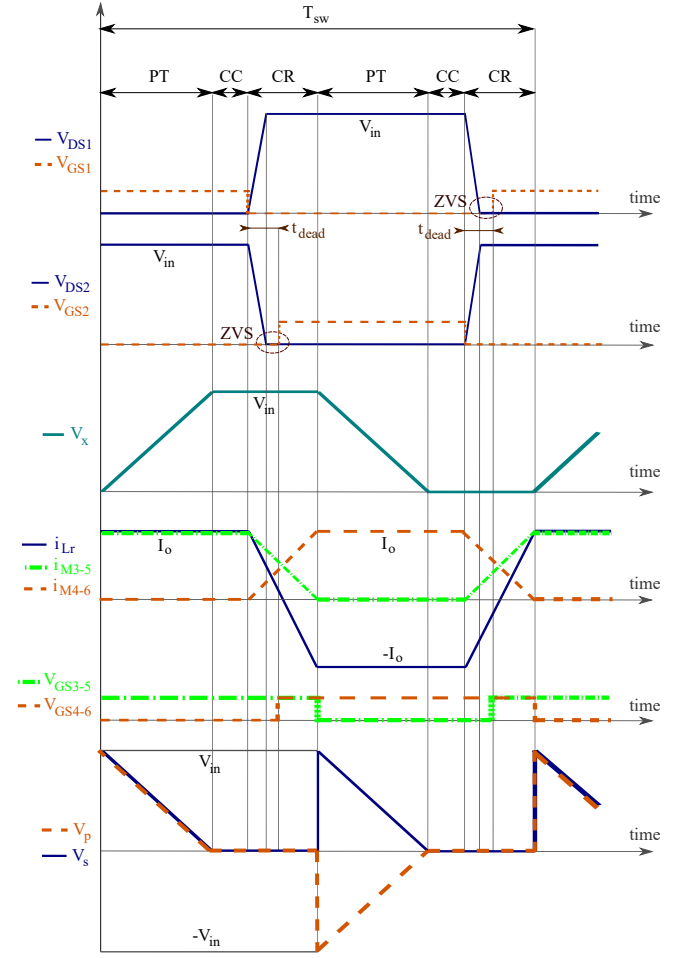


Fig. 3: Main voltage and current waveforms in a switching period.

capacitances of  $M_1$  and  $M_2$ , and the ZVS condition is lost. This maximum time can be analytically estimated assuming a linear current discharge:

$$t_{dead,max} \approx t_1 + \frac{L_r I_o}{V_{in}}. \quad (5)$$

Together with  $M_2$ , also  $M_4$  and  $M_6$  are turned ON, at zero-voltage. The Kirchhoff Current Law (KCL) applied at the output nodes allows to derive the source-to-drain MOSFETs currents as:

$$i_{M_3} = i_{M_5} = \frac{I_o}{2} + \frac{i_{L_r}}{2} \quad (6)$$

$$i_{M_4} = i_{M_6} = \frac{I_o}{2} - \frac{i_{L_r}}{2}. \quad (7)$$

From (6), if  $M_3$  and  $M_5$  are turned OFF when  $i_{L_r} = -I_o$ , ZCS commutation is achieved, as shown in Fig. 3. The CR phase is concluded when  $M_3$  and  $M_5$  are turned OFF. It is important to observe that the duration of this phase is exaggerated in Fig. 3 for a better visualization.

The previous analysis assumes that the switching period is long enough to allow  $I_o$  charging and discharging  $C_1$  and  $C_2$

between 0 V and  $V_{in}$ . If this is true, the transferred power can be simply computed by multiplying the energy stored and released by each capacitor  $C_1$  and  $C_2$  by the switching frequency:

$$P \approx 2CV_{in}^2 f_{sw}. \quad (8)$$

However, this condition occurs only if  $I_o$  can raise/lower the  $V_x$  voltage by  $V_{in}$ . Given a target peak current  $I_{o,max}$ , the condition holds for:

$$\frac{T_{sw}}{2} \geq 2C \frac{V_{in}}{I_{o,max}} \Rightarrow f_{sw} \leq \frac{I_{o,max}}{4CV_{in}} \triangleq f_{limit}. \quad (9)$$

For  $f_{sw} > f_{limit}$ , the output power starts decreasing non-linearly with the switching frequency. In this second operating mode,  $I_o$  charges and discharges only partially  $C_1$  and  $C_2$ , causing  $D_1$  and  $D_2$  to never enter in conduction. As a result,  $V_x$  assumes a triangular shape centered around  $V_{in}/2$  and the CC phase is not achieved.

Beside this, the PT and CR operating phases remain as before. Due to the partial charging of the dividing capacitors,  $V_p$  and  $V_s$  assume a trapezoidal behaviour.

It is important to observe that the battery charging voltage is the average of  $V_s$ , which is a direct consequence of the volt-second balance applied to  $L_o$ . This implies that, to ensure the desired battery charging:

$$\bar{V}_s \approx \frac{V_{in}}{2} \geq V_{batt} \Rightarrow V_{in} \geq \frac{V_{batt}}{2}. \quad (10)$$

Condition (10) dictates the minimum input voltage, i.e. the minimum number of series-connected cells that the input PV source should exhibit to satisfy the voltage constraint. Assuming monocrystalline silicon, a good estimate for the open circuit voltage is 0.55 V [9]: as such, a minimum number of 48 cells is required to ensure net power flow to a 12 V battery.

### III. DESIGN OF A 100 W PROTOTYPE

A physical prototype was designed and tested to validate the predicted theoretical and simulation results on the working operation, and to derive the converter performances in terms of conversion efficiency. The designed input voltage was selected to be below 30 V, corresponding to typical open-circuit voltages of 48-cell PV panels.

The converter MOSFETs exhibit the same current stresses ( $I_o/2$  RMS current and  $I_o$  peak current), but different voltage stresses. While  $M_1$  and  $M_2$  voltage is bounded by  $V_{in}$ , the rectifier MOSFETs are subjected to large voltage spikes when they are turned OFF. This phenomenon occurs because the difference between  $i_{L_r}$  and  $I_o$  flows in their parasitic capacitances, producing resonant spikes that require to increase their voltage rating. Due to the temporary shortage of silicon power devices, the same 100 V rated transistor was selected. Since the topology is designed to reduce or eliminate the switching losses, a low conduction resistance  $R_{DS,ON}$  (below 10 m $\Omega$ ) is determinant to obtain a high-efficiency conversion.

The adopted Si-MOSFETs, can be turned ON with  $V_{GS} = 5$  V. A dual-output DC-DC converter was adopted to generate the supply voltages for the half-bridge and rectifier MOSFETs from  $V_{in}$ . Three half-bridge gate drivers were selected, which rely on external bootstrap networks to drive the high-side MOSFETs.

The dividing capacitors  $C_1$  and  $C_2$  are subjected to a significant RMS current stress  $\frac{I_o}{2}$ , requiring a low ESR and large stability to frequency variations. On the other hand, their working voltage is limited by  $V_{in}$ , thanks to the clamping diodes action. The capacitance value is a design parameter linked to the desired rated power, at rated source voltage and boundary frequency conditions, as determined in Eq. (9). In the present design, assuming 100 W rated power at 28 V input voltage, 12 V battery voltage and 60 kHz operation, the required capacitance must satisfy:

$$C \leq \frac{P_{rated}}{4f_{limit}V_{in}V_{batt}} \approx 1.24 \mu\text{F}. \quad (11)$$

The adopted Multi-Layer Ceramic Capacitor (MLCC) is characterized by 50 V<sub>DC</sub> rated voltage, 12 A<sub>RMS</sub> rated current at 100 kHz and 940 nF capacitance.

The input capacitor  $C_{in}$ , responsible for stabilizing the working point of the PV panel was selected according to the allowed input current ripple. This limit can be linked to the deterioration of the output power of a PV panel when it is forced to provide strongly rippled current.

Elkhateb et al. in [10], exploiting a Single-Diode Model (SDM), derived an analytic relation between the current ripple  $\Delta I_{RMS}$  and the power decrease  $\Delta P_{ripple}$  of a PV panel:

$$\frac{\Delta P_{ripple}}{P_{MPP}} \approx 10.67 \left( \frac{\Delta I_{RMS}}{I_{MPP}} \right)^2. \quad (12)$$

By applying this approach to the equivalent SDM of a commercial poly-crystalline silicon 48-cell, an approximated constraint was derived for the capacitor ESR:

$$ESR \ll 650 \text{ m}\Omega. \quad (13)$$

From the relation of the RMS currents applied at the input node, an approximated expression for the RMS capacitor current  $i_{C_{in},RMS}$  can be derived:

$$i_{C_{in},RMS} \approx 2Cf_{sw}(V_{in} + 2V_{fd})\sqrt{\frac{V_{in}}{2V_{batt}} - 1}, \quad (14)$$

where  $V_{fd}$  is the forward voltage drop of the clamping diodes. Assuming the above-mentioned worst-case conditions,  $i_{C_{in},RMS} \approx 1.34$  A. An aluminum electrolytic capacitor was selected, exhibiting 63 V rated voltage, 750  $\mu\text{F}$  capacitance, 68 m $\Omega$  ESR and 2.5 A rated ripple current.

The inductor  $L_o$  was sized according to the maximum allowed current ripple overimposed to the average charging current. Application Notes like [11] recommend to limit the ripple current in *ampere* below a value equal to 1/20 of

the battery capacity, expressed in *ampere-hour*. Considering a 50 A h battery, for instance, the ripple current should be maintained below 2.5 A.

By integrating the  $L_o$  voltage, an approximated value of the parabolic current ripple can be determined:

$$\Delta I_{o,\text{ripple}} \approx \frac{V_{\text{in}}}{12f_{\text{sw}}L_o} < 2.5 \text{ A}. \quad (15)$$

The current rating should consider the maximum charging current ( $\approx 8 \text{ A}$  for a 100 W operation). A ferrite-core, wire-wound inductor was selected, with  $8.8 \text{ m}\Omega$  DC resistance, 13 A saturation current for 30% inductance decrease, and 17.5 A maximum current for a temperature increase of  $40^\circ\text{C}$ . Its  $47 \mu\text{H}$  inductance satisfies Eq. (15) for the rated power condition. The DC losses of this component at the maximum power condition are estimated to weigh for around the 0.6% of the total power.

The inductance value of  $L_r$ , investigated in details in this work, determines two concurrent consequences:

- the maximum allowed deadtime to achieve ZVS of the half-bridge MOSFETs, as described in (3).  $L_r$  should be large enough to relax the timing constraints imposed on the controller and the gate drivers;
- on the other hand, an increased inductance value increases the reactive power absorbed by  $L_r$ , in turns decreasing the power peak of the static characteristic and reducing  $f_{\text{limit}}$ .

A trade-off value of 330 nH was selected iteratively relying on *LTspice XVII* simulations [12]. According to (3), this value, combined with the MOSFETs parasitic  $C_s = 640 \text{ pF}$  and with  $V_{\text{in}} = 28 \text{ V}$ , satisfies the necessary condition for ZVS for any output current larger than 1.23 A. This consideration has important consequences on the behaviour of the conversion efficiency: it states that  $L_r$  value provides a minimum operating power above which a deadtime exists such that ZVS can be achieved. As a result, the switching losses, which may be impactful at light loads conditions, are basically eliminated on a wide range of larger operating powers, if a proper deadtime is selected. It is meaningful to observe that the ZVS condition is achieved exploiting a small inductor and the output parasitic capacitances of the half-bridge MOSFETs, with benefits on the power density.

A ferrite-core inductor was selected, exhibiting low DC resistance ( $1.3 \text{ m}\Omega$ ), 36.5 A rated current for  $40^\circ\text{C}$  temperature increase, and 62 A saturation current for a 20% inductance decrease.

Tab. I summarizes the selected components for the physical prototype, while Fig. 4 shows the top view of the physical PCB prototype of quasi-resonant battery charger.

#### IV. EXPERIMENTAL RESULTS

The aim of the experimental testing was to prove the coherence of the measured open-loop operation with the theoretical analysis and extract meaningful measurements of efficiency. The experimental testbench is illustrated in Fig.

TABLE I: Main converter components for the physical prototype.

Component	Part code	Manufacturer
MOSFETs $M_{1,6}$	TPH4R10ANLL1Q	Toshiba
Resonant inductor $L_r$	IHLP5050CEERR33M01	Vishay
Dividing capacitors $C_{1,2}$	C1812C944J5JLC7805	KEMET
Input capacitor $C_{\text{in}}$	UC21J751MNS1MS	Nichicon
Output filter inductor $L_o$	74437529203470	Würth Elektronik
Clamping diodes $D_{1,2}$	V8PAL45HM3_A/I	Vishay
Half-bridge gate drivers	ADUM3223WARZ	Analog Devices
Dual-output DC-DC converter	PRQ3W-Q48-D55-S	Cui Inc.

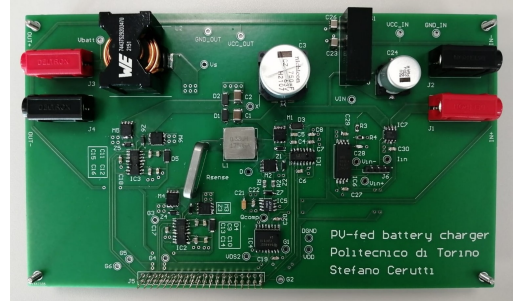


Fig. 4: Top view of the 100 W PCB prototype.

5. A DC power supply and a programmable electronic load were adopted as source and load, respectively. The switching functions to drive the MOSFETs were generated by Intel Cyclone V FPGA on Terasic De1-SoC board, through a Finite State Machine algorithm.

Fig. 6 shows some of the acquired experimental waveforms. Specifically, Fig. 6a depicts the steady-state behaviour of  $V_{\text{DS}2}$ ,  $V_x$  and  $i_{L_r}$ . The measurements refer to  $V_{\text{in}} = 27.5 \text{ V}$ ,  $V_{\text{batt}} = 12 \text{ V}$ ,  $f_{\text{sw}} = 45 \text{ kHz}$  and  $t_{\text{dead}} = 80 \text{ ns}$ . The measured waveforms are coherent with the predicted behaviour of the converter in the DVM, since  $f_{\text{sw}} < f_{\text{limit}} \approx 48.4 \text{ kHz}$ .

Fig. 6b shows a detail of the ZVS turn-ON of  $M_2$  with the adopted deadtime value. As visible, since  $V_{\text{GS}1}$  toggles to 5 V before  $i_{L_r}$  reverses polarity, the body diode of  $M_2$  is conducting and ensures the zero-voltage turn-ON.

Fig. 7 reports some efficiency plots referring to different source and load voltage conditions, at a fixed 80 ns deadtime. The switching frequency was varied up to  $f_{\text{limit}}$  to modify the operating power: for each working point, the conversion

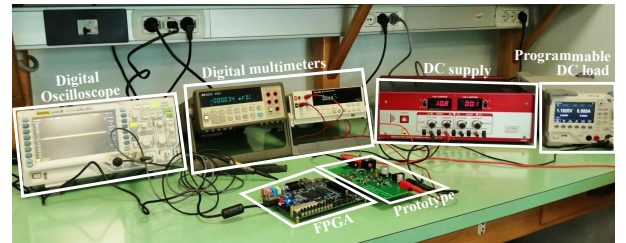


Fig. 5: Testbench for the experimental validation of the prototype.

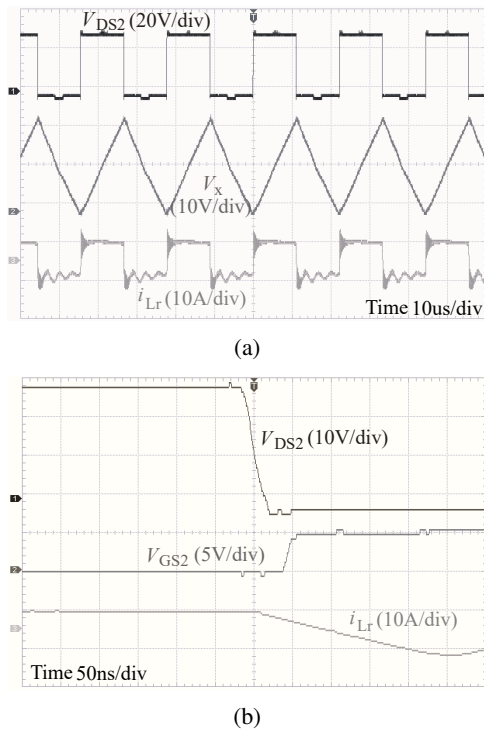


Fig. 6: Experimental waveforms of the converter: (a)  $V_{DS2}$ ,  $V_x$  and  $i_{Lr}$ ; (b) Zoom on  $V_{DS2}$ ,  $V_{GS2}$  and  $i_{Lr}$  during the ZVS turn-ON of  $M_2$ .

efficiency was computed by including also the gate driving losses. The results show an almost flat efficiency curve independently on the source and load conditions, for operating powers larger than 20 W, and a peak efficiency of 94.5%. The selected deadtime ensures ZVS for almost all the power range, allowing to avoid the frequency-dependent increase of the switching losses. A flat efficiency curve is a desirable feature of PV-fed systems, due to the need to ensure high efficiency over a wide range of operating powers, intrinsic characteristic of RES. This is the reason why this converter is considered to be suitable for PV applications. At low power operations, the ZVS condition is lost and a minimum of 84% efficiency is measured at 5 W.

## V. CONCLUSIONS

This work proposed a new quasi-resonant battery charger designed to achieve the ZVS of its switches. The quasi-resonant behaviour exploits a small additional inductor and the parasitic capacitances of the MOSFETs, allowing to decrease the overall component count. The adoption of an active rectifier and the selection of low  $R_{DS,ON}$  MOSFETs allow to decrease the conduction losses, while the ZVS minimizes the switching losses over a wide range of operating powers. A 100 W prototype is designed and tested to validate the operating principle and measure the conversion efficiency. The experimental results are in agreement with the expected operation and prove that the charger is able to achieve an almost flat efficiency over the wide 20 W – 95 W operating range with

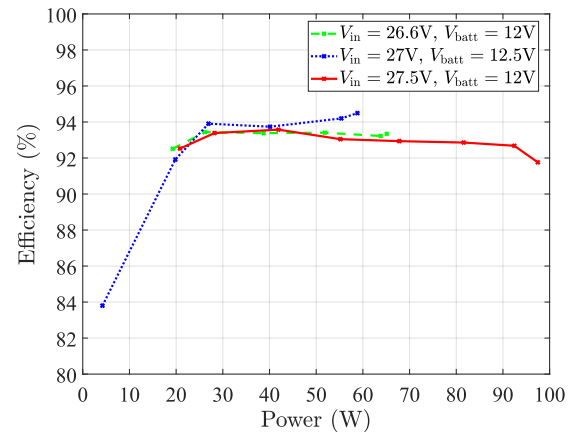


Fig. 7: Measured conversion efficiency as function of operating power, for different source and load voltages.

94% peak. Below 20 W operation, the efficiency decreases because of the absence of ZVS condition and reaches 84% at 5 W operation.

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