A 28 nm 368 fJ/cycle, 0.43%/V Supply Sensitivity, FLL based RC Oscillator Featuring Positive TC Only Resistors and M Based Trimming

A 28-nm 368-fJ/cycle, 0.43%/V Supply-Sensitivity, FLL-based RC Oscillator Featuring Positive-TC-Only Resistors and ΔΣM-Based Trimming

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***Abstract*— This Brief presents a process-scaling-friendly frequency-locked-loop (FLL)-based RC oscillator. It features an R-R-C frequency-to-voltage converter that entails resistors with only the same-sign temperature coefficients. Together with a low-leakage switched-capacitor resistor and a delta-sigma-modulator-based trimming, our 71.8-MHz RC oscillator in 28-nm CMOS achieves a frequency inaccuracy of 77.6 ppm/°C, a 0.43%/V supply sensitivity, and an 11-ps$_{rms}$ period jitter. The energy efficiency is 368 fJ/cycle.**

***Index Terms*—Frequency-locked-loop (FLL), RC oscillator, CMOS, temperature coefficients, switched-capacitor resistor, delta-sigma-modulator, frequency inaccuracy, energy efficiency.**

I. Introduction

Recently, the rapid development of battery-powered internet-of-thing (IoT) applications keeps demanding low-power and temperature-resilient kHz-to-MHz clock sources. On-chip RC oscillator is one of the promising candidates due to its low-cost integration and high energy efficiency, which has made significant progress in performance (e.g. <10ppm/ºC temperature sensitivity). However, they are detained mostly in mature process nodes, such as 65nm [1-6] and 180nm [7-11], because they rely on combining various foundry-supported resistors with positive and negative temperature coefficients (TC) to compensate for the temperature sensitivities of on-chip resistors and RC oscillators (Fig. 1). Unfortunately, resistors with both positive and negative TCs are unavailable in finer CMOS process nodes, e.g., only positive-TC resistors in 28nm, or only negative-TC thin-film metal resistors in 5nm. Additionally, the off-state leakage current (I_{leak}) of the finer-length MOS switches severely deteriorates the frequency instability. There are alternatives to nullify the temperature effect, e.g., by tuning the comparator delay [12] or adding a bandgap reference [13], but the achieved frequency stability is inferior (158ppm/ºC in [12]), or the power penalty becomes too large (840μW in [13]).

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In view of the aforementioned considerations, this brief proposes a *process-scaling-friendly* frequency-to-voltage converter (FVC). It performs temperature compensation with two same-sign-TC resistors, i.e. only positive-TC or only negative-TC. In the proposed 28nm CMOS circuit, we realize the RC oscillator based on the R_P-R_P-C FVC, embedded in the frequency-locked loop (FLL) for improving the frequency stability and energy efficiency. Besides, we propose a delta-sigma-modulator (ΔΣM)-based voltage-domain trimming scheme to achieve precise TC compensation, and a low-leakage switched-capacitor resistor (SCR) to hinder the off-state leakage current of the MOS switches.

The rest of this brief is organized as follows, Section II introduces the proposed R_P-R_P-C FVC, Section III describes the proposed RC oscillator architecture and key building blocks. Experimental results are presented in Section III, and the key contributions of this brief are summarized in Section IV.

II. Proposed R_P-R_P-C FVC

From Fig. 1 (left), a common frequency-to-voltage converter (FVC) consists of two types of switched-resistor banks with opposite-sign TC and a capacitor, designated (R_P+R_N)-C network. However, the finite number of switched banks limits the compensation accuracy, and the switch's leakage current can incur nonlinear frequency instability. The delta-sigma-modulator (ΔΣM)-based switched-resistor scheme [2], (R_P//R_N)-C, can precisely cancel the opposite-sign resistive TCs with only two switches (Fig. 1, middle). Yet, both above FVCs entail two opposite-sign-TC resistors, limiting their commonness in advanced processes.

Herein, we introduce two same-sign-TC resistors to avert such a constraint (Fig. 1, right). Our *process-scaling-friendly* R_P-R_P-C FVC incorporates a series connection of two same-sign-TC resistors and a switched-capacitor resistor (SCR). The feedback voltage (V_F) taken from the middle of the two resistors feeds the succeeding integrator. Previous works simply divide the reference voltage (V_{REF}) of the integrator from the supply voltage (V_{DD}) using the same-type resistors. Adjusting V_{REF} only can alter the output frequency but not the temperature dependence. Interestingly in the proposed FVC, V_{REF} can effectively adjust the equivalent resistance ratio. Specifically, with V_{REF}=xV_{DD}, the equivalent resistance of the FVC becomes

$$R_{\mathrm{eq}} = x/(1-x)\cdot R_{\mathrm{P1}} - R_{\mathrm{P2}} \qquad (1)$$

where x denotes the scaling ratio of V_{REF} with respect to V_{DD}. The equivalence of resistance subtraction allows the feasibility of TC cancellation by two same-sign-TC resistors. Specifically, the TC of R_{eq} can be given as:

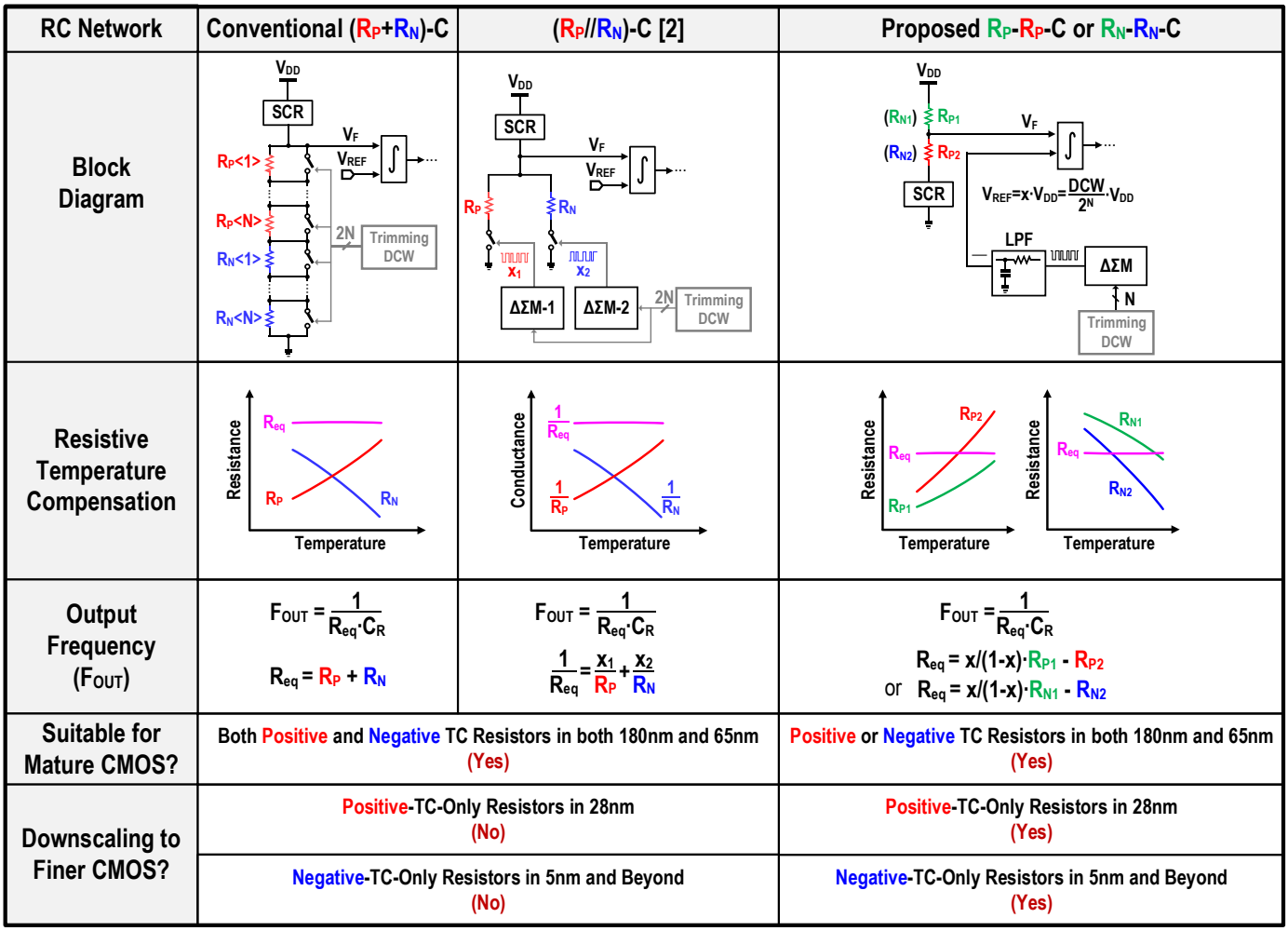

Fig. 1. Key features of different RC networks for temperature compensation.

$$TC(R_{eq}) = \frac{x/(1-x)\cdot R_{P1}\cdot \alpha_{P1} - R_{P2}\cdot \alpha_{P2}}{x/(1-x)\cdot R_{P1} - R_{P2}} \quad (2)$$

where α_{P1} and α_{P1} are the first-order TC of R_{P1} and R_{P2} respectively. Furthermore, we can modify the proposed FVC as R_N-R_N-C to be compatible with advanced nodes offering only negative-TC thin-film metal resistors, e.g., in 5nm and beyond. As shown in Fig. 2, by tailoring the V_{REF} value via a delta-sigma-modulator (ΔΣM)-based digital-to-analog converter, the temperature trimming can reach a very fine resolution without any additional switches.

III. Proposed RC Oscillator Architecture

Fig. 3 depicts the schematic of our RC oscillator consisting of an FLL and a ΔΣM-based V_{REF} generator. The R_P-R_P-C network embraces an R_{P1} (1.26MΩ non-silicided p-poly resistor), an R_{P2} (264kΩ non-silicided n-diffusion resistor), and a 6-bit tunable switched-MOM capacitor C_R (1pF at middle banks). Here, the filtering networks (R_{F1}=678kΩ, C_{F1}=10pF, and C_{F2}=40pF) connect at the V_F node to stabilize the FVC operation and reduce the voltage ripple. The integrator features a chopper-stabilized folded-cascode operational transconductance amplifier with a PMOS input pair cascaded by a common-source amplifier and has a high DC gain (~100dB). Due to the high DC loop gain, V_F=V_{REF} holds in a steady-state regardless of V_{DD}, which results in a good supply sensitivity of the output frequency (F_{OUT}). Moreover, we introduce a subthreshold proportional to an absolute temperature (PTAT) current reference together with a bias voltage generator to uphold a high DC gain over temperature and supply variations. Thick-oxide transistors hinder the temperature-sensitive leakage currents of the integrator and its bias circuitry. Considering the low bandwidth of the subthreshold amplifier, we select the chopper frequency as f_{VCO}/1024, where f_{VCO} is the voltage-controlled oscillator (VCO) frequency. Besides, we set C_{INT}=39pF to define the dominant pole of the loop dynamics, while C_L=15pF at the V_C node to attenuate the chopping ripple. The VCO is a 3-stage inverter-based ring oscillator. To suppress the VCO frequency variation over PVT variations, we load each inverter with a fixed resistor and a 4-bit tunable capacitor[2]. The choice of a non-silicided n-diffusion resistor results from its high positive TC (2569ppm/°C), which can compensate for the aggressive frequency elevation of VCO with temperature. A 4-bit MOM capacitor array and a MOS varactor perform coarse- and fine-frequency tunings, respectively. The division of the VCO output by 32 with a boosted swing generates the non-overlapping clocks ($\varphi_{1,2}$) for the SCR. A 1st-order ΔΣM

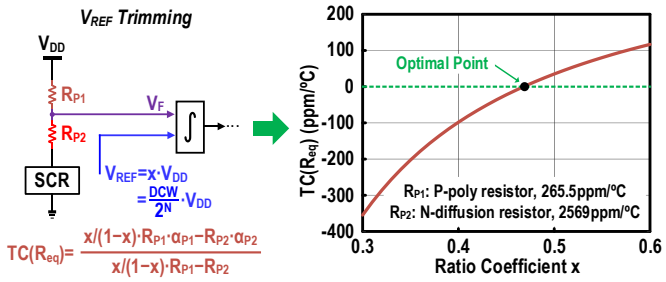

Fig. 2. The principle of the temperature coefficient trimming.

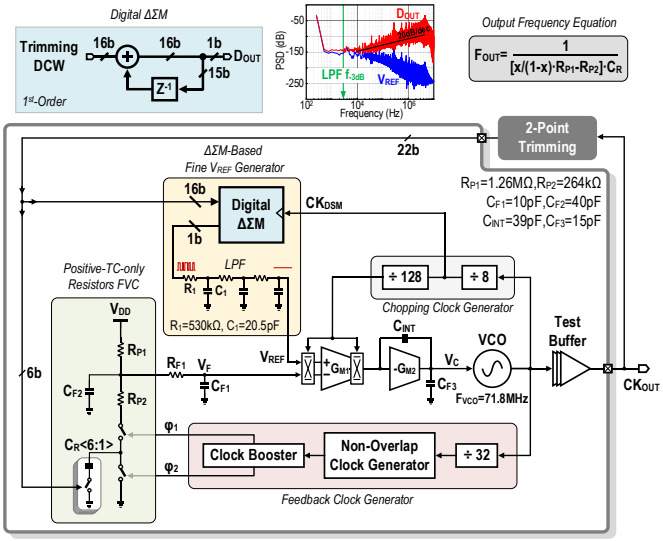

Fig. 3. Block schematic of the proposed R_P-R_P-C FLL-based RC oscillator along with a ΔΣM-based fine-tuning V_{REF} generator.

followed by a 3rd-order RC lowpass filter (LPF) realizes the V_{REF} generator. From Fig. 3 (top), to suppress the ΔΣM quantization noise and avert degrading the output clock jitter, we set the cut-off frequency of the LPF at ~2.8kHz. With a 16-bit digital control word (DCW), a very fine tune of V_{REF}=xV_{DD} is achievable against PVT variations. The ΔΣM clock frequency is f_{VCO}/8.

The I_{leak} of MOS switches affects the equivalent resistance of the SCR. For instance, the simulated I_{leak} of an NMOS (1µm/30nm) is ~100nA at 60 ºC in our 28nm node, and it climbs intensely with the temperature (Fig. 4, bottom). This leakage-incurred instability is nonlinear and hard to compensate. Downscaling the switch size can moderately reduce the I_{leak}, but the switch's turn-on resistance (R_{on}) will substantially increase. We realize that applying a negative gate-to-source voltage (V_{GS}) of -V_{DD} can stem the I_{leak} into the sub nA regime even at a high temperature while R_{on} remains unchanged. Inspired by this negative V_{GS} concept, we propose a low-leakage SCR by featuring a clock booster and a super-cut-off switch to tackle the leakage current effectively, as detailed in Fig. 4 (right). The clock booster doubles the clock swing [-V_{DD}, V_{DD}], and the negative V_{GS} (-V_{DD}) holds during the off period of $\varphi_{1,2}$. Similarly, with an inverter inserted between the gate and source nodes of the MOS switch, we obtain a super-cut-off switch. Simulations verified that the low-leakage SCR exhibits a temperature-insensitive equivalent resistance even using low-threshold transistors.

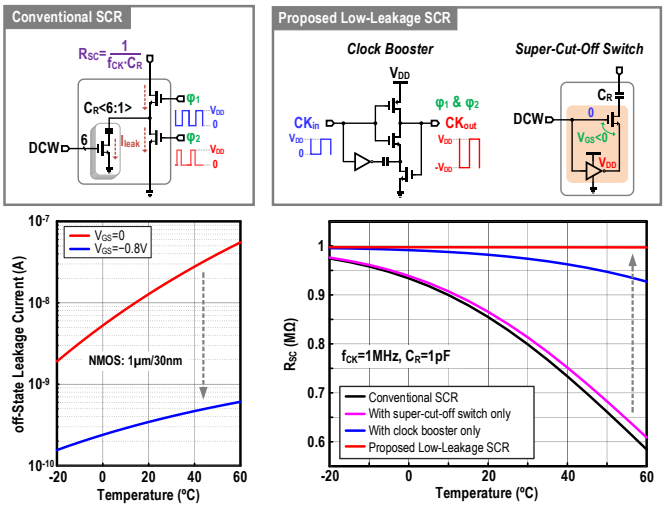

Fig. 4. Proposed low-leakage SCR combining clock booster and super-cut-off switch.

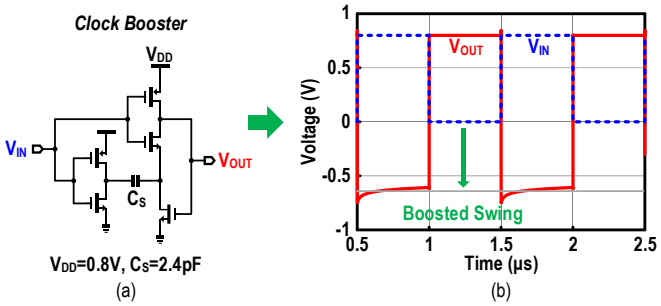

Fig. 5. Circuit detail of (a) the clock booster (a) and (b) its simulated transient waveform.

Fig. 5 shows the schematic and simulated transient waveforms of the proposed clock booster. The conventional bootstrapped inverter can deliver an output voltage between -V_{DD} and 2V_{DD}, which is advantageous for low voltage applications [14]-[15]. Here, as shown in Fig. 5, to avoid relibility issue, we modified the boostrapped inverter to constrain the voltage swing to [-V_{DD}, V_{DD}]. Thus, the drived mos switches can work stably under standard supply voltage while the leakage current is greatly suppressed.

IV. Measurement Results

A prototype FLL-based RC oscillator is fabricated in 28-nm CMOS technology, the die micrograph is shown in Fig. 6, and the core area is 0.038mm^2. At V_{DD}=0.8V, the oscillator operates at 71.8 MHz while dissipating 26.4 µW dominated by the VCO. The result corresponds to an energy efficiency of 368 fJ/cycle. Fig. 7(a) shows the measured frequency variations when sweeping the ΔΣM DCW and FLL is turned off. As shown in Fig. 7(a), the free-running VCO frequency rises by 2.3% over -20 to 60 ºC, while the closed-loop frequency TC varies from negative to positive as expected. Thus, the ΔΣM DCW executes the 2-point trimming digitally. After choosing the optimal ΔΣM DCW, we then tune the DCW of C_R to calibrate the absolute oscillation frequency. As shown in Fig. 7(b), the average supply sensitivity is 0.43%/V when V_{DD} varies from 0.8 to 1 V.

TABLE.I PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART.

	This Work	JSSC'21 [12]	JSSC'22 [13]	JSSC'22 [2]	JSSC'19 [1]	JSSC'22 [7]
Oscillator Architecture	Analog FLL	RxO $	RxO with FEF	Analog FLL	RxO with DFC	Analog FLL
CMOS Process (nm)	28	28	5	65	65	180
Area (mm^2)	0.038	0.0052	0.0152	0.18	0.051	0.168
Frequency (MHz)	71.8	2.1	77	32	1.05	1.387
Power (μW)	26.4	1.4	840	34	69	1.23
Supply Voltage (V)	0.8-1	0.35-0.38	1.1-1.35/0.9	1.1-2.3	0.98-1.02	1.2-1.9
Supply Sensitivity (%/V)	**0.43**	83.3	2	0.008 *	4.25	0.57
Energy Efficiency (pJ/Cycle)	**0.368**	0.67	10.91	1.06	65.7	0.89
No. of Trimming Points	2	3	2	2	Temp. Sensor	2
Temperature Range (ºC)	-20 to 60	-20 to 120	-40 to 125	-40 to 85	-15 to 55	-40 to 80
Temperature Coefficient (ppm/ºC)	77.6	158	36	8.7	4.3	34.4
Temperature Dependance & Compensation Method	**R_P-R_P-C & V_{REF} Trimming**	Delay Trimming Banks	Bandgap V_{REF} Trimming	(R_P//R_N)-C Switched	(R_P+R_N) & 1-bit Temp.Sensor	(R_P+R_N) Impedance Sensing
Period Jitter (ps_{rms})	**11 (790 ppm)**	800 (1680 ppm)	59.7 (4597 ppm)	22.3 (714 ppm)	160 (168 ppm)	3187 (4090 ppm)
No. of Tested Samples	7	7	8/16 #	6	1	4
Allan Deviation (ppm)	58.6	210	N/A	2.5	N/A	15
FOM_{Jitter} (dB) &	**-235**	-211	-205	-228	-208	-199

$ *Relaxation Oscillator* * *With on-chip LDO* # *8 for temperature variations and 16 for supply variations*
& $FOM_{Jitter}=10*log(\sigma^2_{jitter}*Power/1mW)$

A	Amplifier + Bias Circuit	E	VCO
B	V_{REF} Generator	F	FVC
C	Chopping Clock Generator	G	Loop Filter
D	Feedback Clock Generator	H	Test Buffer
Total Core Area: 0.038mm²			

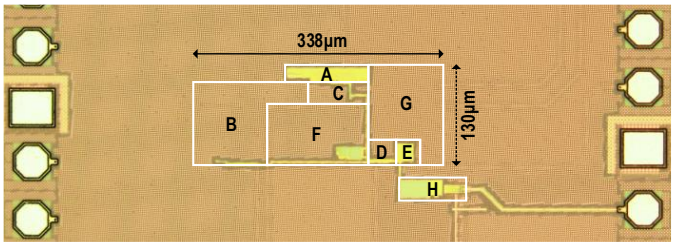

Fig. 6. Chip micrograph of our RC oscillator prototyped in 28nm CMOS.

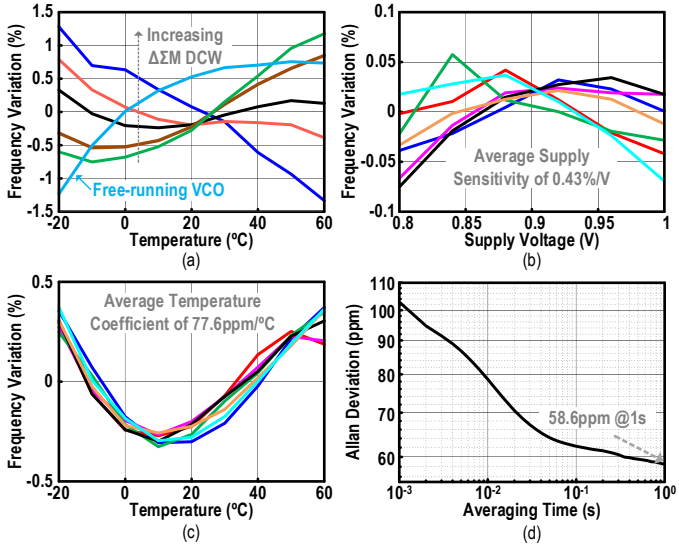

Fig. 7. Measured ΔΣM-tuning effect (a), frequency variation versus supply voltage (b) and temperature (c), and Allan deviation (d).

The decent supply dependency results from the supply-insensitive SCR and switchless trimming scheme. Fig. 7 (c) depicts the measured frequency variations of 7 samples over -20 to 60 ºC, and the average TC is 77.6 ppm/ºC. The Allan deviation for a 1-second stride is 58.6 ppm (shown in Fig. 7(d)). Fig. 8 shows the measured period jitter and accumulated jitter. The output period jitter is $11ps_{rms}$ (790ppm of the period), and the accumulated jitter over 10,000 cycles is $1.77ns_{rms}$. The chopping scheme helps suppress the 1/f noise and offset of the integrator, and the achieved jitter-power FOM is -235dB.

Table. I compares our positive-TC-only resistors-based RC oscillator with recent on-chip RC oscillators. The proposed techniques allow our design to exhibit higher energy efficiency and jitter-power FOM than all [1-2, 7, 12-13]. Benchmarking with [12] using the same process, our design achieves better frequency accuracy, jitter performance, and long-term stability. Compared to [13] in 5-nm FinFET that necessitates a power-hungry bandgap reference, our work is 29x more energy-efficient. Fig. 9 shows the benchmarks of the temperature coefficient and supply sensitivity versus the energy efficiency for this work with respect to the recent MHz-range RC oscillators. The proposed RC oscillator achieves a competitive temperature and supply stability with the lowest energy efficiency.

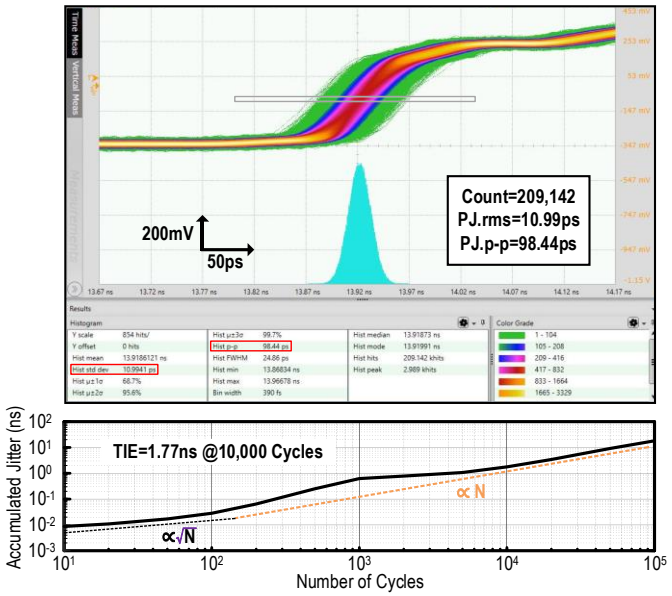

Fig. 8. Measured period jitter and accumulated jitter.

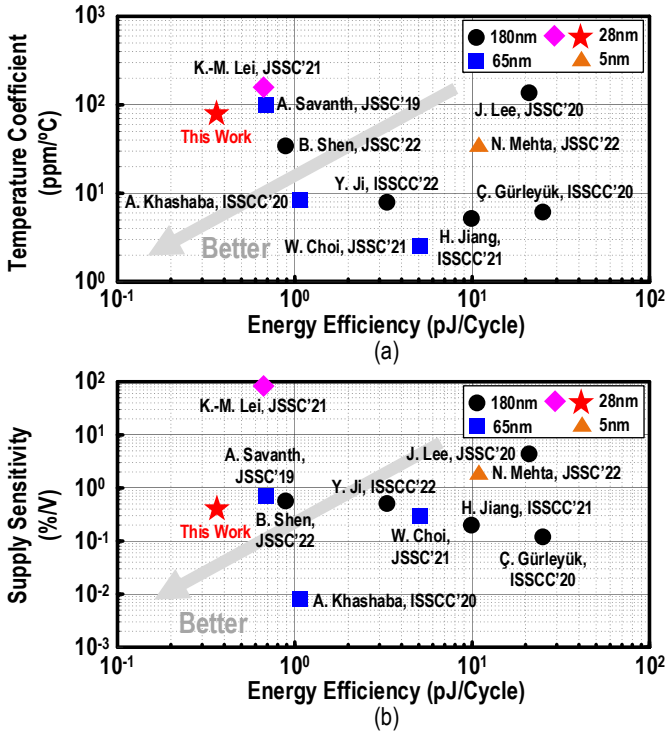

Fig. 9. Benchmarks of the temperature coefficient and supply sensitivity versus the energy efficiency.

V. Conclusion

This paper reported a process-scaling-friendly RC oscillator that allows the use of same-sign TC resistors. This architectural advantages favors technology downscaling in very advanced nodes, e.g., 5 nm, with mainly the metal resistors (same-sign TC). Protptyped in 28nm CMOS technology, the proposed FLL-based 71.8-MHz RC oscillator achieves a frequency inaccuracy of 77.6 ppm/°C, a 0.43%/V supply sensitivity, and an 11ps$_{rms}$ period jitter. The energy efficiency is 368fJ/cycle and the jitter-power FOM is -235 dB.

References

[1] N. Liu, *et al.*, "A 2.5 ppm/°C 1.05-MHz relaxation oscillator with dynamic frequency-error compensation and fast start-up time," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 1952–1959, Jul. 2019.

[2] A. Khashaba, *et al.*, "A 32-MHz, 34-µW temperature-compensated RC oscillator using pulse density modulated resistors," *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1470–1479, May 2022.

[3] T. Wang, *et al.*, "A 6µW ±50 ppm/°C ±1500 ppm/V 1.5 MHz RC oscillator using self-regulation," *IEEE Trans. on Circuits and Syst. II: Express Briefs*, vol. 66, no. 8, pp. 1297–1301, Aug. 2019.

[4] W. Zhou, *et al.*, "A 3-MHz 17.3-µW 0.015% period jitter relaxation oscillator with energy efficient swing boosting," *IEEE Trans. on Circuits and Syst. II: Express Briefs*, vol. 67, no. 10, pp. 1745–1749, Oct. 2020.

[5] Y. Li, *et al.*, "A 20-µs turn-on time, 24-kHz resolution, 1.5–100-MHz digitally programmable temperature-compensated clock generator," *IEEE J. Solid-State Circuits*, Early Access.

[6] W. Choi, *et al.*, "A 0.9-V 28-MHz highly digital CMOS dual-RC frequency reference with ±200 ppm inaccuracy from −40 °C to 85 °C *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2418–2428, Aug. 2022.

[7] B. Shen, *et al.*, "A frequency-locked oscillator using complex RC impedance IQ-balancing," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 677–687, Mar. 2022.

[8] J. Lee, *et al.*, "An ultra-low-noise swing-boosted differential relaxation oscillator in 0.18-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2489-2497, Sept. 2020.

[9] J. Zheng, *et al.*, "Relaxation oscillator with dynamic comparator and slope-boosting technique," *IEEE Trans. on Circuits and Syst. II: Express Briefs*, vol. 65, no. 10, pp. 1330–1334, Oct. 2018.

[10] K. -W. Cheng, *et al.*, "Design and analysis of a resistive frequency-locked oscillator with long-term stability using double chopper stabilization," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Early Access.

[11] Y. Ji, *et al.*, "A second-order temperature-compensated on-chip R-RC oscillator achieving 7.93ppm/°C and 3.3pJ/Hz in -40°C to 125°C temperature range," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 64–66, Feb. 2022.

[12] K.-M. Lei, *et al.*, "A 0.35-V 5,200-µm^2 2.1-MHz temperature-resilient relaxation oscillator with 667 fJ/cycle energy efficiency using an asymmetric swing-boosted RC network and a dual-path comparator," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2701–2710, Sep. 2021.

[13] N. Mehta, *et al.*, "An on-chip relaxation oscillator in 5-nm FinFET using a frequency-error feedback loop," *IEEE J. Solid-State Circuits*, vol. 57, no. 10, pp. 2898–2908, Oct. 2022.

[14] Y. Ho, *et al.*, "A 0.2–0.6 V ring oscillator design using bootstrap technique," in *Proc. IEEE* Asian *Solid-State Circuits Conf. (A-SSCC)*, pp. 333–336, Nov. 2011.

[15] K. -M. Lei, *et al.*, "A 0.4 V 6.4 µW 3.3 MHz CMOS bootstrapped relaxation oscillator with ±0.71% frequency deviation over −30 to 100 °C for wearable and sensing applications," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, May 2018.