Design and Testing of an Automotive Compliant 800V 550 kVA SiC Traction Inverter with Full-Ceramic DC-Link and EMI Filter

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***Abstract*—The traction inverter represents a crucial component of an electric vehicle (EV) powertrain. Efficiency, power density and overall integration are the primary targets of the inverter design process, which represents an active research and development topic for both industry and academia. The great majority of published EV inverter designs only focus on the DC/AC converter power stage (i.e., power modules and DC-link capacitor), disregarding fundamental elements for the correct operation of the system and/or for its compliance with automotive standards (e.g., control board, current measurement, EMI filter, case integration, etc.). Therefore, this paper focuses on the design and testing of a complete drive inverter system for a high-performance, 800 V 550 kVA, EV traction application. In particular, the inverter design includes state-of-the-art direct cooled SiC power modules, a full-ceramic DC-link capacitor and an EMI filter including an inductor concept providing both differential-mode and common-mode filtering actions.**

***Index Terms*—traction inverter; silicon carbide (SiC); wide bandgap (WBG) devices; electric vehicles (EVs); direct cooling.**

I. Introduction

The traction inverter represents a central component of an electric vehicle (EV) powertrain, being responsible for the DC/AC power conversion between the battery and the electrical machine. As a consequence, this power electronic converter is subject to great pressure for improvement [1], [2] and simultaneously requires high power density (both volumetric and gravimetric), high efficiency over a wide load range (especially at light load), high temperature operation capability, and high switching frequency (i.e., to provide sufficient control margin and reduce time-harmonic losses in low-inductance, high-speed machines with several pole pairs typically adopted in automotive [3]). Furthermore, a shift towards 800 V EV powertrain architectures is currently underway [4], as the increased voltage level allows to reduce the weight and size of on-board power cables, while unlocking faster DC-charging rates. Although several inverter designs for EV traction applications have already been published [5]–[17], they are typically focused on the inverter core (i.e., power modules, gate drivers and cooling system) without considering auxiliary components and/or elements required to achieve automotive compliance (e.g., control board, current measurement, EMI filter, busbars, mechanical case, etc.). Most importantly, efficiency and power density figures tend to lose significance and/or become misleading when critical components such as the EMI filter are not taken into account. Therefore, the aim of this paper is to present a high-performance 800 V inverter design featuring full automotive compliance and thus suitable for direct use on a commercial electric vehicle. This manuscript thus proceeds as follows: Section II shows an overview of the proposed automotive inverter. Next, Section III analyzes the adopted 1200V SiC MOSFET power modules, characterized by an industry-low on-state resistance per unit of footprint and a high-performance direct-cooling technology. Then, Section IV describes the sizing and prototyping of the full-ceramic 900V DC-link capacitor, achieving far superior current and capacitance density values with respect to state-of-the-art film-based solutions. Section V illustrates the design and preliminary experimental validation of the integrated EMI filter using a novel inductor which integrates common and differential mode inductance. Section VI reports a set of experimental results where the designed inverter is tested in back-to-back configuration with a second inverter. Section VII concludes the paper by underscoring the key innovations of the realized traction inverter with respect to state-of-the-art solutions.

II. Drive Inverter System Overview

The drive system specifications and nominal operating conditions are reported in Table I, targeting a high-end commercially

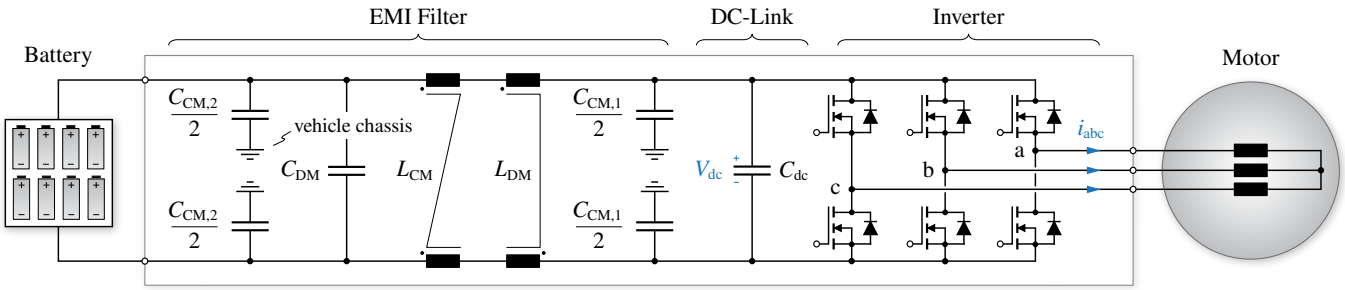


Fig. 1. Equivalent circuit schematic of the considered electric vehicle (EV) powertrain, with highlight of the 800 V 550 kVA drive inverter system.

TABLE I. DRIVE SYSTEM SPECIFICATIONS AND NOMINAL OPERATING CONDITIONS.

Parameter	Description	Value
S	Apparent Power	550 kVA
P	Active Power	400 kW*
I	Peak Phase Current	795 A
V_{dc}	DC-Link Voltage	800 V
f_{sw}	Switching Frequency	20...50 kHz

*limited by the saturation current of L_{DM}.

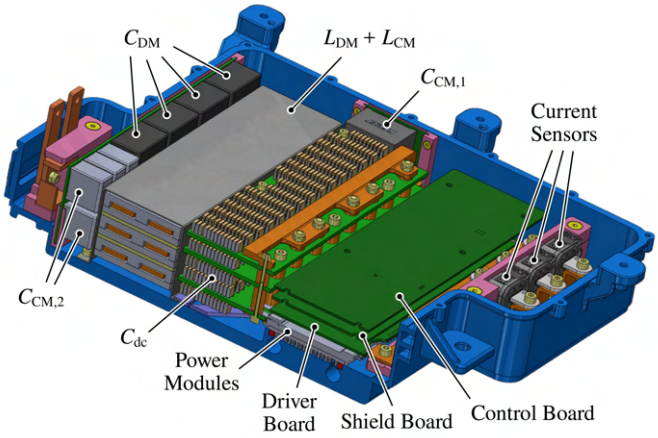


Fig. 2. 3D side view of the designed 800 V 550 kVA three-phase drive inverter system.

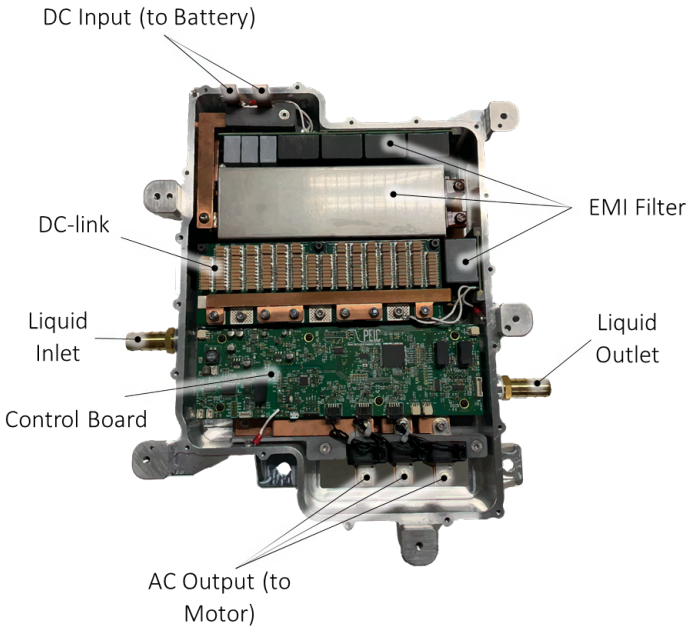


Fig. 3. Top view of the designed 800 V 550 kVA three-phase drive inverter system.

available electric vehicle. In particular, the inverter prototype aims to achieve a relatively high technology readiness level (TRL), namely TRL7. Since the drive system requires full automotive compliance, an integrated differential-mode (DM) and common-mode (CM) EMI filter is included between the DC-link and the battery-side DC connection, as schematically illustrated in Fig. 1.

A 3D side view of the drive inverter prototype is shown in Fig. 2, emphasizing the most relevant components. The complete system is enclosed in a waterproof IP 67 aluminum case (blue color) with a total of 9 anchor points, designed to match the ones of the original inverter currently used on the target vehicle. The drive inverter system embeds all the necessary components to operate autonomously (i.e., sensors, control board) and to comply with automotive standards in terms of connecting interfaces, mechanical roughness, safety requirements, and EMI emissions. As reported in Table I, the maximum inverter output power is 550 kVA/400 kW, where the difference between apparent and active power capability is to be attributed to the saturation current of the EMI filter inductor, limiting the maximum input DC current to 500 A. The total converter volume is 7.7 dm^3, thus translating into a power density figure of $\approx 71\,\mathrm{kVA/dm^3}$ (or $\approx 52\,\mathrm{kW/dm^3}$), considerably higher than currently available state-of-the-art commercial products. An overview of the realized prototype is shown in Fig. 3.

To reduce the overall drive system volume, three main concepts/technologies have been introduced: (1) a direct-cooling system integrated in the inverter case, (2) a full-ceramic DC-link capacitor and (3) an EMI filter featuring a single inductor providing both DM and CM filtering actions. Each one of these elements is briefly presented in the following sections.

III. SiC Power Modules with Direct Cooling

Power semiconductors are the core element of a power converter heavily affecting its performance, efficiency and power density. New wide-bandgap devices such as SiC MOSFETs are gradually replacing Si IGBTs thanks to their lower conduction and switching losses, better temperature stability and better

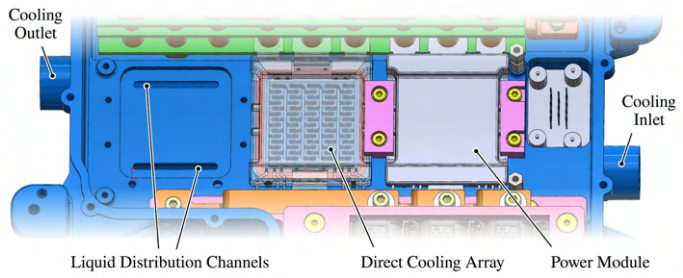


Fig. 4. 3D overview of the direct cooling concept integrated in the inverter case.

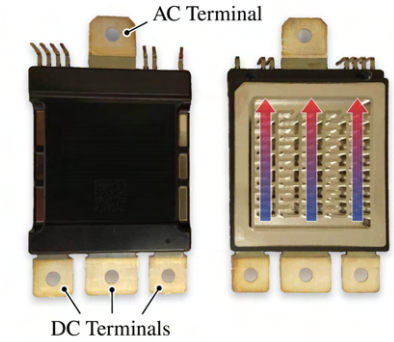


Fig. 5. Top/bottom view of the adopted power modules based on the DCM^{TM}1000 platform from Danfoss.

thermal conductivity. Although all these favourable characteristics have enabled to push power electronic integration as never before, heating extraction is still a major issue. Semiconductors for high-power applications such as traction inverters are usually embedded in a power module, where the dies are connected throughout different material layers to the base plate which has the function of a heat spreader. The power module is then mounted to the heat-sink by means of a thermal interface material (TIM) usually consisting of a high conductive thermal paste. The TIM is in fact normally required as gap filler between mating rigid surfaces, namely the bottom plate of the power module and the top surface of the cold plate. On the other hand, the TIM layer introduces the highest thermal resistance with respect to the other layer in the thermal stack-up [18].

The direct cooling is a promising advancement in the new power module generation. It features a structure where the liquid coolant flows in direct contact with the module base plate. In particular, the power module direct cooling array used for this inverter is highlighted in Fig. 4. The direct cooling allows to eliminate the additional thermal resistance introduced by the TIM leading to a substantial reduction of the overall thermal resistance [19]–[24]. The future trend is to apply this cooling concept also to double-side cooled power modules [25], [26]. The power stage of the proposed drive inverter consists of three 1200 V half bridge SiC MOSFET power modules based on the DCM^{TM}1000 platform produced by Danfoss, whose package is shown in Fig. 5. These power modules are not off the shelf, and they can be customized based on the customer needs (i.e. it is possible to select the dies to use in the power module). The adopted power modules have an industry-low 2.1 mΩ ON-state resistance @ $T_j = 25\,°C$, limited footprint area (i.e., 63x73 mm case), a proprietary direct cooling technology and fast switching capabilities thanks to the SiC MOSFETs combined with a low stray inductance of 6.5 nH. These power modules further enhance the classical direct cooling concept, by using an advanced version of it named ShowerPower® [27]. This technology patented by Danfoss utilizes several meandering cooling channels to guide the coolant along the baseplate. This solution improves the thermal performances by creating swirl effect in the cooling channels. This means that the coolant is constantly brought into contact with the surface that requires cooling. This feature enables to almost double the heat transfer coefficient, thus reflecting in a much higher current capability. In addition, as shown in Fig. 4, the heat sink (i.e., the liquid distribution system) has been directly integrated within the inverter case, allowing a further reduction in volume and weight.

IV. Full-Ceramic DC-Link

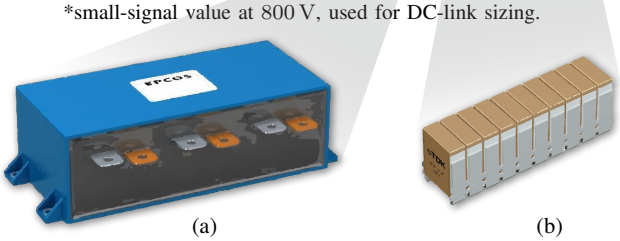
The DC-link often defines the volume and the weight of a power converter. As consequence, it is one of the main targets of optimization in order to improve the overall converter power density. New technologies must be exploited to further reduce the DC-link volume. In literature, there are plenty of papers focusing on the sizing and the designing of a DC-link for a three phase inverter [28]–[30]. However, only a limited number of works focus on non-standard solutions such as ceramic capacitors [31]–[33].

Film capacitors are an established technology for the automotive industry, due to their high thermal stability (operative ranges are in the order of 100-125 °C), low cost and self-healing capabilities which allow them to guarantee high levels of reliability required by the automotive industry. On the other hand, due to their large physical size, they are characterized

TABLE II. Specification of the considered benchmark capacitors.

	Film	**Ceramic**
Manufacturer	EPCOS(TDK)	TDK
Part Number	B25655P9127K151	CeraLink® FA10
Rated Voltage	900 V	900 V
Rated Capacitance	120 µF	2.5 µF (1.3 µF*)
Rated RMS Current	120 A	32 A
Maximum Temperature	105 °C	150 °C
Volume	554.4 cm^3	2.0 cm^3
Weight	800 g	11.5 g

*small-signal value at 800 V, used for DC-link sizing.



(a) (b)

Fig. 6. Highlight of the considered 800 V benchmark capacitors (not to scale): (a) EPCOS B25655P9127K151 [35], (b) TDK CeraLink® FA10 [36].

by a relatively high series inductance, reflected in a low self-resonance frequency. This limits the frequency operating range of the capacitor itself. Furthermore, they exhibit a relatively high series resistance that increases at high frequency (above 100 kHz) due to the AC skin effect. This leads to low RMS current capability that becomes the limiting factor for the sizing of the capacitors. Film capacitors do not fully exploit the benefits of the higher switching frequency made possible by the use of wide bandgap devices. In fact, when the switching frequency is increased, a lower capacitance value is required to meet the same voltage ripple constraints. However, in case of film capacitors their minimum size is limited by their RMS current capabilities. To shrink the DC-link size, the proposed inverter employs high-voltage lead–lanthanum–zirconate–titanate (PLZT) ceramic capacitor technology (e.g., CeraLink® from TDK [34]) that promises far superior performances with respect to state-of-the art film-based solutions. The main benefits of such technology are: (1) higher specific capacitance, (2) higher RMS current capability, (3) higher maximum temperature operation, (4) lower equivalent series inductance (due to the smaller package), and (5) decreasing resistance with frequency (i.e., effectively benefiting from higher frequency operation). With the aim of providing a quantitative analysis between these two different capacitor technologies, the main features of two commercially available high-voltage DC-link capacitors are compared in Table II and Fig. 6. Due to the very different size of the two selected capacitors, the capacitance and RMS current values are expressed in relative terms thus providing useful specific performance indicators, which are summarized in Fig. 7. From the performance comparison, clearly results that PLZT ceramic presents a higher volumetric and gravimetric current density, so the RMS current of the capacitor is no more the limiting factor of a ceramic DC-link design. In a proper design, the

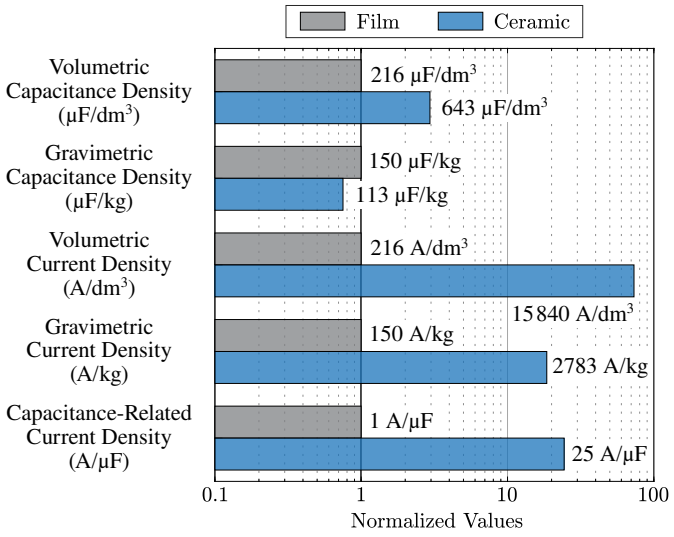


Fig. 7. Specific performance comparison between the selected benchmark film and PLZT ceramic capacitors (small signal capacitance). The specific performance indicators are normalized with respect to the film capacitor value and are shown in logarithmic scale.

DC-link capacitors must fulfill two requirements: they must withstand the RMS current stress for the required application and they must have enough capacitance to ensure a maximum voltage ripple superimposed to the voltage DC-link [29]. For the PLZT ceramic capacitor the small-signal capacitance must be considered. This is the most precautionary value for the case where a small voltage ripple is superimposed to a large DC bias voltage (i.e. DC-link of a two level three phase inverter) [34]. The RMS current stress generates losses that must be carefully handled to avoid achieving the capacitor maximum temperature. Knowing the peak phase current I, the inverter modulation index M and the load power factor angle φ, the RMS current ripple flowing in the DC-link capacitor can be analytically expressed by the following formula [37]:

$$I_{\mathrm{C_{dc},RMS}} = I\sqrt{M\left[\frac{\sqrt{3}}{4\pi}+\cos^2\varphi\left(\frac{\sqrt{3}}{\pi}-\frac{9}{16}M\right)\right]} \qquad (1)$$

According to (1) the worst case value for the RMS current is found for $\varphi = 0$ and $M = 0.61$.

The second limit is on the DC-link voltage ripple so as not to overcome the maximum voltage rating of the semiconductors and not to move away from ideal operation conditions. Usually, the DC-link capacitor peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{dc},pp}}$ is defined first, as it is directly proportional to the DC-link peak-to-peak voltage ripple $\Delta V_{\mathrm{C_{dc},pp}}$. Due to the dependencies from the modulation strategies, M and φ, it is not possible to extract a general analytical formula for $\Delta Q_{\mathrm{C_{dc},pp}}$. In case of space vector modulation strategy (SVPWM), the maximum peak-to-peak charge ripple is obtained for $M = 2/\sqrt{3}$ and $\varphi = \pm\pi/2$ [38]:

$$\Delta Q_{\mathrm{C_{dc},pp,max}} = \frac{1}{4}\frac{I}{f_{\mathrm{sw}}} = C_{\mathrm{dc}}\,\Delta V_{\mathrm{dc,pp,max}} \qquad (2)$$

To sum up, the DC-link capacitor sizing depends on the most strict requirement specified by

$$C_{\mathrm{dc}} = \max\left[C_{\mathrm{dc,I_{RMS}}}, C_{\mathrm{dc},\Delta \mathrm{V_{pp}}}\right] \qquad (3)$$

For film capacitor the sizing depends mostly on the RMS current stress. On the contrary the limitation factor for ceramic capacitor is the capacitance amount to limit the voltage ripple on the DC-link. Since this requirements change with the converter switching frequency [33], the ceramic capacitor technology is effectively able to benefit from the WBG semiconductor features.

Fig. 8 shows the DC-link sizing using ceramic and film technology for the proposed inverter. The inverter specifications are listed in Table I, while the maximum peak-to-peak voltage ripple is set to 10%. It is clear that the ceramic technology brings a substantial power density increase, by reducing both the volume and the weight of the DC-link compared to a state-of-the-art film solution. It must be pointed out that since the ceramic capacitors are discrete components, their assembly will reduce the volumetric and gravimetric advantages compared to film technology, which are usually found in ready-to-use packages. To sum up, Fig. 8 shows the maximum advantages achievable by using ceramic capacitors.

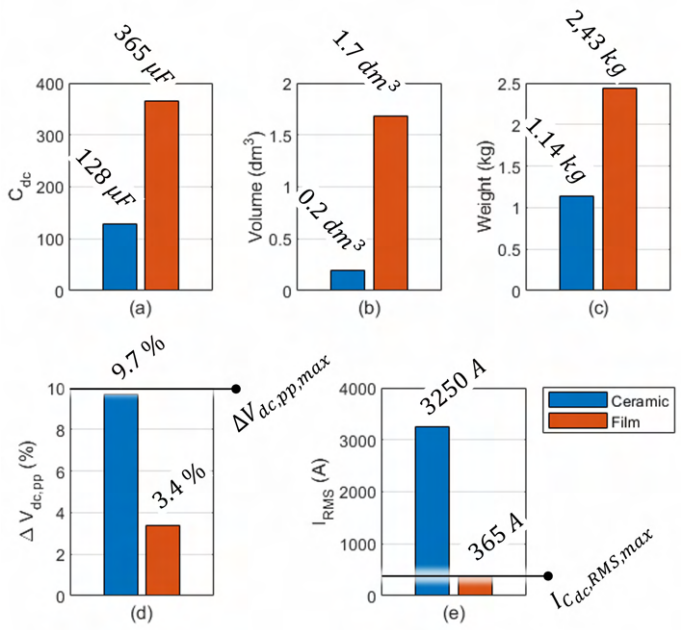


Fig. 8. Film vs. ceramic DC-link capacitor (small signal capacitance) sizing according to the procedure outlined in [33], assuming $\Delta V_{\mathrm{dc,pp,max}} = 10\%$, $T_{\mathrm{a}} = 85°C$ and the inverter specifications reported in Table I. (a) DC-link capacitance C_{dc}, (b) volume, (c) weight, (d) normalized peak-to-peak voltage ripple $\Delta V_{\mathrm{dc,pp}}$ and (e) RMS current capability $I_{\mathrm{C_{dc},RMS}}$.

A detailed 3D model of the prototyped ceramic DC-link is shown in Fig. 9. It consists of three identical double-side 800 µm thick copper PCBs, housing several 900 V CeraLink® capacitors, thus reaching a total small signal capacitance of 128 µF. In particular, the three boards house in total: 80 FA10 B58035U9255M001 (1.3 µF each), 60 FA3 B58035U9754M062 (0.39 µF each) and 6 B58031U9254M062 LP (0.13 µF each) that are placed only on the bottom board in correspondence of

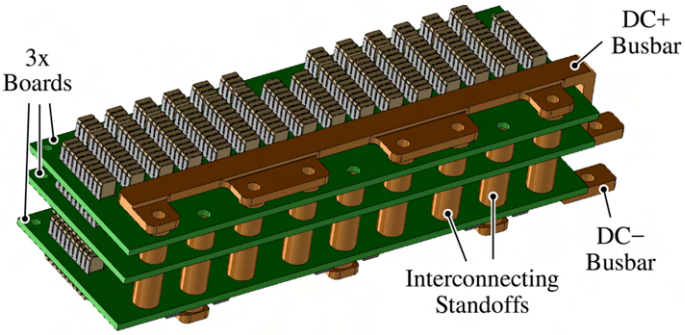


Fig. 9. 3D overview of the full-ceramic DC-link concept.

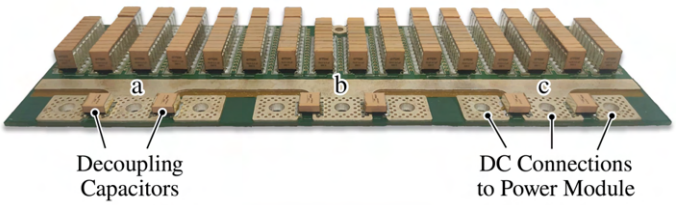


Fig. 10. Bottom view of the DC-link board directly connected to the power modules.

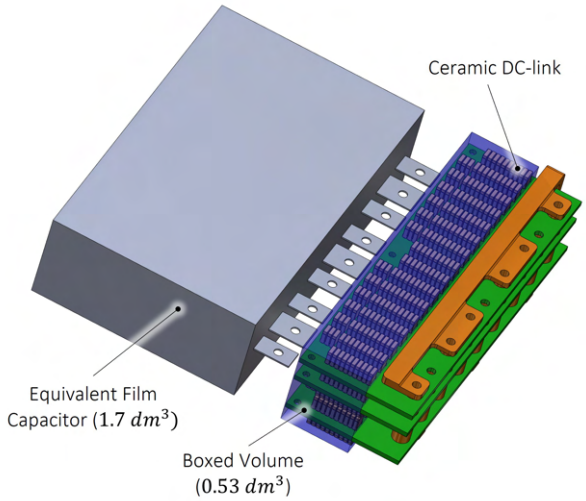


Fig. 11. 3D overview of the proposed 900 V full-ceramic DC-link capacitor and comparison with the equivalent film-based solution.

the DC terminals of the power modules as shown in Fig. 10, thus minimizing the commutation loop inductance. It should be noted that on the two lower boards the capacitors were mounted on both sides, while on the third board the capacitors were mounted only on the top side (sufficient to reach the target capacitance). The designed DC-link targets a maximum peak-to-peak voltage ripple $\Delta V_{\mathrm{pp}} = 80\,\mathrm{V}$ at the minimum switching frequency (i.e., $f_{\mathrm{sw}} = 20\,\mathrm{kHz}$) and maximum output current (i.e., $I = 795\,\mathrm{A}$).

Fig. 11 shows the rendering 3D of the proposed DC-link ceramic solution concept compared to the target film-based equivalent DC-link. The boxed volume of the proposed ceramic DC-link is equal to 0.53 L, which is more than double the theoretical solution. Indeed, the compared volume encloses the CeraLink® capacitors and the thick-copper PCB. A more advanced manufacturing process could realistically improve the space exploitation. Nevertheless, the proposed solution enables a ≈ 3 times volume reduction compared to the state of the art film solution.

V. EMI Filter

The EMI filter is a critical component in EV drive inverter systems, having a major impact on the converter volume, weight and losses. The role of the EMI filter is to ensure that only limited electromagnetic noise is conducted outside of the inverter case, in order to ensure the correct operation of neighbouring systems. The common and differential noise emissions at the DC input of the inverter must be limited to meet the automotive standards. In this case, the filter is designed to comply with the CISPR 25 class 3 emission standard.

The expected Common Mode (CM) and Differential Mode (DM) noise can be separately computed via numerical analysis using the equivalent circuits shown in Fig. 12. While the common mode noise is affected only by the output duty cycle, the differential mode noise depends also on the output current. All the expected converter operating conditions must be examined and the worst-case scenario (i.e. maximum noise

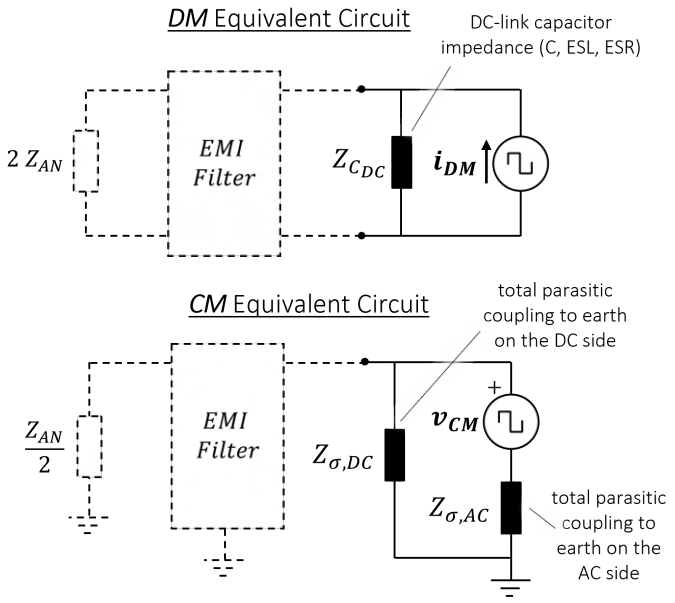


Fig. 12. Equivalent circuital models used for the numerical computation of the common and differential mode noise emissions.

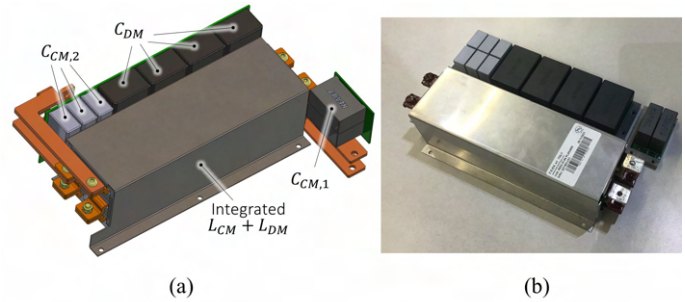


Fig. 13. (a) 3D overview of the EMI filter concept and (b) top view of the integrated DM/CM inductor and the filter capacitor boards.

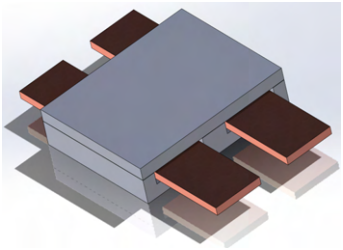


Fig. 14. EI shape magnetic core and DC-link busbars.

emission) must be taken into account for the filter sizing. The computed noise is then reported in the frequency domain by means of a Fast Fourier Transformation (FFT) and compared with the limits imposed by the CISPR standard, thus enabling to compute the EMI filter attenuation requirements. A detailed explanation of the adopted approach can be found in [39]. In this case, a single stage CLC filter is sufficient to meet the CISPR requirements while minimizing the overall volume. The full schematic of the converter including the EMI filter stage is reported in Fig. 1, while the filter parameters are reported in Table III. The filter is placed between the DC-link capacitor and the battery-side DC connector terminals as shown in Fig. 3, thus ensuring that the noise propagated to the battery (i.e., differential-mode) and the vehicle chassis (i.e., common-mode) is properly limited.

The filter components are shown in Fig. 13 b), while their connection layout is shown in Fig. 13 a). $C_{\mathrm{CM},1}$, $C_{\mathrm{CM},2}$ and C_{CDM} consist of multiple off-the-shelf film capacitors connected in parallel on a standard PCB. As $C_{\mathrm{CM},1}$ and $C_{\mathrm{CM},2}$ are connected to the inverter aluminum case, type Y capacitors are used to meet the automotive safety standards. L_{DM} and L_{CM} consist of a single custom designed inductor integrating both the DM and CM filtering functions, thus reducing the overall system components count and substantially improving the filter power density. The custom inductor consists of 12 EI shaped ferrite cores (material 3C92 from Ferroxcube) crossed by the two dc-link busbars (DC+ and DC-) as shown in Fig. 14. Fig. 15 and Fig. 16 show the magnetic flux path when the two busbars are crossed respectively by common and differential mode current.

It is observed that the common mode flux path exploits the external edges of the core, while the differential mode flux path exploits the central core column. Since the common mode current is in the order of a few ampere, the common mode flux path can be designed to achieve a low reluctance value, thus maximizing the common mode inductance value (i.e. no air gap is added to the common mode magnetic path). On the other hand, the differential mode current that is responsible for the power transfer can rise up to $500\,\mathrm{A}$. To avoid the magnetic core saturation, a sufficiently high reluctance must be designed within the differential mode flux path, thus leading to a relatively low differential mode inductance value (i.e. a $1.6\,\mathrm{mm}$ gap is added to the center column of the ferrite core). As shown in

TABLE III. EMI FILTER PARAMETERS.

Parameter	Design Value	Measured Value
L_{CM}	$75.6\,\mu\mathrm{H}$	$65.85\,\mu\mathrm{H}$
L_{DM}*	$4.98\,\mu\mathrm{H}$	$6.6\,\mu\mathrm{H}$
C_{DM}	$40\,\mu\mathrm{F}$	$40\,\mu\mathrm{F}$
$C_{\mathrm{CM},1}$	$1.98\,\mu\mathrm{F}$	$1.98\,\mu\mathrm{F}$
$C_{\mathrm{CM},2}$	$1.36\,\mu\mathrm{F}$	$1.36\,\mu\mathrm{F}$

* $I_{\mathrm{SAT}} = 500A$.

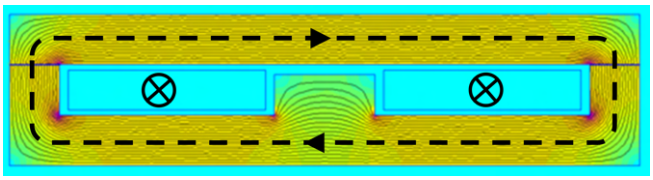


Fig. 15. Common mode magnetic path.

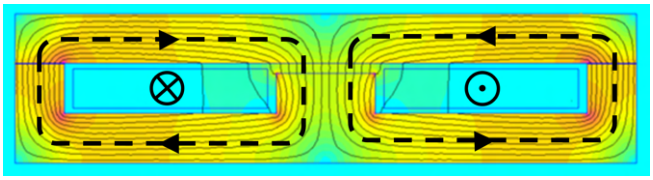


Fig. 16. Differential mode magnetic path.

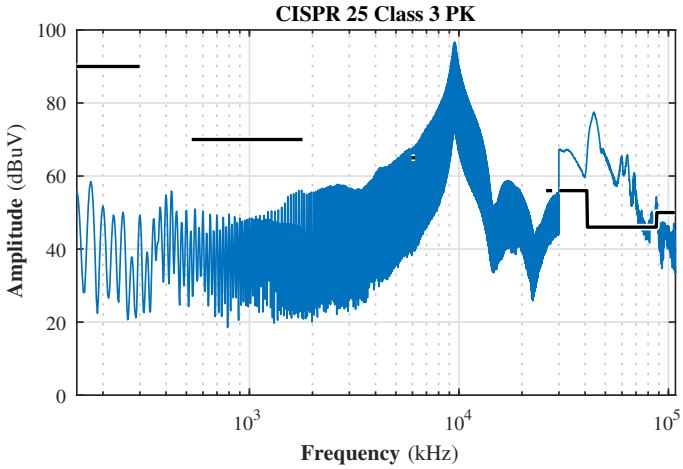


Fig. 17. Experimenal noise emission evaluation. Testing conditions: no load, $V_{\mathrm{dc}} = 800\,\mathrm{V}$, $f_{\mathrm{sw}} = 20\,\mathrm{kHz}$, $M = 0$.

Table III, the measured values of L_{DM} and L_{CM} slightly differ from the design values due to manufacturing tolerances.

The CISPR 25 standard requires evaluating the EMI emission with the inverter connected to the target motor and supplied via a LISNR network at the nominal voltage. As the target motor or a motor with a similar rated current were not available, the inverter has been tested at no load. In this case, all the generated noise is due to the common mode, as no load current is flowing. Fig. 17 shows the measured conducted EMI emissions (blue trace) and the peak limit values according to the CISPR 25 class 3 standard (black trace). The filter is operating correctly keeping the noise emission below the limits up to a frequency of a few MHz. However around 10 MHz there is a peak in the noise emission due to a resonance of the filter caused by its parasitics elements (e.g. the connection between the common mode capacitors and the busbars consists of a few centimeters of copper wire). Multiple countermeasures can be used to mitigate the problem. Reducing filter parasitics (e.g. by shortening component connections) can help to increase the resonance frequency. Alternatively, a second filter stage specifically targeting the high frequencies can be added. Another solution would be to employ a magnetic core with higher losses helping the damping of the system.

VI. Experimental Tests

The proposed inverter has been tested in back-to-back configuration according to the functional schematic shown in Fig.18. The converter under test is connected in opposition by means of three inductors to a second converter named the "loading inverter". The loading inverter is current-controlled, thus imposing the phase currents of the converter under test. At the same time, the converter under test is voltage-controlled, thus enabling to work at different modulation indexes and different power factors.This setup enables to test the inverter on the whole operating range without the need for the target motor (i.e. the motor that will be matched with the inverter on the final vehicle). Furthermore, the power is recirculated between the two inverters allowing to supply only the losses of the system.

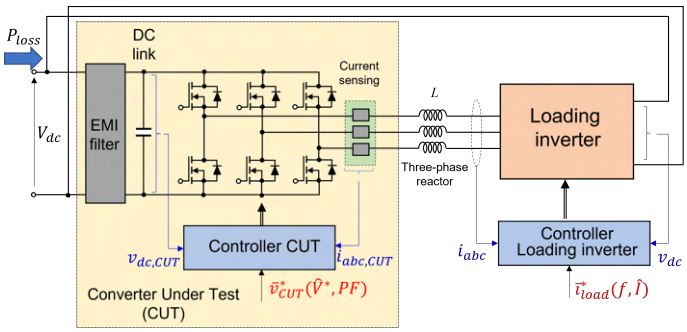


Fig. 18. Functional schematic of the back-to-back test rig.

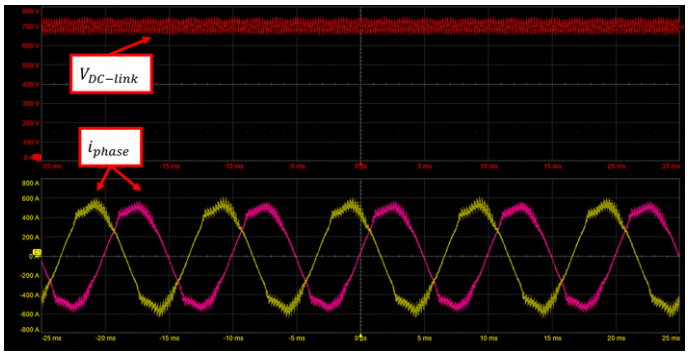


Fig. 19. Experimental waveforms from the back-to-back test. **Test conditions:** $f_{\mathrm{sw}} = 20\,\mathrm{kHz}$,$V_{\mathrm{dc}} = 700\,\mathrm{V}$, $I = 600\,\mathrm{A}$, $f = 100\,\mathrm{Hz}$, $M = 0.6$, $\cos(\varphi) = 0.9$. **Top:** DC-link voltage measured at the power modules DC terminals. **Bottom:** phase a and phase b currents.

This feature is particularly advantageous considering the rated power of the converter under test.

Experimental results from the back-to-back test are shown in Fig. 19. The load converter is imposing a 100 Hz, 600 Apk sinusoidal current, while the converter under test is operating with a modulation index and a power factor respectively of 0.6 and 0.9. The red trace on the top plot shows the voltage measured at the DC input of one of the power modules while the yellow and purple traces are the currents of phases 'a' and 'b'. When the phase current approaches 600 A the coupling inductors tend to saturate causing the current distortion visible in the figure. During the back-to-back test, the temperatures of the main components (i.e. power modules, ceramic capacitors and busbars) were continuously monitored and no issues were spotted. New inductors and a new load converter will be used in the future, thus enabling the test of the inverter up to the maximum current. The back-to-back configuration is not suitable for EMI evaluation, as the common and differential mode impedances are not representative of a real working condition.

VII. Conclusion

This paper provides an overview of a high-performance full-SiC 800 V 550 kVA drive inverter design for EV applications, achieving a power density figure of $\approx 71\,\mathrm{kVA/dm^3}$. With respect to the existing literature, this work takes into account typically disregarded drive system components, such as the control board, the current sensors, the EMI filter, the cooling system and the

case integration. In particular, to achieve such performance, the proposed inverter design includes state-of-the-art direct cooled power modules, a full-ceramic DC-link capacitor and an integrated EMI filter inductor concept providing both differential-mode and common-mode filtering actions. The proposed inverter has been preliminarily validated via a set of experimental tests allowing to emulate different operative conditions (i.e. current load, modulation index, power factor and so on). No design issues were found, excepting for the self-resonance of the EMI filter around 10 MHz, however as previously stated, multiple countermeasures can be adopted to mitigate the problem. Future work will include an efficiency map of the converter and a full EMI test with the inverter connected to the target motor. Additional studies will target the integrated inductor, where the benefits in terms of volume and weight will be evaluated in a more rigorous and quantitative way.

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