

ALICE Zero Degree Calorimeters. The new readout system in LHC Run 3

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## 5 **ALICE Zero Degree Calorimeters** 6 **The new readout system in LHC Run 3**

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15 **ABSTRACT:** The Zero Degree Calorimeters (ZDC) were designed to provide the measurement of the  
16 event geometry and luminosity in heavy-ion operation. The readout system was redesigned in order  
17 to operate in continuous mode without dead time at 2.5 MHz event rate. The new acquisition chain  
18 is based on a commercial 12 bit digitizer with a sampling rate of about 1 GSps, assembled on an  
19 FPGA Mezzanine Card. The signals produced by the 26 ZDC channels are digitized, and samples  
20 are processed through an FPGA to extract information such as timing, baseline average estimation  
21 and luminosity.

22 **KEYWORDS:** Detector control systems (detector and experiment monitoring and slow-control sys-  
23 tems, architecture, hardware, algorithms, databases); Front-end electronics for detector readout

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32 **1 Introduction**

33 The ZDC of the ALICE experiment consists of two identical sets of calorimeters located on both  
34 sides of the interaction point IP2 (side A and C), 112.5 m away from it [1, 2]. In that region the two  
35 LHC beams circulate in two different pipes. Each set of detectors consists of a neutron (ZN) and a  
36 proton (ZP) calorimeter. The ZN is placed at zero degree with respect to the LHC axis, between the  
37 two beam pipes, while the ZP is positioned externally to the outgoing beam pipe. Collisions may  
38 occur in fixed time slots named bunch crossings (BC) that are separated by  $\sim 25$  ns. ZDC is mainly  
39 sensitive to spectator nucleons. The spectator protons are separated from the ion beams by means  
40 of a dipole magnet, while spectator neutrons fly at zero degrees without further changing direction.  
41 The ZDC detector is completed by 2 forward EM calorimeters (ZEM) placed at about 7.35 m from  
42 IP2, on side A. The ZDCs are quartz-fiber spaghetti calorimeters with silica optical fibers as active  
43 material embedded in a dense absorber. The main purpose of these calorimeters is to provide an  
44 independent measurement of the time of the collision, of the vertex position, centrality, event plane  
45 and to measure the luminosity in heavy-ion collisions [3–6]

46 **2 The ZDC readout system and challenges**

47 In order to exploit the potential offered by the LHC increased luminosity in Run 3, the ALICE ex-  
48 periment upgraded its trigger and readout system, to be able to acquire all collisions in self-triggered  
49 mode without dead time[7–9]. The purpose of the ZDC readout upgrade was to enable the detector  
50 to cope with the increased event rate while preserving its time and charge resolution performance.  
51 The operating conditions for the ZDC are extremely challenging, in particular concerning Pb-Pb  
52 collisions, due to the presence of electromagnetic dissociation processes (EMD) [10, 11]. When  
53 running in self-triggered mode the ZDC system will need to sustain a readout rate of  $\sim 2.5$  MHz for

54 the channels of the most exposed calorimeters that compares to the foreseen hadronic rate of 50 kHz  
55 sustained by the other detectors. The previous electronics, based on Charge-to-digital converters  
56 (QDCs), with a fixed dead time of  $\sim 10 \mu\text{s}$ , and on readout through VME bus, could not cope with  
57 such a high rate [12]. Moreover a crucial aspect of the ZDC operation in Run 3 is acquiring the  
58 events with a reduced bunch spacing of 50 ns (lower than the length of the signal of  $\sim 60$  ns) in the  
59 presence of a large signal dynamics (from a single neutron to  $\sim 60$  neutrons).

### 60 **3 The readout architecture**

61 Given the low number of channels of the detector (26), the new readout is based on commercial  
62 FPGA Mezzanine Card (FMC) digitizers that allow a continuous sampling of the signal waveform  
63 followed by a real time analysis on a FPGA. The chosen digitizer is the ADC3112 from IOXOS,  
64 each mounting two TI ADS5409 ADC. Every FMC module has 4 channels, a maximum sampling  
65 rate of 1 GSps, 12 bit resolution (with an ENOB of 10 bit) and can be configured with  $50 \Omega$   
66 termination [6]. The ADC is configured applying a low pass filter and subsequent 2x decimation  
67 filter, with the purpose to reduce the total noise and the sampling rate down to 480 MSps. Thanks  
68 to the adequate bandwidth available through the FMC connection from the digitizer to the FPGA  
69 the full waveform can be analyzed, thus the time and charge resolution of the previous system can  
70 be preserved while still allowing the required acquisition rate for Run 3. Each digitizer is mounted  
71 on a commercial IFC1211 VME carrier from IOXOS. The VME format was chosen in order to  
72 exploit the existing infrastructure. The readout, however, will not be carried out via VME, but on  
73 CERN developed 4.8 Gbps bi-directional optical links (GBT)[13] implemented through commercial  
74 TAS-A2NH1-P11, multimode, 850 nm, SFP+ transceivers. Each carrier contains a Xilinx FPGA  
75 Kintex Ultrascale xcku040-1ffva1156 and a PowerPC processor. A fast trigger logic is executed  
76 on the FPGA and the interesting portions of the waveform are transferred to the acquisition and  
77 reconstruction system through the GBT links. Each readout module uses two GBT links, namely  
78 Link 0 and Link 1. Link 0 is used for channel 0 and 1 data transmission and for receiving the orbit  
79 number information, trigger messages from the Central Trigger Processor (CTP)[14], start/stop  
80 commands and synchronization signals, while Link 1 is used for channel 2 and 3 data transmission  
81 and for receiving configuration commands from the Detector Control System (DCS). Each channel  
82 can be selectively enabled or disabled for readout by means of a configurable 4 bit readout mask.  
83 A scheme of a readout module is shown in figure 1. The complete detector readout system uses  
84 a total of 8 modules, thus having a maximum of 32 usable channels. Digitized data are aligned  
85 with the appropriate BC by means of two delay parameters for each channel and, if the auto-trigger  
86 algorithm is satisfied, data from the corresponding BC is flagged for acquisition[15].

### 87 **4 The trigger algorithm**

88 A trigger algorithm has been developed and tested with digitized data [15]. The algorithm involves  
89 differences between samples that are compared to a threshold  $t$ . Indicating with  $y_i$  the  $i^{th}$  ADC  
90 sample and considering that the signal has negative polarity, the trigger can be evaluated with a  
91 double (eq 4.1) or triple (eq 4.2) condition, the first one being more sensible to pile-ups, while the

92 second one offering better protection from the electronic noise.

$$T = (y_i - y_{i+k} > t) \wedge (y_{i+1} - y_{i+k+1} > t) \quad (4.1)$$

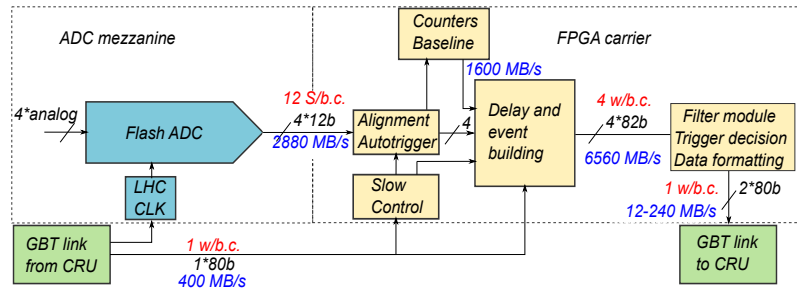
93

$$T = (y_i - y_{i+k} > t) \wedge (y_{i+1} - y_{i+k+1} > t) \wedge (y_{i+2} - y_{i+k+2} > t) \quad (4.2)$$

94 The choice between double and triple condition is configurable and can be changed on the fly before  
 95 the data taking without firmware modifications. Typical values for the algorithm parameters are  
 96  $k = 4$  and  $t = 10$ . The trigger algorithm runs on every channel and sets the auto-trigger flags  
 97 independently for each channel. The logic reads the auto-trigger flags of the different channels of  
 98 each module and puts them in logic AND with a configurable trigger mask. If the result is not zero  
 99 this provides the global trigger decision for the module.

## 100 5 Firmware architecture

101 The main firmware blocks are summarized in figure 1. The logic is working at  $\sim 240$  MHz, thus  
 six clock cycles are available to process the information produced in a bunch crossing. The Link 0



**Figure 1.** The rate of information for each link is shown in red text, in black the number of lanes multiplied by the bus width and in blue the data bandwidth[15].

102

103 upstream payload coming from the Common Readout Unit (CRU)[16], conveying trigger messages,  
 104 is 80 bit for each bunch crossing and is fanned-out to the processing pipelines of each channel. The  
 105 Link 1 upstream payload is reserved for 80 bit Single Word Transfer (SWT) messages which are used  
 106 for slow control board management, in particular for writing or reading configuration parameters,  
 107 for sending reset commands, for triggering the auto-calibration of the delays, for reading the status  
 108 of the two links or the FIFOs memories and for enabling or disabling a "special run" data acquisition  
 109 mode, where a larger portion of the waveform is transferred. Each word passes through a handler  
 110 which is connected to the main event building module. The digitized data, after decimation, result in  
 111 12 words of 12 bit per channel and per bunch crossing. Firstly, the signals are aligned in the center of  
 112 the bunch crossing with a resolution of 1 sample by means of a shift register of configurable length.  
 113 This procedure is done automatically by the firmware logic at every new fill of LHC and it works  
 114 by calculating the average sample at which an auto-trigger fires and the subsequent compensation  
 115 delay value. After synchronization, a configurable number of trigger differences from eq 4.1 or eq  
 116 4.2 (between 0 and 12) are evaluated in a window of 12+2 samples related to the current crossing  
 117 and the beginning of the next one. If the selected trigger condition is satisfied, then the bunch is  
 118 flagged for acquisition. Information from an internal orbit counter, bunch crossing counter, and

119 number of hits along the orbit are also inserted in the data stream for every channel. Collisions at  
120 the IP can occur only in well-defined bunch crossings, depending on the active LHC filling scheme.  
121 This feature is exploited to identify the bunch crossings that are free from any signal and can be  
122 used to evaluate the average baseline for each orbit. The first stage of the event building combines  
123 the different pieces of information into four words 82 bit long for each channel by means of a ring  
124 buffer delay that synchronizes the output of the digitizer with the ALICE trigger information and  
125 with locally computed quantities. The full information of each bunch crossing is then passed to  
126 the second stage of event building using a FIFO. The final filter module verifies the presence of  
127 auto-trigger or ALICE trigger flags, checks if there are interactions in the three preceding bunch  
128 crossings (pile-up) and verifies the presence of the "special run" condition. At this point the data  
129 can be formatted and transmitted to the CRU. If the filter module does not detect any trigger flag  
130 then the event is discarded from the FIFO. In auto-trigger mode, each active channel produces a  
131 payload of six 80 bit long words, out of which three are for the signal and the other three are the  
132 samples of the previous bunch crossing (with respect to the triggered bunch crossing), that are used  
133 to perform a more accurate baseline subtraction during reconstruction and to detect the presence  
134 of pile-up. The payload bandwidth ranges from  $\sim 12$  MBps for the modules with lower occupancy  
135 (connected to the detectors sensitive mainly to hadronic collisions) to about  $\sim 240$  MBps for the  
136 four modules dedicated to the readout of the neutron calorimeters.

## 137 **6 Detector segmentation and cabling**

138 The auto-trigger strategy takes advantage of the segmentation of the detectors. The light produced  
139 by the hadronic showers is collected in such a way that half of the signal is readout by a common  
140 photomultiplier (TC) and the other half by fibers that are bundled to divide the detector into four  
141 towers [15, 17] readout by four different photomultipliers (T1, T2, T3, T4). In normal operation  
142 the auto-trigger of each neutron calorimeter is based on the TC signals since it has the best energy  
143 resolution. These signals are therefore fanned-out to two modules but readout only once. The analog  
144 signals of the four towers are summed (SUM) to provide an alternative auto-trigger in case of failure  
145 of the common photomultiplier and therefore are fanned-out to two modules too. The remaining  
146 four free channels are dedicated to the readout of the four towers. For the proton calorimeters the  
147 redundancy requirement is less stringent. A cabling scheme is shown in table 1. In order to exploit  
148 the full input dynamics of the digitizer, the input signals are shifted by  $\sim 450$  mV.

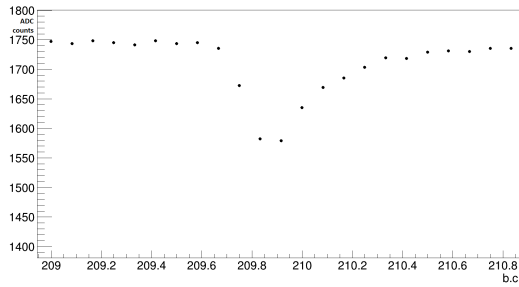
## 149 **7 Performance and conclusions**

150 The readout chain and the auto-trigger algorithm were tested using a pulse generator in laboratory  
151 during development and using a laser to stimulate the photomultipliers during the testing at the  
152 ALICE site. Tests on the maximum trigger rate throughput were performed with different configu-  
153 rations of readout mask and auto-trigger mask. This resulted in a maximum trigger frequency of  $\sim$   
154 5.5 MHz in the best case scenario and  $\sim 2.1$  MHz for the worst case scenario. In September 2022  
155 a first commissioning phase with LHC p-p collisions at 13.6 TeV was performed. This allowed to  
156 assess the performance of the readout in real world conditions, in particular regarding the auto-trigger  
157 algorithm and the GBT based data transmission. Regarding the link stability, it was observed that

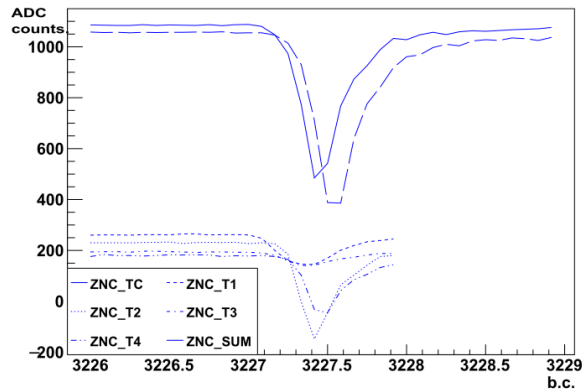
	MODULE 0	MODULE 1	MODULE 2	MODULE 3
ch 0	ZNA_TC(T)	ZNA_TC (OT)	ZNC_TC(T)	ZNC_TC(OT)
ch 1	ZNA_SUM(S)	ZNA_SUM	ZNC_SUM(S)	ZNC_SUM
ch 2	ZNA_T1	ZNA_T3	ZNC_T1	ZNC_T3
ch 3	ZNA_T2	ZNA_T4	ZNC_T2	ZNC_T4
	MODULE 4	MODULE 5	MODULE 6	MODULE 7
ch 0	ZPA_TC(T)	ZPA_TC (OT)	ZPC_TC(T)	ZPC_TC(OT)
ch 1	ZEM1(T)	ZPA_SUM	ZEM2(T)	ZPC_SUM
ch 2	ZPA_T1	ZPA_T3	ZPC_T3	ZPC_T1
ch 3	ZPA_T2	ZPA_T4	ZPC_T4	ZPC_T2

**Table 1.** [15] Cabling of each IFC1211 module of the upgraded ZDC readout system. T = (Trigger) triggering channel. OT = (Only Trigger) channel used for trigger, but not for readout. S = (Spare) Channel not used for trigger nor for readout.

158 during the full data taking the links never lost connection and regarding the data throughput it was  
159 in line with what was calculated for a 50 KHz hadronic interaction rate at  $\sim 160$  MBps for the full  
160 readout. Several tests were performed with different thresholds and readout configurations in order  
161 to evaluate the optimal working conditions for p-p and Pb-Pb interactions. Figure 2 shows a single  
162 waveform acquired by stimulating a photomultiplier by means of a laser, while waveforms from a  
single p-p interaction, observed by the ZN side C (ZNC), are reported in figure 3.



**Figure 2.** Signal waveform of ZNC\_TC stimulated by a laser.



**Figure 3.** Signal waveforms from ZNC calorimeter during p-p interaction.

163  
164 In conclusion, from preliminary tests in the laboratory and with beam, it seems that the FMC  
165 digitizer with FPGA data processing is working as expected. Further commissioning is scheduled  
166 for November 2022 with p-p and Pb-Pb interactions.

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