A 64-channel waveform sampling ASIC for SiPM in space-born applications

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A 64-channel waveform sampling ASIC for SiPM in space-born applications

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Abstract: The architecture of a 64-channel ASIC for the readout of Silicon Photomultipliers in space experiments is described. Each channel embeds a front-end amplifier with a common gate topology followed by a 256 cells analogue memory with a sampling frequency of 200 MHz. A single memory cell includes a storage capacitor, a single-slope Analog-to-Digital Converter (ADC) with programmable resolution between 8 and 12 bits and the digital control logic. To save power, the A/D conversion is carried-out only when a trigger signal is received. The trigger can either be generated inside the ASIC or provided by an external source.The analogue samples are digitized in parallel, thus reducing the conversion dead time. The memory cells can be arranged in a single array or they can be grouped in shorter slots of 32 or 64 cells that work in a multi-buffer configuration. The channels can work independently or they can be synchronised to acquire the same time-frame in the full chip. The target power consumption is 5 mW/channel. The ASIC is being designed in a 65-nm CMOS technology. A digital-on-top flow is applied for the integration and final validation of the chip. The tape-out is scheduled in the first quarter of 2023.

Keywords: VLSI circuits, Front-end electronics for detector readout

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Contents

1 Introduction

Silicon Photomultipliers (SiPMs) are today employed in many different fields such as High Energy Physics (HEP) instrumentation [1], LIDAR [2] and Positron Emission Tomography (PET)[3]. Due to their good detection efficiency, compactness and capability to work with moderate power supply voltages they are becoming even more attractive also for space-born applications. SiPM are considered, for instance, to equip on board cameras of future satellite-based cosmic ray observatories. In this context, they will be used to detect the Cherenkov light produced by the interaction of Ultra-High Energy Cosmic Rays (UHECRs) and neutrinos with the terrestrial atmosphere [5].

Two common approaches to readout SiPMs rely on charge integration [6] or photon counting technique [7]. However, these solutions do not allow studying in detail the signal waveform and, as a consequence, to distinguish the signal of interest from spurious signals created by the direct interaction of cosmic rays within the sensor. For the method to be effective, the waveform should be captured with a sampling frequency of at least 100 Ms/s. A large dynamic range (up to 12 bits) is also required as the energy of the primary particle can span several orders of magnitudes. High integration density is desired to keep the overall system compact and lightweight and low power dissipation is mandatory. Therefore, a single channel should offer a complete signal processing chain with a power budget of only a few milliwatts. Care must be paid to radiation tolerance as well, with particular emphasis on Single Event Effects. On the basis of these considerations, the design of a custom ASIC optimized to read-out a SiPM-based Cherenkov radiation imager has been undertaken. The key target specifications are a sampling frequency of 200 Ms/s, a maximum power consumption of 5 mW/channel and a dynamic range of 12 bits.

2 ASIC architecture

The 64-channel ASIC is being designed in a commercial 65-nm CMOS technology and must operate with a power supply of 1.2 V. The choice of the technology stems from the fact that it provides a good integration density and its radiation tolerance has been extensively studied. The straightforward approach in a waveform sampling system is having one free running ADC per channel followed by a digital signal processor. Despite the impressive progress made in ADC developments [8], [9], the

use of one 12-bit ADC per channel would hardly be compatible with the target power consumption. Furthermore, since the flux of UHECRs is extremely low (0.1 to 100 particles per hour are expected [10]), a continuous digitization is unnecessary. Analog memories provide instead an interesting alternative to capture fast transient signals occurring sparsely in time.

The block diagram of one channel is shown in figure 1. The current pulse coming from the sensor is amplified and converted into a voltage by the input amplifier. The resulting voltage is buffered into a 256-cells analog memory which is used to store temporarily the signal information.

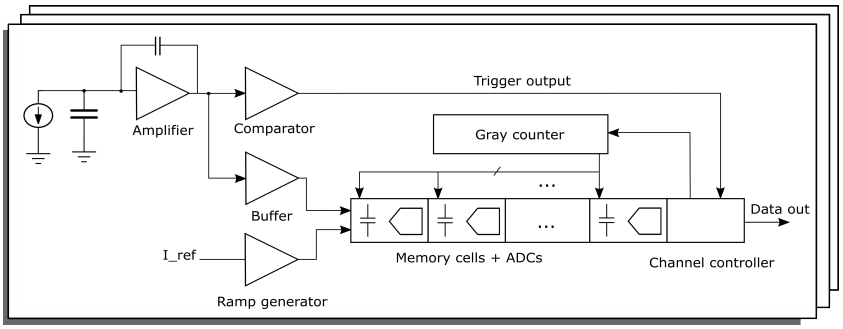


Figure 1: Channel block diagram.

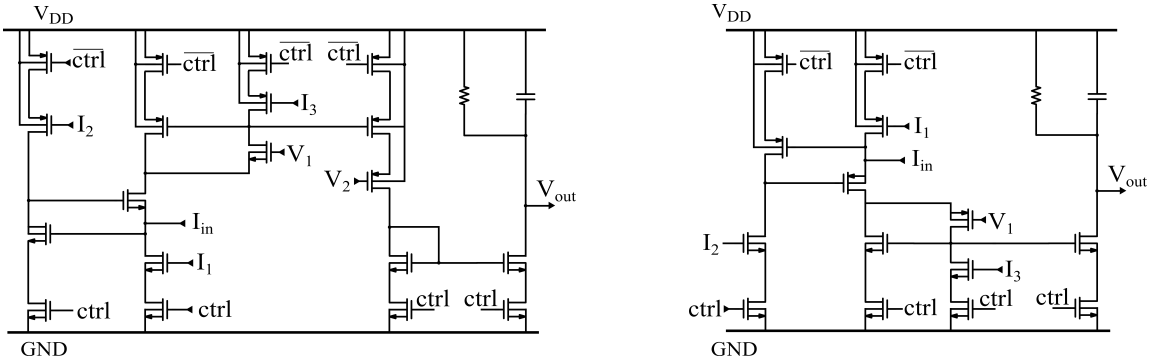
When the sampling is enabled, the cells are written with a frequency of 200 MHz and the memory works as a ring buffer. If an event occurs, a trigger signal is issued and the cells enter the digitization phase, otherwise they are overwritten. In order to perform background monitoring, an external trigger can be sent to the chip. The analog memory can work as a single buffer or it can be divided into a maximum of 8 segments of 32 cells each thus enabling multi-buffering mode. By segmenting the analog memory, the data are derandomized, so the system acquires an event even if the processing of the previous one is still in progress. Furthermore, the channels of the ASIC can be programmed to operate in parallel (imaging mode) or independently from each others (sparse mode). The digitized data are transmitted off-chip by employing a 8-channel Double Data Rate (DDR) serializer operating with a frequency of 400 MHz.

2.1 Front-End

The front-end amplifier is based on the common gate topology [11]. Two different circuits, shown respectively in figures 2a and 2b, have been implemented to read both positive and negative input pulses, thus increasing the flexibility of the chip. The front-end amplifiers are followed by a discriminator (not shown in the figure) that compares the signal V_{out} to a programmable threshold to provide a trigger. In sparse mode, each channel is triggered independently. In imaging mode, two trigger modalities are foreseen: a fast OR between the channels and a topological trigger that looks at the firing on nearby channels. The generated information can either be used to trigger a readout sequence directly on the chip or it can be provided as primitive to an external trigger processor, that looks at the trigger outputs of different ASICs before issuing a final trigger decision.

2.2 Analog Memory

The basic building blocks of the analogue memory is the sampling cell. Several options can be considered to digitize the sampled data. One possibility is to have a fast ADC per channel or



(a) Front-end amplifier with NMOS input.

(b) Front-end amplifier with PMOS input.

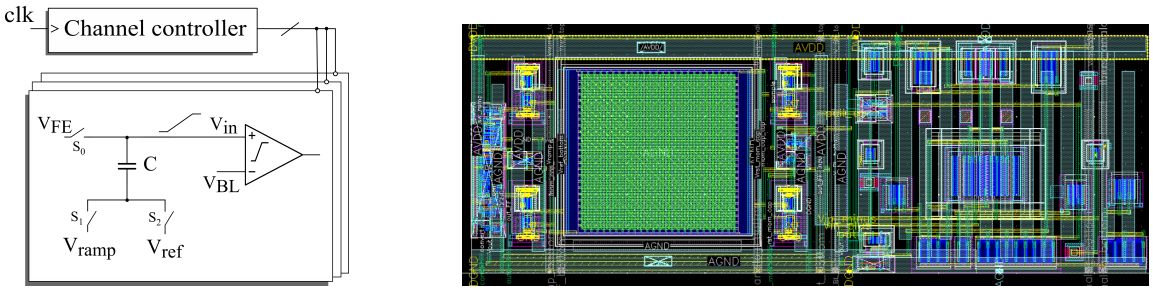
Figure 2

per group of channels. However, even using a moderate speed ADC (e.g. 20 Ms/s), 12.8 μs are needed to readout 256 cells. The Wilkinson ADC topology is attractive for its simplicity, but it has long conversion time. However, it requires a limited number of hardware resources. Therefore, a massive parallelism can be used to keep the overall conversion time of the memory to an acceptable level. For instance, in [12] a fast sampling ASIC with an analog memory of 128 cells is described. The digitization is fulfilled by using 128 10-bit single-slope ADCs placed at the periphery of the chip. Therefore, all the cells in a single channel are converted in parallel. However, the scaling in CMOS technologies allows developing chip with even higher integration density. Hence, in our device a 12-bit single-slope ADC has been embedded direcly in each memory cell. This allows for the digitization of all the samples in the ASIC in parallel thus reducing the dead time. The time needed for the conversion is given by:

$$2^N \times T_{clk} = 20.48\,\mu s \tag{2.1}$$

where N is the resolution and T_{clk} represents the clock period of 5 ns. The resolution of the converter can be programmed between 8 and 12 bits. Hence, with a lower resolution, this time interval is decreased. For instance, for a 10-bit resolution (that could still adequate for our purpose) the conversion shrinks to $5.12\,\mu s$. However, in a waveform sampling ASIC an important contribution to dead time is also given by data transmission. In fact, the digital data stream is composed of a 27-bit long header and the digitized data. By selecting the maximum resolution for the ADC, an amount of 3099 bits per channel must be transmitted to readout 256 cells. Even using 10 Gbit/s serializer per chip the time to send the raw data out would be 19.83 μs. To increase the system modularity and thus its fault tolerance, instead of using a single fast serializer, 8 DDR serializers working with a 400 MHz clock have been implemented. This allows for the segmentation of the ASIC in modules of 8 channels which are basically independent of each other The data transmission time thus becomes $30.99\mu s$ in the worst case in which all the 256 cells are used to capture a single event. It must be pointed-out that the dead-time is not a critical parameter for the application, as only a few events per second are expected to be read-out from the ASIC. Data could be of course zero-suppressed and compressed on chip before transmission, but it has been preferred to shift a more elaborated signal processing to the on-board FPGA.We have chosen

to keep the ASIC as simple as possible to reduce its design time, which is on the critical path of the project, while more time is available to develop the FPGA firmware.



(a) Memory cell building blocks.

(b) Layout of the memory cell.

Figure 3

The building blocks of the memory cell are shown in figure 3a. Each cell includes the sampling capacitor, the comparator of the ADC, some switches and a control logic (not illustrated in the figure). A single Gray counter whose outputs are shared among the cells, is embedded in each channel. In the sampling phase, the storage capacitor is charged to a voltage equal to $V_{FE} - V_{ref}$, where V_{FE} is the output of the input amplifier and V_{ref} is a reference voltage. In contrast with the most common architecture [13], the minus terminal of the comparator is not connected to a ramp generator. In fact, this solution can deteriorate the linearity of the system because the common mode of the comparators changes between the cells. A possible solution consists in fixing the threshold to a steady value while charging the capacitor through a constant current generator. However, the mismatch between the current sources can lead to gain variation between the cells. Hence, a single ramp generator is applied to all the storage capacitor. During the digitization the top plate of the capacitor is connected only to a gate terminal of a MOS transistor, so this node remains floating. Hence, if a ramp generator is connected to the bottom plate, the same voltage variation is replicated on the top thanks to charge conservation. When the voltage on this terminal reaches the threshold, the comparator flips triggering the storage into local latches of the output of the Gray counter. This allows embedding a single ramp generator which is common to all the cells in a single channel as shown in ref. [13]. This alternative approach ensures a good gain uniformity among the cells. The gain of the analog memory can thus be calibrated together with the front-end gain by injecting at the input of the channel known pulses through a programmable pulse generator embedded on chip. The offset is measured cell by cell by feeding a steady input voltage to the cells. This offset can be stored into a local memory and subtracted when the cells is readout

The schematic of the comparator is shown in figure 4b. It has two possible states which are called power-up and power-down mode. The input differential pair and its bias transistors have been divided in two branches. The first branch, which is composed by M_1, M_2, M_7, M_8 drives a quarter of the total current and it is always on. The second branch is formed by M_3, M_4 M_9 and M_{10} and it drives three quarter of the total bias current. The latter is powered on only during the digitization phase by closing switch M_{10}. This arrangement allows for a reduction of the power dissipation when the comparator is not used, while keeping constant its common mode. Simulations show that this reduces kick-back effects toward the sampling capacitor when the comparator is set back to full

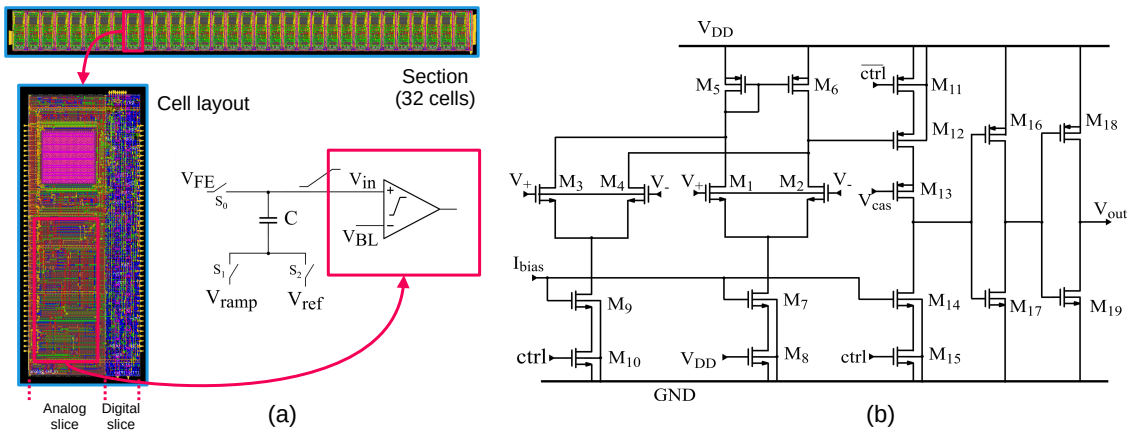


Figure 4: (a) Layout of a section. (b) Schematic of the comparator.

power mode. Before digitization, 2 clock cycles are dedicated to power up the converters and to switch the bottom plates of the capacitors from the fixed reference to the voltage ramp.

The final layout of the cell has a size of $43.62 \times 15.20\,\mu m^2$ and it is illustrated in figure 3b. This sizing allows integrating the analog memory in a chip with final dimensions of $6mm \times 4mm$. The analog cell is integrated with a digital-on-top methodology. Figure 4a reports the layout where the Wilkinson ADC is included alongside the latches. They are divided into a data memory and an offset memory used to store the offset of the converter. The upper part of the image depicts a section in which the cells are hierarchically organized. Each section is managed by a channel controller (not shown in the layout) where dedicated Finite State Machines (FSMs) are implemented. These FSMs take into account the partitioning of cell array by appropriately managing the sampling, digitizing and readout states. The channel controller also drives the configurable Gray counter whose output is distributed to each section. The digital power was evaluated by synthesizing each block and the consumption is limited to 1.3 mW per channel which includes the power contribution of the serializer.

3 Conclusions

This paper presented the architecture of a 64-channel ASIC designed in a commercial 65-nm CMOS technology for SiPM readout in space environment. The input current pulse is amplified, converted into a voltage value and stored into a 256-cells analog memory. The memory cells allow acquiring a snapshot of the incoming event with a resolution of 12 bits. Sampling and digitization steps are decoupled since the conversion starts only if a trigger signal (both generated internally or provided from the outside) is received. This results in a lower power consumption compared to the implementation of a free-running converter. The chip flexibility has been increased by applying the derandomization technique. The power consumption aims to be 5 mW/ch considering both analog and digital circuits. The integration of the building blocks is ongoing and the chip tape-out is scheduled at the beginning of 2023.

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