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Digital-Based Analog Processing in Nanoscale CMOS ICs for IoT Applications

By

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Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

Pedro Filipe Leite Correia de Toledo2022

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I want to dedicate this thesis to all my family.

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Abstract

The Internet-of-Things (IoT) concept has been opening up a variety of applications, such as urban and environmental monitoring, smart health, surveillance, and home automation. Most of these IoT applications require more and more power/area efficient Complementary Metal–Oxide–Semiconductor (CMOS) systems and faster prototypes (lower time-to-market), demanding special modifications in the current IoT design system bottleneck: the analog/RF interfaces.

Specially after the 2000s, it is evident that there have been significant improvements in CMOS digital circuits when compared to analog building blocks. Digital circuits have been taking advantage of CMOS technology scaling in terms of speed, power consumption, and cost, while the techniques running behind the analog signal processing are still lagging. To decrease this historical gap, there has been an increasing trend in finding alternative IC design strategies to implement typical analog functions exploiting Digital-in-Concept Design Methodologies (DCDM). This idea of re-thinking analog functions in digital terms has shown that Analog ICs blocks can also avail of the feature-size shrinking and energy efficiency of new technologies.

This thesis deals with the development of DCDM, demonstrating its compatibility for Ultra-Low-Voltage (ULV) and Power (ULP) IoT applications. This work proves this statement through the proposing of new digital-based analog blocks, such as an Operational Transconductance Amplifiers (OTAs) and an ac-coupled Bio-signal Amplifier (BioAmp).

As an initial contribution, for the first time, a silicon demonstration of an embryonic Digital-Based OTA (DB-OTA) published in 2013 is exhibited. The fabricated DB-OTA test chip occupies a compact area of 1,426 μm^2, operating at supply voltages (V_{DD}) down to 300 mV, consuming only 590 pW while driving a capacitive load of 80pF. With a Total Harmonic Distortion (THD) lower than 5% for a 100mV input signal swing, its measured small-signal figure of merit (FOM_S) and large-signal

figure of merit (FOM_L) are 2,101 V^{-1} and 1,070, respectively. To the best of this thesis author's knowledge, this measured power is the lowest reported to date in OTA literature, and its figures of merit are the best in sub-500mV OTAs reported to date.

As the second step, mainly due to the robustness limitation of previous DB-OTA, a novel calibration-free digital-based topology is proposed, named here as Digital OTA (DIGOTA). A 180-nm DIGOTA test chip is also developed exhibiting an area below the 1000 μm^2 wall, 2.4nW power under 150pF load, and a minimum V_{DD} of 0.25 V. The proposed DIGOTA is more digital-like compared with DB-OTA since no pseudo-resistor is needed.

As the last contribution, the previously proposed DIGOTA is then used as a building block to demonstrate the operation principle of power-efficient ULV and ultra-low area (ULA) fully-differential, digital-based Operational Transconductance Amplifier (OTA), suitable for microscale biosensing applications (BioDIGOTA) such as extreme low area *Body Dust*. Measured results in 180nm CMOS confirm that the proposed BioDIGOTA can work with a supply voltage down to 400 mV, consuming only 95 nW. The BioDIGOTA layout occupies only 0.022 mm^2 of total silicon area, lowering the area by 3.22X times compared to the current state of the art while keeping reasonable system performance, such as 7.6 Noise Efficiency Factor (NEF) with 1.25 μV_{RMS} input-referred noise over a 10 Hz bandwidth, 1.8% of THD, 62 dB of the common-mode rejection ratio (CMRR) and 55 dB of power supply rejection ratio (PSRR).

After reviewing the current DCDM trend and all proposed silicon demonstrations, the thesis concludes that, despite the current analog design strategies involved during the analog block development has been indispensable to unfold several cutting edge applications over the last decades, the DCDM design strategy presented here seems to be very attractive for new technologies and continuing advance analog interface performance, especially for IoT applications. These circuits could take advantage of better awareness of the discrete nature of information and the steadily increasing timing resolution of more advanced CMOS nodes.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The Internet of the Things (IoT) concept aims to turn everyday life objects into smart things by exploiting underlying technologies like ubiquitous and pervasive computing, embedded devices, communication technologies, sensor networks, internet protocols, and applications. The IoT enables physical objects to see, hear, feel, measure, think, and perform tasks by "talking" together, sharing information, and coordinating decisions. The emerging idea of IoT is rapidly finding its momentum throughout our modern life, aiming to increase our comfort and improve our quality of life.

The IoT architecture embracing all abstraction levels needs to be carefully conceived to make this concept reasonably viable. Challenges should be pointed out and addressed, including facts related to the cheapest technology that makes it possible: Complementary Metal Oxide Semiconductor (CMOS) technology. Devices made in CMOS are deployed on the edges of the IoT network gathering information from the physical world and sharing back to the cloud for more ambitious analytic capabilities.

Such edge devices, i.e., integrated circuits (ICs), comprise analog, mixed-signal, radio-frequency (RF), and digital processing capability (for instance, to get precise information from the sensors), and the definition of their architectures, technologies, and design methodologies play a fundamental role in the final performance of the whole system. Such aspects are intrinsically related to the last ICs area and power consumption, which in turn can be several times the IoT chain bottleneck. In other words, often, the edge device performance dictates the final decision to evaluate whether that application is viable or not.

In this introduction, the section 1.1 exposes the IoT concept principles as well as its applications, also showing their current market perspectives. In section 1.2, IoT network architectures are briefly reviewed, focusing on the CMOS edge devices description. Challenges found in such devices during their design are described in section 1.3, outlining the main current analog and digital techniques for power reduction. Based on several examples, the Digital-in-Concept Design Methodology (DCDM) trend is then introduced as an alternative design approach for the next generation of low power analog circuits within IoT nodes in section 1.4. The thesis organization is outlined in section 1.5, stressing how the following chapters are organized and the main thesis contributions.

1.1 IoT Concept and Applications

In 1999, Kevin Ashton, co-founder of the Auto-ID Laboratory at MIT, gave birth to the term Internet of Things [42]; however, the general concept idea has been around for much longer. Back in the early 80s, at Carnegie Mellon University, a group of students designed a system to get their campus Coca-Cola vending machine to report on its contents. They could make the machines let them know whether newly loaded drinks were cold or not. Later, in 1990, John Romkey connected a toaster to the internet for the first time using File Transfer Protocol (FTP) [43].

In the following years, worldwide organizations and research institutes started to become excited about the Internet of Things, and several definitions and visions were proposed and spread. The International Telecommunication Union (ITU) delineates IoT as a universal information infrastructure for the society, permitting advanced and sophisticated services by interconnecting objects based on existing and evolving communication technologies [44]. Both the UK Government Office of Science and the European Commission share a similar outlook of the IoT: *a world in which everyday objects are connected to a network so that valuable data can be shared* [45, 46]. Among all definitions found in the current literature, common characteristics of each of these visions can be narrowed into four well-clear principles:

- Global scale principle: the IoT exists at a global scale [47].
- Physical world interaction principle: it consists of uniquely identifiable things with sensing or actuating capabilities linked to the physical world [48].

- Interconnection principle: things are interconnected by existing or future technologies so that data can be shared [49, 50].
- Servicing principle: analytics derived from gathered data have potential for societal impact through advanced services [46].

From the most cited paper about IoT in the Institute of Electrical and Electronics Engineers (IEEE) database [1], Fig.1.1 illustrates the global and comprehensive IoT concept in which every single domain-specific application is interfacing with domain-independent services, whereas in each domain sensors and actuators (IoT nodes or edge devices) broadcast relevant information directly with each other [1]. Even though Fig. 1.1 summarizes reasonably well the IoT general concept through two abstraction levels/domains; this picture is far away from an authentic representation of the entire IoT network architecture, its challenges, and its real applicability potential. In the following section 1.2, the current state-of-the-art of the IoT architectures is shown, giving special attention to the challenges found on the hardware implementation of the edge devices.

The list of applications is extensive in enterprise settings, numbering more than two hundreds known applications, as reported by McKinsey [3], from healthcare to monitoring chemical processes [51–78]. Regardless of its nature, all the above-cited applications needs in general to pursue six goals: *identification*, *sensing*, *communication*, *computation*, *services* and *semantics* [46]. *Identification* is mandatory for the IoT to name and match services based on the demand. The IoT *sensing* means gathering data from related objects within the network and sending it back to the cloud. The IoT *communication* circuits connect heterogeneous objects together to deliver specific smart services. Processing units (e.g., microprocessors (MCU), SOCs, FPGAs) and software applications represent the *computational* IoT ability. As reported in [46, 3], IoT *services* can be categorized into identity-related services, information aggregation services, collaborative-aware services, and ubiquitous services. In IoT, the definition of *Semantics* attributes to the qualification of distilling knowledge by distinctive sources to afford the required services [46].

The vast list of applications and their potential services bring an appropriate amount of expectations and, the latter, investments. In 2013, McKinsey had highlighted a 300% growth in connected IoT devices in the last five years and a potential economic growth rate from 2 to 6 trillion annually by 2025. McKinsey had also

Fig. 1.1 *Vertical markets*: smart things with their supposed functions constitute domain specific applications. *Horizontal markets*: application domain independent services with ubiquitous computing and analytical services [1].

shown in [2] its prediction of market share by 2025, as depicted in Fig.1.2a. In 2019, McKinsey updated these numbers, keeping the same optimism and presenting more interesting parameters [3]. At that year, the annual economic benefits related to the IoT were expected to reach 3.9 trillion to 11.1 trillion by 2025 (2X times compared to 2013). Moreover, the businesses number that use IoT technologies had increased from 13 % in 2014 to about 25% in 2019, the number of IoT-connected edge nodes around the world was predicted to escalate to 43 billion by 2023, and investments were projected to grow at 13.6% per year through 2022 [2, 3]. Fig.1.2b also emphasizes (red square) that there is still room for economic growth in the

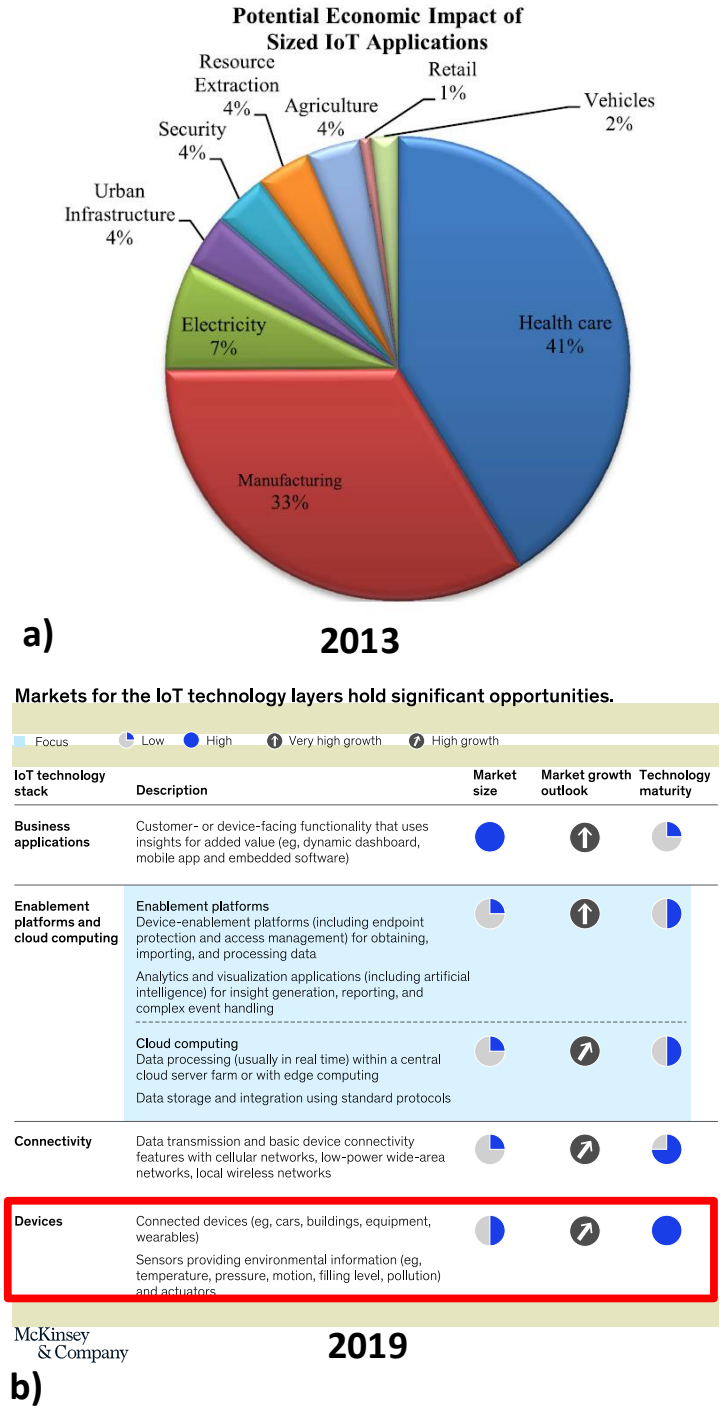


Fig. 1.2 a) McKinsey shows in 2013 its prediction of market share by 2025 [2] b) Significant opportunities along the IoT technology layers, highlighting a healthy market growth for edge devices [3].

device layer (edge devices or IoT nodes, which are the focus of this thesis) within the IoT technological stack. Also, in [3], it is quoted that "Smart devices—the foundational layer of the IoT technology stack and the most mature product category—are dominated by large manufacturers and specialist suppliers and enjoy healthy market growth."

Although relatively imprecise, all these speculations point to the potentially significant and fast-paced growth of the IoT, especially applications related to industries and services.

1.2 IoT Network Architecture and Edge Nodes

The IoT architecture must be able to interconnect billions (Giga) or trillions (Tera) of heterogeneous objects through the Internet, demanding a flexible layered architecture [1]. Fig. 1.3 shows the most relevant IoT technological stacks found so far in the literature [1]. The basic model is the three-layer architecture consisting of the application, network, and perception layers. Some other models have been proposed adding more abstraction such as middle-ware-based, service-oriented architecture (SOA) based, and five-layers [79].

Once the five layers have a similar network shape as in current internet protocol (i.e., the Transmission Control Protocol/Internet Protocol- TCP/IP), Al-Fuqaha et al. affirm that the research and standardization point to this direction [1]. Each layer can be described as follows:

- **Business Layer:** The business layer manages the overall IoT system activities and services. Its responsibilities are to build a business model, graphs, flowcharts, etc., based on the received data from the Application layer. In this layer, it is where is supposed to be implemented most of the analytics [46]. In addition, monitoring and management of the underlying four layers are achieved at this layer. Once it is very close to the final client, this is the layer with the significant market impact.
- **Application layer:** The application layer provides the services required by the customers [80]. For instance, the application layer can provide precious information such as data from the sensors to the client who asks for. This

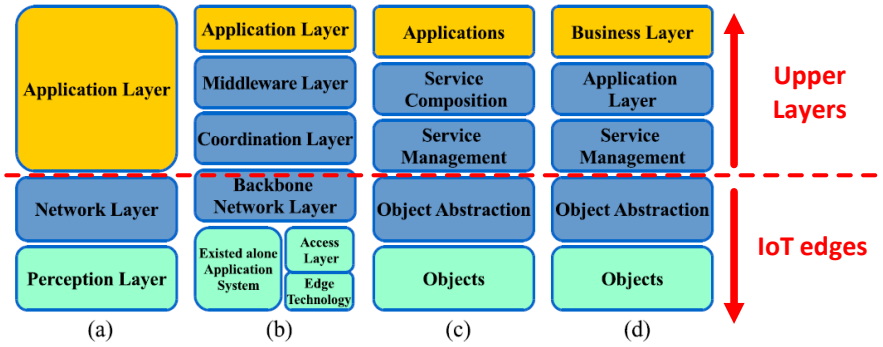


Fig. 1.3 The IoT architecture. (a) Three-layer. (b) Middle-ware based. (c) service-oriented architecture (SOA) based. (d) Five-layer [1].

layer importance is that it can offer high-relevant smart services to fulfil the customers' needs [80].

- **Service Management:** This specific layer matches services to its requester based on addresses and names [80]. This layer enables IoT applications to work heterogeneously with the data regardless of the hardware platform found below in the stack. In addition, it processes received data, deciding and delivering the needed services over the network protocols [80].

- **Object Abstraction:** This layer transfers data produced by the Objects layer to the Service Management layer through secure channels [81]. The information can be shared through various technologies such as NFC, ZigBee, IrDA, UWB/IR, ANT, DASH7, Z-Wave, RPL, BTLE, 6LowPAN, 802.15.4, SAN, etc [82].

- In the first layer (**perception layer**), **the smart objects or edge devices**, serves as an IoT external-physical sensors which aim to gather and post-process the relevant information by demand [1]. Edge devices comprise sensors and/or actuators to perform different functionalities[1]. Standardized plug-and-play mechanisms still be a challenge in this layer due to their intrinsic heterogeneous characteristics. The perception layer digitizes and transfers data to the Object Abstraction layer through secure channels.

In this entire ecosystem, there is a set of challenges at which one is worthy of being mentioned: availability and reliability. The IoT availability must be considered

in the hardware and software levels to provide services for customers anywhere and anytime. Hardware availability refers to the existence of devices that are always compatible with the IoT functionalities and protocols. The challenges related to the hardware system, which generates and collects data (IoT nodes or devices placed on the edges), are deeply investigated here, leading us to conclude the need to design ultra-low-power/area CMOS systems. These systems also include analog/RF IoT interfaces.

Fig.1.4 shows an ordinary block diagram for an edge device, which affords some capacity to measure and interpret the raw data before connecting to a gateway, and subsequently, to the cloud [4, 83]. In this case, the data is processed with some analytics before it is sent for deeper data mining. Albeit the block diagram presented here can be further reduced by eliminating the signal processing and analytic subblocks, i.e., leaving these tasks to the cloud to reduce the total node power/area, the current trend is to increase the computing resources on the edges to minimize the big data issue [84, 85]. A wide spectrum of prepossessing strategies have been studied and proposed in the IoT context such as principle component analysis (PCA) [86], pattern reduction, dimensionality reduction, feature selection [87], compressed sensing [88], and distributed computing methods [89].

In the IoT architecture context, embedding more and more computing ability on edges is called Fog Computing (a.k.a. cloudlets or edge computing). Fog resources can perform data aggregation to send partially processed data instead of raw data to the cloud data centers for further processing. Fog resources can be positioned either in intelligent objects or before the cloud data centers; thus, providing a better delay-performance trade-off [1] (See Fig. 1.5 for better illustration).

Nowadays, hardware availability to gather and process the environment information is strictly related to the cheapest technology used to develop the IoT nodes, i.e., CMOS technology. Integrated Circuits (IC) techniques connect CMOS devices using electronic design automation (EDA) tools. Such tools follow design flows. The Fig. 1.6 shows a simplified view of the two main IC design flows used to develop the hardware of IoT nodes: digital and analog design flow [5].

Digital design flow automatically creates the final circuit layout based on a given design specification and design constraints. Depending on a fixed amount of layout components available from a design library as standard cells (logical gates), a high level of automation in digital design is achieved by heuristic algorithms that usually

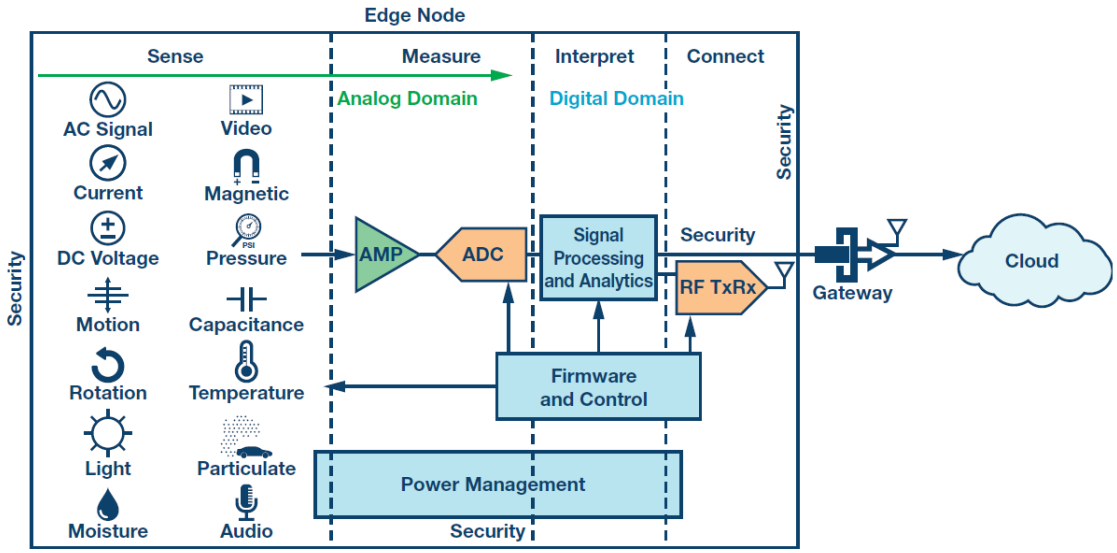


Fig. 1.4 Modern edge device with embedded intelligence before connecting to the cloud. Analytics can be applied to pre-process the raw data coming from the sensors before sending it upwards for deeper data mining analysis [4].

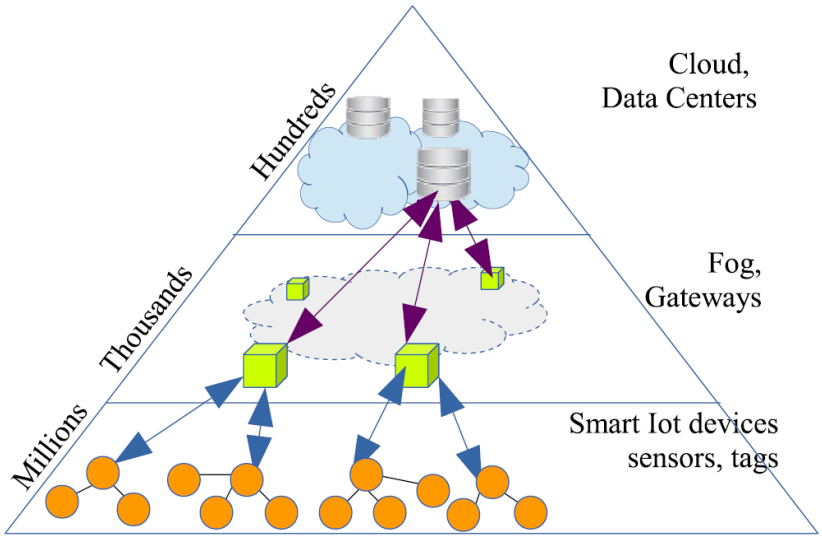


Fig. 1.5 The role of the cloud and fog resources in the delivery of IoT services [1].

perform the different layout tasks like placement and routing. This automation is also possible due to the discrete nature of digital signals [90], reducing the total design time, layout design effort, and time to market.

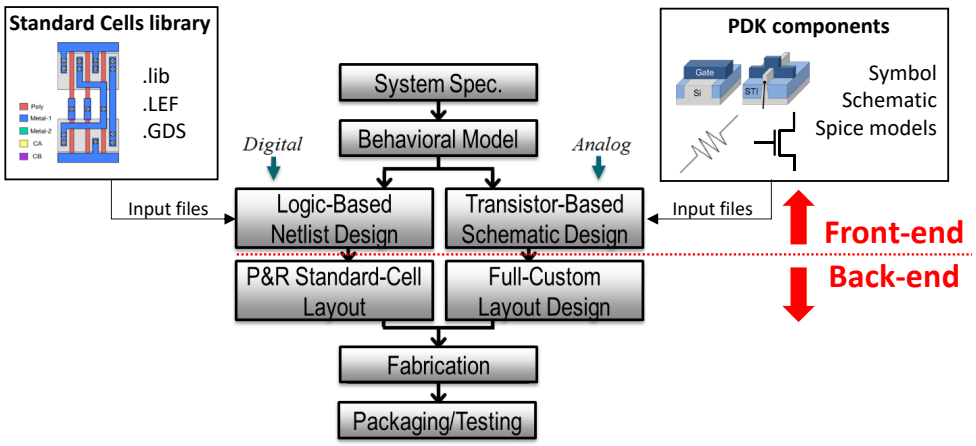


Fig. 1.6 Simplified IC Digial and Analog Design Flow [5].

On the other hand, in the analog/RF domain, design productivity is considerably smaller than for digital circuits, especially in advanced CMOS technologies. As shown in the Fig. 1.6, full custom design flow is adopted to implement analog and RF blocks, simulating their schematic views numerically and doing placements and routing manually to reduce layout-parasitic side effects. This flow is assumed because analog interfaces handle continuous-time, continuous amplitude signals from diverse physical sources (from sensors, for instance), mutual perturbation, and parasitic effects. Such requirements demand to comprehensively harness the entire spectrum and variety of all available degrees of freedom from the process design kit (PDK) components (transistors, capacitors, resistors, diodes, etc.).

In the next section 1.3, the IC design challenges related to developing IoT nodes are revised based on available devices in the current electronic market, showing the need for new design techniques to reduce analog block power and area. Based on this demand, in the section 1.4, Digital-in-Concept Design Methodologies (DCDM) are introduced and reviewed, defining the fundamental concept for the subsequent thesis chapters.

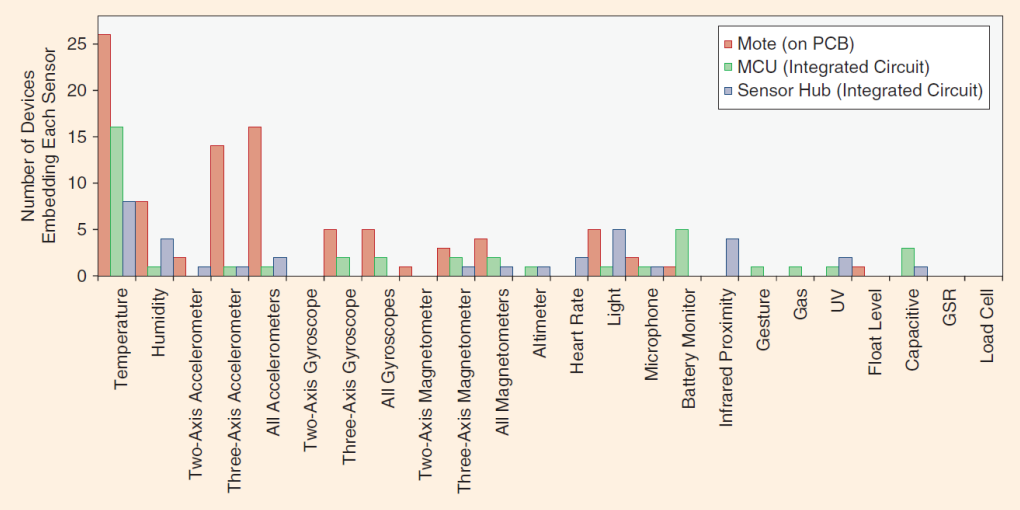


Fig. 1.7 A histogram of commercial IoT devices embedding each type of sensor [6]. This survey of commercial IoT devices was done on a worldwide scale, using platforms such as Digi-Key to collect the data.

1.3 IoT Challenges in IC design

1.3.1 General Challenges Based on the IoT Nodes Available on the Market

The integrated circuits IoT nodes, depicted in Fig. 1.4, aim to have sensing and processing capabilities, to be communicatively accessible, unobtrusive (reduced form-factor), cost-effective, untethered (self-powered), and long-lived (to avoid maintenance costs) [7]. In 2018, [6] released a proper survey regarding the current state-of-the-art of commercial IoT devices, comprising Motes (PCBs), MCUs, and sensor hubs. This survey of commercial IoT devices was done worldwide, using platforms such as Digi-Key to collect the data.

Sensing and processing capabilities in IoT nodes are required to process sensed data locally to a certain extent. Fig. 1.7 shows a histogram of commercial IoT devices embedding each type of sensor [6]. Temperature sensors are the most widely diffused ones mainly due to their intrinsic compatibility with the semiconductor itself. However, a drawback is clearly seen in these devices that concerns the interface resolution. Each sensor resolution needs to be tweaked to the maximum resolution

across several applications domain to maximize its flexibility, i.e., to cover the largest possible market, it is common to find ADC overdesign adding a relevant energy waste. On average, an Effective Number of Bits (ENOB) of 6.2 bits is the resolution found in this survey within this broad sensor type spectrum.

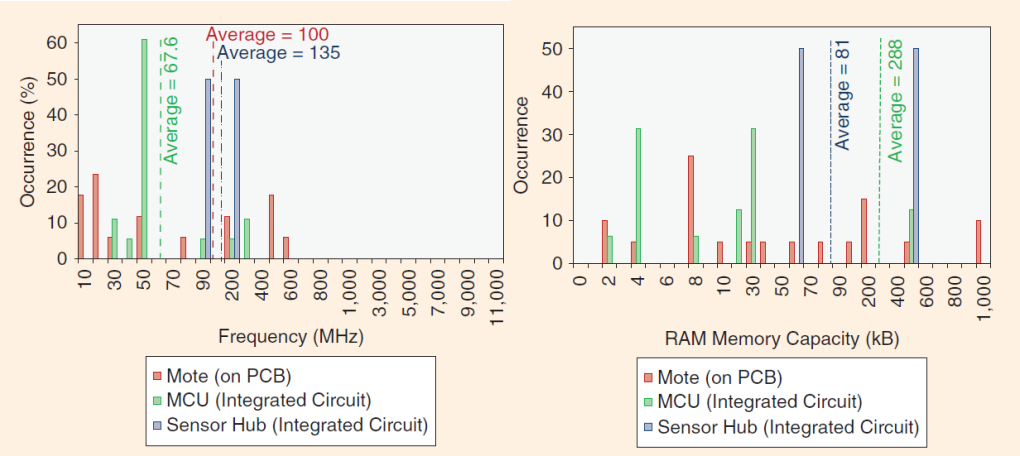


Fig. 1.8 A histogram of maximum microcontroller clock frequency and of RAM memory capacity in commercial IoT nodes [6].

Some computing power is expected to be available in the IoT nodes to partially process the raw data and deliver more enriched information up to the next layer [91, 92]. In [6], all types of IoT nodes are based on microcontrollers. Typically, the microcontroller is an ARM Cortex M0-M4, MSP430, 8051, Atmega, XSCALE, and QUARK. Most of the integrated MCU has 50 MHz of maximum clock frequency while containing 288kB of RAM capacity as a mean value, as justified by their on-chip implementation (see Fig. 1.8). For no-volatile memory, the on-chip flash memory capacity in MCUs is typically around to 64 kilobytes [6].

The IoT nodes need to transmit raw, preconditioned, compressed, or distilled data (e.g., extracted features). It can be done either in a wireline or wireless mode. Serial peripheral interfaces (SPIs)/inter-integrated circuits (I2Cs) for intra-sensors communication and universal serial buses (USBs)/universal asynchronous receiver-transmitters (UARTs) for setting information sharing inside of cables are the most common wireline interfaces. For wireless communication, most MCUs operate at 2.4 GHz. At the same time, motes are more diversified in terms of carrier frequency, being 60% working at ISM-band. In contrast, the remaining ones operate at different available bands (i.e., from 315 to 1,900 MHz). Wireless interfaces are

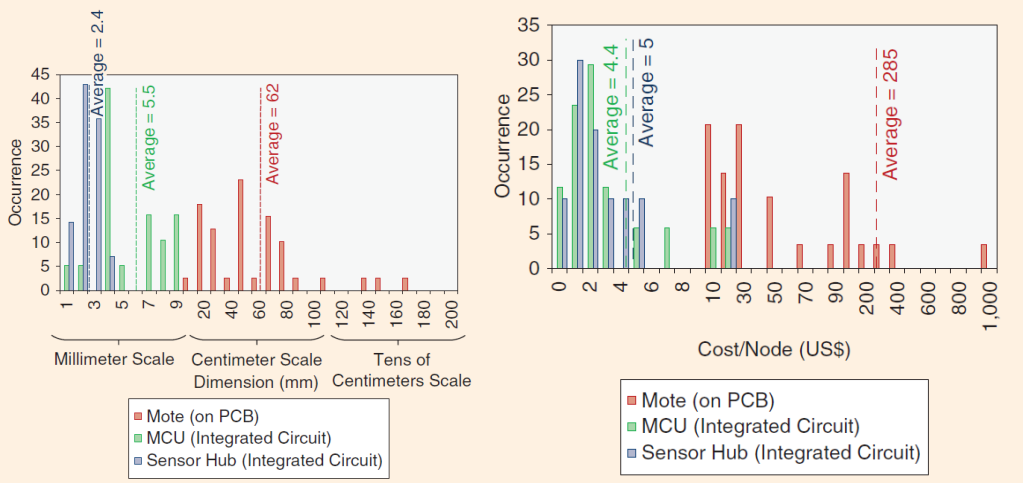


Fig. 1.9 The commercial devices size and cost for distributed sensing [6].

well known for a significant fraction of the IoT device power consumption, with best-in-class commercial radios consuming an energy per bit on the order of a few tens of nanojoules per bit [6]. However, there are numerous academic prototypes with the energy-efficiency around one nJ/bit. The bad news is that the energy/bit is expected to rest relatively constant in the decade ahead (1.34x/year for sub-GHz and 1.42x/year for GHz frequency carrier [93]). Even worse, during transmission, the energy per bit cannot be further reduced through improvements in modulation techniques and spectral efficiency for the already existing schemes with reasonably low complexity (e.g., on-off keying). They are only 10 times (or 10 dB) surpassing the minimum theoretical limit [83, 94].

The IoT node size is another vital specification once it could enable or jeopardize the application. Following Bell's law, personal computers have been historically shrinking by 10–100× per decade; hence, the IoT is also expected to harness this size shrinking. Fig. 1.9 shows the form-factor of commercial off-the-shelf IoT devices found in the market until 2018. A sub-10mm-scale MCU (with an average size equal to 5.5 mm^2) is encountered, while the centimeter scale is found for motes mounted in PCB, which have more functionalities than the MCUs alone.

Supposing that the goal is to have one trillion devices connected in the following years (global scale principle from section 1.1), taking from Fig. 1.9 the 62 mm^2 as the size of each IoT, this will lead to a total area equal to 0.0000416% of total land earth area, making one trillion a reasonable number. From a manufacturing

perspective, as described in [95], if it is assumed 2 mm^2 per IoT sensor device (a little lower than sensor hub from Fig. 1.9), or 35,000 packed ICs per 300mm wafer, a trillion devices would need 28 million wafers. That is ≈3X the annual capacity of the industry's largest foundry (Taiwan Semiconductor Manufacturing Company or TSMC until the date of this thesis); but just one third of 2017's total annual worldwide production. So in this context, it is still achievable [95].

Also, in Fig. 1.9, the cost per device type is plotted. For the motes, the average cost/node is about 285 dollars. Such high cost is mainly due to the lack of economy of scale in PCB-based motes (PCB manufacturing and assembly costs, for instance). According to the International Monetary Fund (IMF), in 2020, the United States Gross Domestic Product (GDP) was 20.93 trillion, 14x less than 1 trillion times 285 dollars. It gives us insight into the amount of money involved to deploy one trillion devices and shows that the value of $285/mote is unfeasible. Therefore, a significant reduction in cost/unit is essential.

Even though this scenario is more favorable for integrated MCUs (1/4 of USA GDP), it seems that maintenance cost per device would be of the same order of magnitude if each device needed at least one repair per year (for instance, to change the battery). In [7], a maintenance estimation is done, and tens of dollars for each battery replacement is predicted, corresponding to an unbearable ≈$4 trillion (or higher) per annum globally. In this perspective, the IoT node power consumption becomes an essential parameter.

For low area IoT nodes (one of the primary goals of this thesis), lower power consumption leads to better miniaturization for a given lifetime target, as the battery mainly sets the system size. It also leads to significantly lower costs once battery cost becomes a significant fraction of the whole system. Eq. (1.1) shows how the lifetime of an IoT node is calculated [7].

$$T_{lifetime} = \frac{E_{BAT}(0)}{P_{stdby} \cdot (1 - DC) + \overline{P_{system}} \cdot DC + P_{self-discharge}} \tag{1.1}$$

where $T_{lifetime}$ is the total lifetime, $E_{BAT}(0)$ is the battery capacity, P_{stdby} is the IoT node standby power, $\overline{P_{system}}$ is the IoT node active power, $P_{self-discharge}$ is the battery self-discharge and $DC = \frac{T_{on}}{T_{on}+T_{stdby}}$ is duty cycle ratio which defines how much time

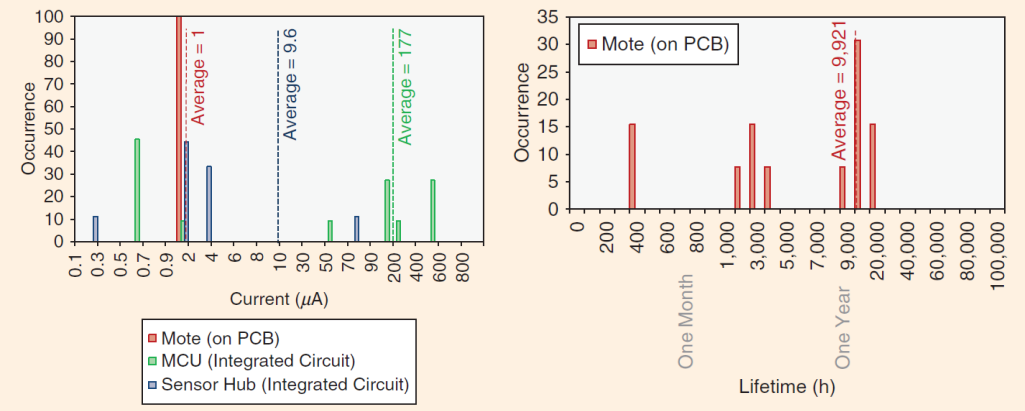


Fig. 1.10 A histogram of standby current and the estimated lifetime of commercial IoT nodes at 1% duty cycle. [6].

the system is between active (T_{on}) and standby (T_{stdby}) mode. Eq. (1.1) is true for time-driven duty-cycled systems, where the IoT node activation can be duty-cycled ($DC = \frac{T_{on}}{T_{on}+T_{stdby}}$) by introducing the standby mode (or sleep mode) with short and periodic wake-up ($T_{wkup} = T_{stdby} + T_{on}$). Lower DC ($T_{stdby} >> T_{on}$) means more power is saved to the detriment of an increased probability of missing events of interest and higher event detection latency [7].

In [6], commercial IoT devices' lifetime (motes in this case) has been estimated using two AA batteries as power supply to earn more insight into the dynamic powering of IoT systems. Each AA battery has 2600 mAh of capacity and 5 μA of self-discharge current. Assuming 1% duty cycle (DC) and 1 μA of standby current under $V_{DD} = 3.6V$, Fig. 1.10 shows an average lifetime of one year. Using Eq. (1.1), the average active power ($\overline{P_{system}}$) can be also estimated, which is around 186.5 mW. For the current IoT nodes available on the market, at least two/three orders of magnitude improvements in energy efficiency are required to meet the IoT device's ultimate goal of a decade-long life (no maintenance cost regarding battery issues).

Basically, IoT nodes must be more energy-autonomous, given their massive number of installed devices. Operation in the microwatt and sub-microwatt range is typically required for a decade-long lifetime under the given device size constraint [7]. Fig. 1.11 shows the IoT node lifetime versus the total system power $\overline{P_{system}}$ for different batteries (AA battery, coin cell, and thin-film battery (TFB)). Regardless the battery nature, the lifetime upper bound is approximately one decade, limited by the battery shelf life calculated using Eq. (1.1) for $P_{stdby} = \overline{P_{system}} = 0$. From this

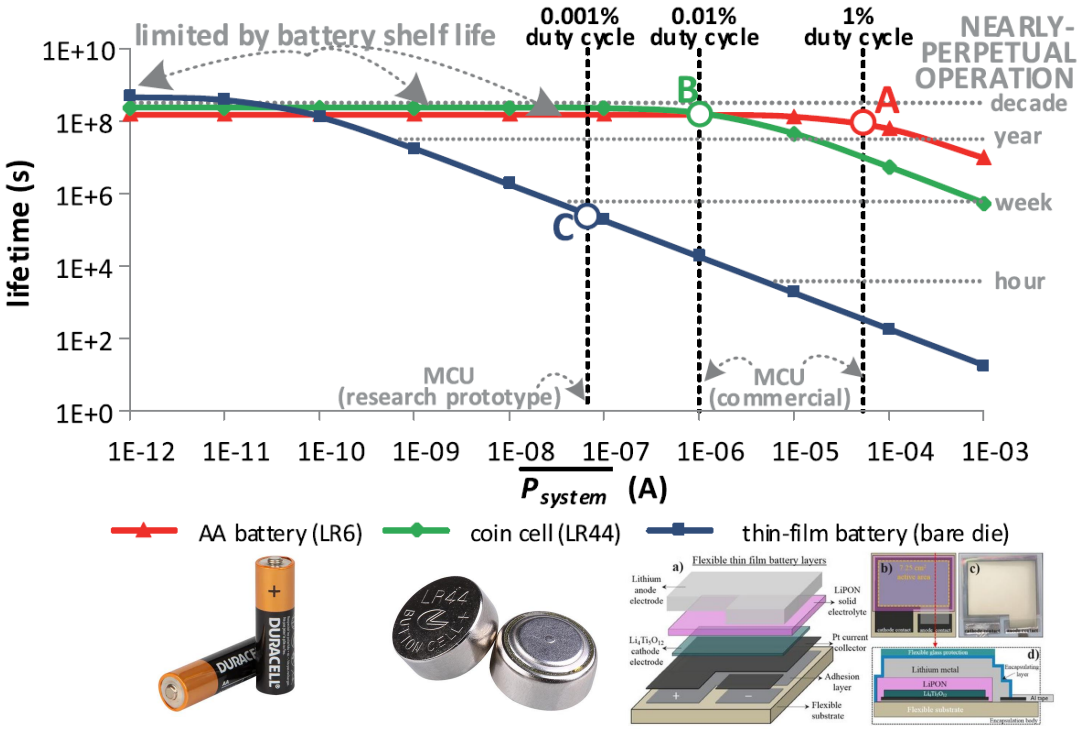


Fig. 1.11 System lifetime versus system power $\overline{P_{system}}$ for different batteries. [7, 8]. $DC = \frac{T_{on}}{T_{on}+T_{stdby}}$ is the duty cycle ratio which defines how much time the system is between active (T_{on}) and standby (T_{stdby}) mode.

picture, it can be realized that only a few days of autonomy are achieved for TFB and using commercial MCU with $DC = 0.001\%$. For research MCU prototypes, the autonomy can reach up to one week for a more aggressive DC, even though just a hundred nW is consumed. As shown in the picture, one solution would be to change the battery type for the coin cell, increasing the whole system form-factor and cost once bare-die (i.e., unpackaged) solid-state batteries are as inexpensive as standard silicon dice (deep sub-$).

Another alternative is to harvest the surrounding available energy sources. Energy harvesters allow the usage of rechargeable batteries with relaxed single-charge capacity and hence small form factor and low cost while still preserving the battery life (Hybrid solution). Fig. 1.12 depicts the necessary harvester size for a given power target for several types. Based on that, an mm-scale harvester is enough to power 100 nW regardless of its nature, making the system either battery-light or battery-free (direct harvesting).

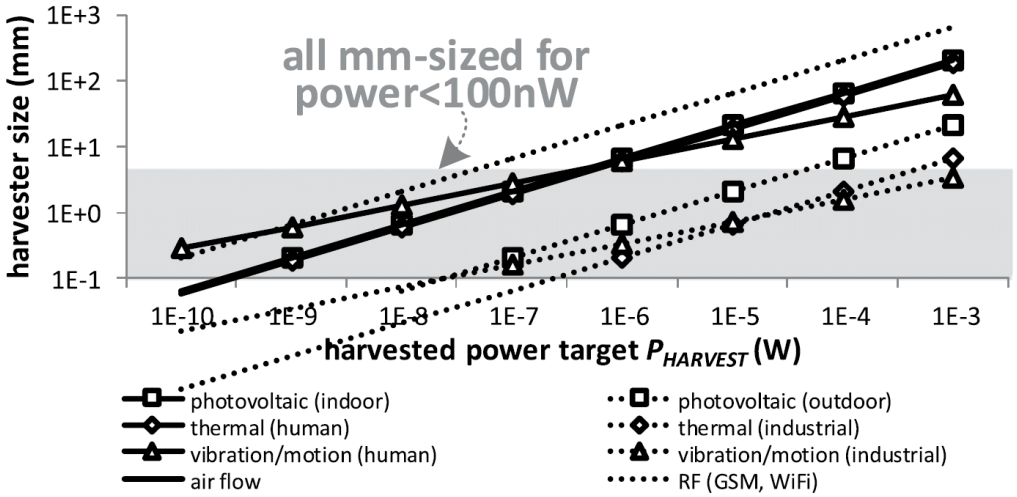


Fig. 1.12 Required harvester size for a given power target for several types of harvesters [7].

In fact, regardless of the energy source type (battery or harvester), low-power IoT systems are indispensable. In the following subsections, digital and analog circuit techniques for power reduction are revisited.

1.3.2 Digital Circuit Techniques For Power Reduction

In the previous subsection, at least one order of magnitude gap between the current status of commercial IoT devices and their ultimate targets has been identified in most aspects (e.g., lifetime). Such limitations are all tightly associated with the inadequate power efficiency of existing devices. In other words, the size-lifetime-cost of IoT nodes will eventually be dominated by the energy source (e.g., battery), and improvement of their power efficiency will be necessary for making the battery more minuscule (less expensive) and their energy harvester in sub-mm-scale while extending the lifetime.

Due to these reasons, to keep the IoT dream alive using CMOS technologies, integrated circuits and distributed sensing systems must be essentially battery-light or battery-less with the lowest power/area possible while trading off the processing workload w.r.t. the entire IoT network stack (fog computing, see Fig. 1.5).

In digital circuits, scalable energy–quality operation is a valuable tool for low-power design. It dynamically manages the tradeoff between energy and data processing quality, minimizing the former to achieve just-enough quality [16]. The application itself dynamically sets the quality target [96, 97]. IoT nodes can considerably benefit from energy–quality scaling, considering that their processing deals with physical signals, which are noisy and hence can be processed with a quality that is commensurated with the level of noise and the acceptable accuracy required by the task at hand.

Dynamic Voltage Scaling (DVS) [98–100] and body biasing [101, 102] are powerful techniques for low-power digital design in static CMOS logic family. Still, typically energy reduction by up to 2 orders of magnitude at ULV is obtained with a speed penalty by 2–5 orders of magnitude. An aggressive pipeline to further reduce the energy per operation is also a good option [103].

In schematic level, a dedicated standard cells library (stdcells) is also a good design approach to reduce further the absolute power, and energy [104]. For instance, higher threshold selection is a more relevant circuit knob compared to the transistor sizing itself. Logic gates with fan-in greater than 2-3 (i.e., no more than two stacked transistors) as well as topologies based on current contention must be avoided. During the transistor sizing, the PMOS/NMOS imbalance is a crucial design parameter that strongly influences the robustness of the stdcells [105].

Not only changing the circuit design approach for CMOS static family makes the difference for digital circuit power reduction, but the development of new logic families has also been demonstrated significantly efficient. Fifteen years ago, David Bol proposed a new family of ultra-low-power low-frequency logical gates [106], now known as Dynamic Leakage-Suppression (DLS) Logic [9]. This kind of logic permits putting the transistor in the super-cutoff region after the transition is done, though suppressing the leakage current and limiting the short circuit current during the state transition. Such operation leads to shallow power consumption levels enabling new horizons for battery-light and direct-harvesting IoT applications. Its drawback comes from the limited speed and low voltage swing compared to static CMOS. Fig.1.13a shows a DLS inverter cell in schematic and layout. In Fig.1.13c [10], a comparison between CMOS and DLS logical style is seen in terms of power and maximum frequency operation for an MCU implementation. It shows sub-100nW power consumption is possible using DLS logical style.

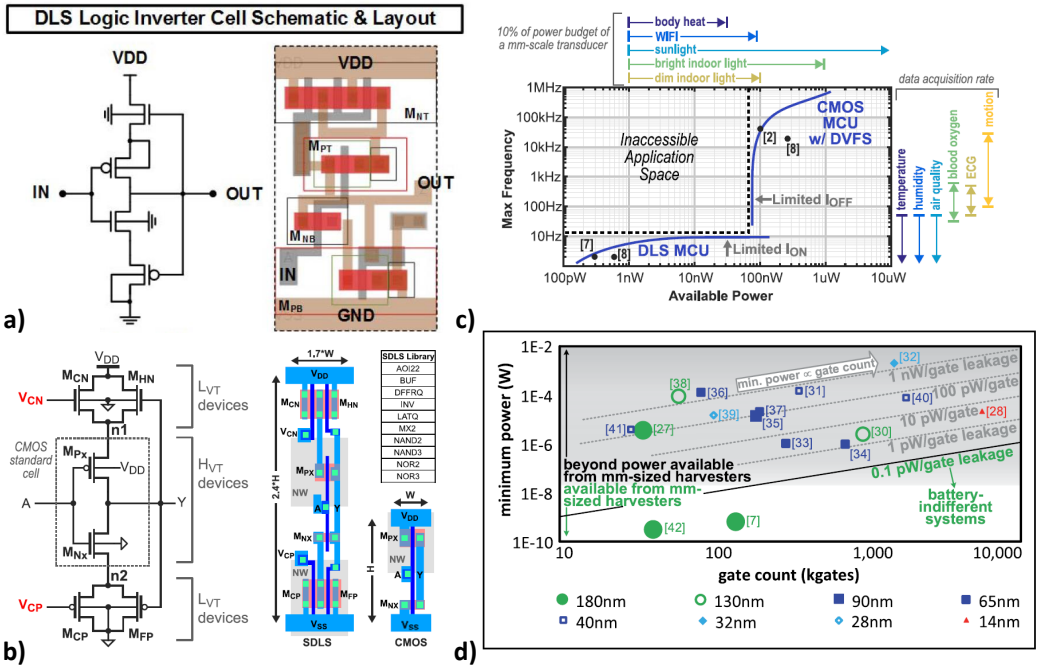


Fig. 1.13 a) DLS inverter cell, schematic and layout [9] b) CMOS and DLS comparison for a MCU implementation [10] c) Dual-Mode Standard Cells [11] or Scalable Dynamic Leakage-Suppression (SDLS) logic style [10] d) Gate count in Kgates versus minimum power consumption in state of the art MCU [7].

A variant of DLS called as Dual-Mode Standard Cells [11] or as Scalable Dynamic Leakage-Suppression (SDLC) logic [10], shown in Fig. 1.13c, has also been proposed. SDLC allows an ultra-wide power-performance trade-off considerably beyond the classical static CMOS voltage scaling and adaptation to the sensed power/energy availability from the harvester and battery, as demonstrated in [11]. Finally, in [7] and also in Fig. 1.13d, it is shown that DLS is the unique logical style so far able to operate an MCU consuming sub-10nW power consumption.

1.3.3 Analog Circuit Techniques For Power Reduction

Generally speaking, the design of low-power and low-voltage analog circuits is the talent for finding the suitable trade-off between conflicting constraints or specifications, as illustrated by the famous analog design octagon [12, 13], in Fig.1.14a. Power, noise, linearity, gain, supply voltage, voltage swing, speed, and input/output

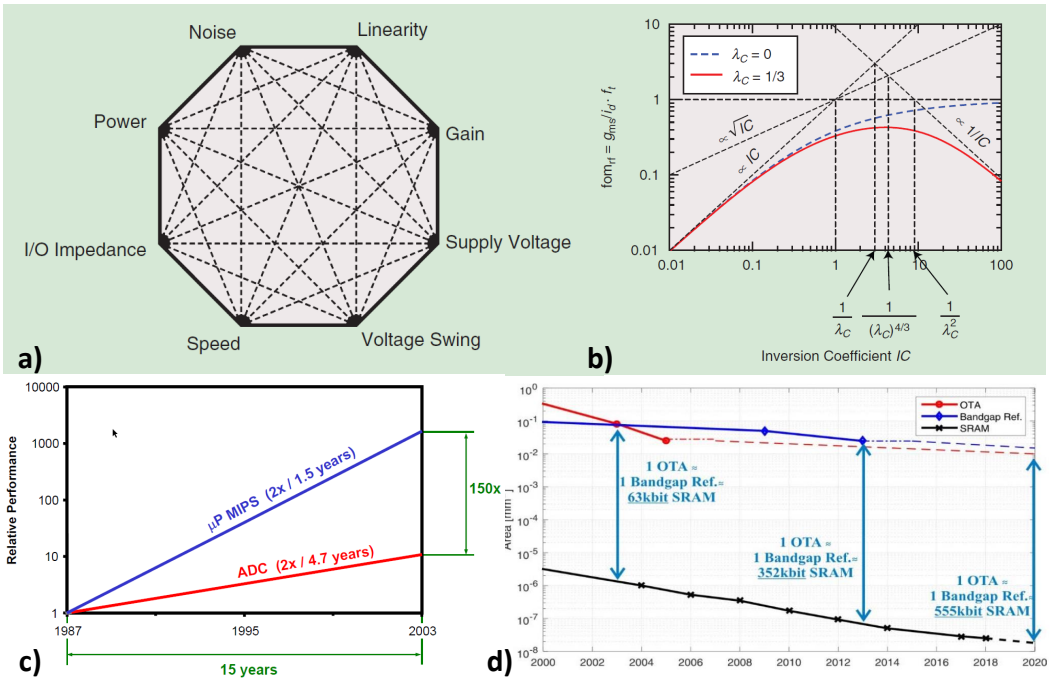


Fig. 1.14 a) analog design octagon b) $g_m/I_D \cdot f_T$ versus the inversion coefficient IC, λ_c is the parameter corresponding to the fraction of the channel in which the carrier drift velocity reaches the saturated velocity over a portion of the channel geometrical length [12, 13] c) Performance difference between analog and digital blocks over time [14, 15] d) Area reduction over the years of the bitcell SRAM, OTA and Bandgap reference [16].

impedance are some parameters typically found during the analog IC design (see Fig.1.14b).

Usually, in the literature about analog design strategies for low power goals, the transistor bias point is the leading circuit knob investigated. In [107], the transistor inversion level (bias point) is deeply related to essential Figures of Merits (FoM), like transconductance efficiency (g_m/I_D), transit frequency (f_T), and the product $g_m/I_D \cdot f_T$. The latter achieves a maximum in moderate inversion (between strong and weak inversion operation), providing a good tradeoff among gain, noise, and current consumption. In addition, analog designers based on the fundamentals of MOSFET principles for all performance use the MOSFET operating plane (see Fig. 1.15a), which illustrates the tradeoffs in performance for the selected inversion coefficient and channel length [17]. A complete version including temperature behavior of MOSFET transistor is also proposed in [21, 20], as shown in Fig. 1.15b.

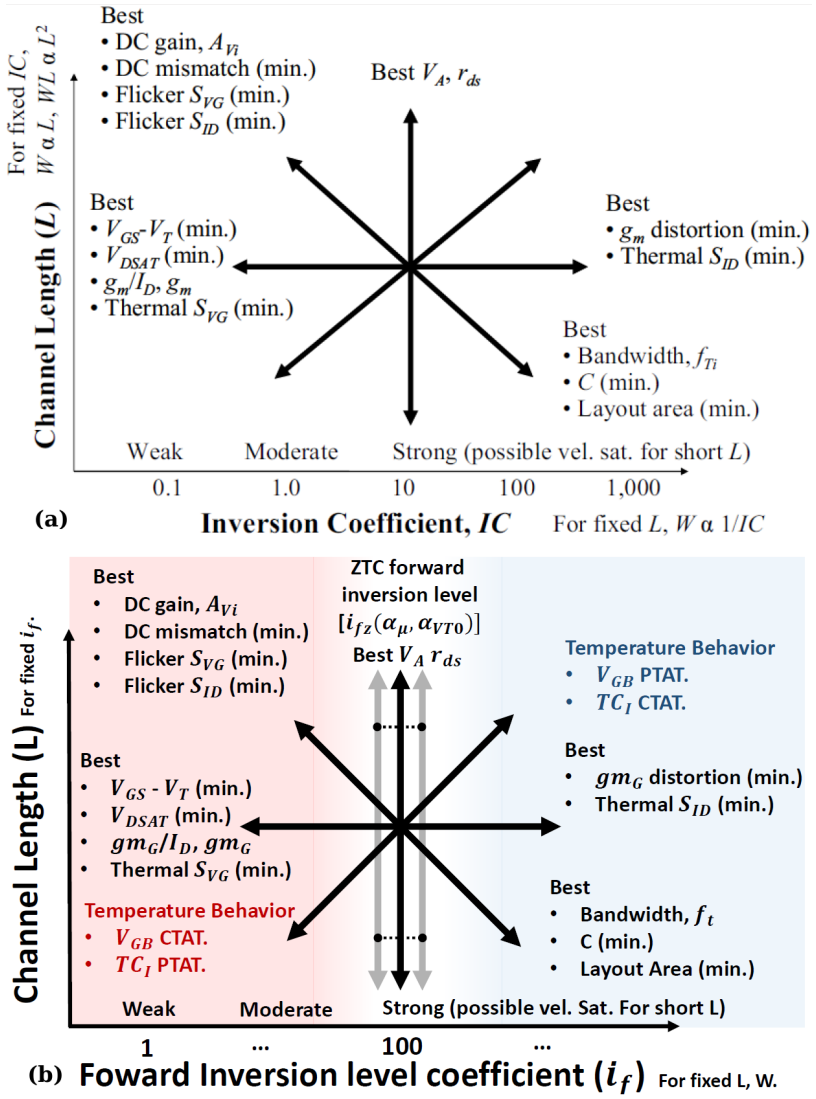


Fig. 1.15 (a) The MOSFET operating plane illustrating tradeoffs in performance for the selected inversion coefficient and channel length. Copyright John Wiley and Sons Limited [17]. (b) MOSFET operating plane translated to Unified Charge-Control Model (UCCM) [18, 19] model presented before including temperature behavior of MOSFET transistor presented in [20, 21].

Looking in this MOSFET operating plane, if it is necessary to reduce the power, more area is required (e.g., increasing the transistor length). The reduction of power consumed by the transistor is also intrinsically related to the minimum noise level produced by itself, leading to a trade-off between power, area, and noise. This trade-off, most of the time, can not only be evaluated for a standalone transistor but how is its impact on the entire circuit performance, conducting us back to the general

picture presented in Fig.1.14a. In summary, reducing power in an analog block is a topology-dependent issue and involves multi-performance trade-offs. This condition states a complex problem to be generalized, unlike seen in the digital circuit at which, roughly speaking, three constraints have to be traded-off: timing, power, and area.

The analog block power can also be reduced, making it work in very-low voltage supplies (V_{DD}). For low voltage analog designs [108, 109], some design tips are highlighted in [110], such as to use reverse-short-channel effect (RSCE) and forward body-bias techniques at the device level. At the block level, eliminating transistor stacks and taking advantage of local CMFB, CMFF, and negative transconductance generators is usually necessary to make the circuit work properly. Finally, at the functional level, revising signaling/architecture and new tuning/biasing strategies is extensively adopted to improve the whole block performance.

Even though all the techniques mentioned above make the difference in whole analog system performance, a DC bias current is always needed, setting a lower bound to the minimum power consumption. Fig. 1.14c shows the performance difference between analog (ADC) and digital (μP) blocks over time. In this illustration, a 150X difference can be found [14, 15]; one of the reasons for this gap is the biasing circuits within the analog blocks, which do not scale well for new technological nodes. Furthermore, as shown in Fig. 1.14d, analog blocks do not scale well for what concerns silicon area [16]. As has happened to the TTL family in the 70s, where the implementation of the CMOS logical family eliminated its static power consumption, it is time to either get rid of the quiescent point of analog blocks or make it more dynamic to improve the analog power consumption, taking advantage of the CMOS scaling. In section 1.4, the analog interfaces signaling and architectures are revisited, showing the new analog/RF IC design trend over the last years and its compatibility to low power/area performance.

From the IC design flow perspective, even though full custom design flow (used during the implementation of an analog block) tends to reach better circuit performance, it requires a long design time, heavy manual layout, labor-intensive and error-prone tasks. Because of that, there have been several prior efforts to automate analog layout synthesis (ALS) [111–114, 39, 115–117]. ALS automation can decrease significantly the design effort as can be seen in last publications [115, 116]; but it is still incipient when compared to the current digital flow. Even worse, ALS has as benchmark traditional analog schematics, which do not improve for new

CMOS nodes. On the other hand, digital flow is more automatic, portable, mature, and improves the time-to-market, achieving a reasonable block performance. For new technological nodes, where the layout design team has two times the designers compared to the schematic group, turning the analog/RD block more digital-like can be more attractive in design effort and performance.

Based on that, the following section presents the idea of Digital-in-Concept Design Methodologies (DCDM) for analog/RF blocks and its current state-of-the-art.

1.4 Digital-in-Concept Design Methodologies (DCDM)

The IoT requirements are challenging to be met for analog interfaces, which do not take advantage of CMOS geometrical scaling [118–120] and face specific design challenges due to the poor analog features of nanoscale transistors (as the feature size is shrunk from 0.5 to 0.022 μm node, the MOS intrinsic gain downfalls from 180 to 6 V/V [121], while the transistor f_T increases by 25X, from 16 GHz to 400 GHz) [119] and to the reduced signal swing at sub-1V power supply voltage. Such drawbacks entirely offset the potential benefits of CMOS scaling in terms of reduced parasitics and negatively impact the area, performance, energy efficiency, and especially the design effort of analog cells in advanced technology nodes. Given that, there have been almost no net power advantage [118], and no area reduction in analog cells like Operational Transconductance Amplifiers (OTAs) or bandgap references when moving from older to more recent technologies [120]. In addition, analog ICs are characterized by poor reconfigurability and portability across technology nodes compared to digital ICs and require significant time and effort in design, transistor-level optimization, simulation, full-custom layout, physical verification, and prototyping [119, 122].

Because of these limitations, there has been intense research interest in implementing traditionally analog blocks by digital-friendly and digital intensive replacements in the last years. This trend can also be observed in the number of CAS Transactions papers on related topics reported in Fig.1.16, which more than doubled in the last decade. This is defined here as **Digital-in-Concept Design Methodologies (DCDM)** trend [22].

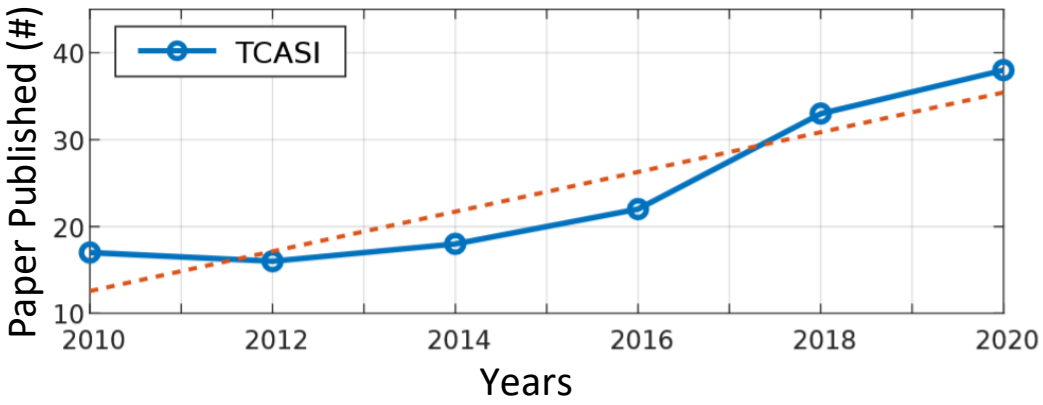


Fig. 1.16 Digital intensive analog/RF building block published in TCASI transactions over the last 10 years [22].

DCDM suggests that analog/RF circuits can take advantage of better awareness of the discrete nature of information [22] and that digital circuits can perform their functions. Following this tendency, fully digital phase-locked loops (PLLs) [123–125], synthesizable A/D converters (ADCs) based on successive approximation registers (SARs) [126–128] and on domino-logic [129], stochastic flash ADCs [130, 131] and VCO-Based ADCs [132–139] have been proposed, extensively investigated and are increasingly employed in applications. Highly digital D/A converters (DACs) [23, 140, 141, 24, 16], voltage comparators [142–144], oscillators [27], low-dropout regulators (LDOs) [145–150], buck converters[151, 152], filters [153, 154], voltage references, [26, 155, 156], temperature sensors [157] and OTAs [25, 35, 158, 159, 34, 33, 160, 161] have also been proposed. This trend can be noticed not only at block-level, but also at system-level, considering that mostly-digital RF transmitters [162–166], receivers [167, 168, 123], and biomedical front-ends [169, 170, 136, 137], have also been introduced. Indeed, it is reasonable to claim that a "digital revolution" in analog blocks is now happening, and it can be clearly observed in two common threads.

The first thread is the effort in moving information processing from the amplitude to the time domain [136, 137, 171–174], which has an intrinsic advantage in nanoscale CMOS. In more advanced CMOS nodes, timing resolution, as opposed to amplitude resolution, is steadily increasing due to the minor delays of digital gates (the fan-out-of-4 (FO4) delay of an inverter has decreased by from 140ps (0.5μm) to 6ps (22nm node), i.e., by 23X [119]).

The second thread encompasses the research activities developed in the last years to extend digital automated design techniques to analog and RF systems. Although promising semi-automatic analog design techniques like procedure-based layout generation and optimization-based layout synthesis have been proposed in the last years [175, 115, 116], the synthesis-friendly analog circuits that use the existing digital flow tools for designing indicate to be the most attractive ones.

These two threads are closely related to each other - since analog circuits based on time-domain information processing are inherently more suitable to automated synthesis, and the functional/logical decomposition and abstraction required for automatic design naturally lead to time-domain, algorithmic processing. Both converge towards the implementation of the functions of analog circuits by *true digital circuits*, in which information is internally processed in the form of two-level digital signals (i.e., *without* using digital gates as analog amplifying stages, as in [176]). As illustrated in Fig. 1.17a, this new circuit design approach, possibly preceded or not by a minimal, non-critical, passive network that can grasp relevant information from any finite-amplitude, band-limited input signals (voltages and/or currents), can generate the desired band-limited output voltages/currents at a pre-fixed degree of accuracy. Note that, even though passives are needed in some cases, depending on the applications, such elements can be implemented by standard cells like using pseudo-resistors (as used in chapter 2).

In [22], Fig.1.17b plots power versus area for ADCs, DACs, OTAs, voltage reference and oscillators [23–27]. Such figure indicates that implementation of the recent analog blocks by DCDM or digital-based approach leads to low power and small area integrated circuits, matching with the IoT nodes needs as mentioned previously in the section 1.3. This thesis investigates this fact, proving that conceivably this is the right path for IoT analog interfaces.

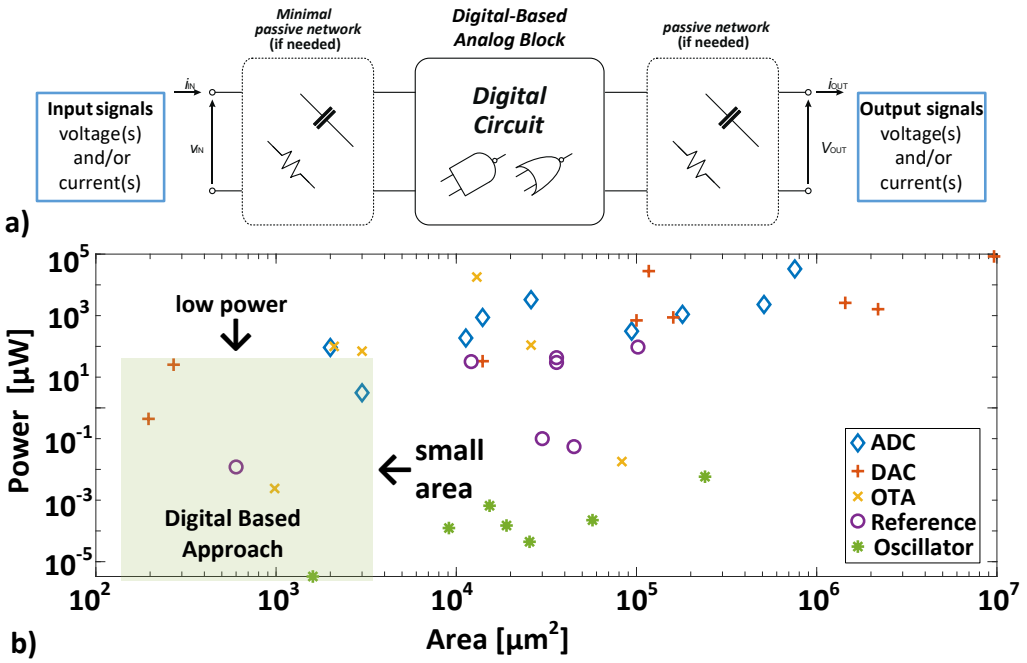


Fig. 1.17 a) Block diagram of digital-based analog block [22] b) Power vs Area for for ADCs [23], DACs [24], OTAs [25], voltage reference [26] and oscillators [27].

1.5 Thesis Organization

While most of the previously cited solutions address the challenges of analog interfaces by more "digital friendly" analog cells based on traditional design concepts [14], the opportunity to implement analog functions with true digital circuits, which fully take advantage of CMOS scaling and of the benefits of a digital design flow, will be explicitly covered in this thesis, demonstrating itself as promising analog design alternative for IoT nodes. Concomitantly, this thesis aims at advancing on low power/area analog design strategies targeting the current IoT bottleneck on the edge devices: power consumption. **Digital-in-Concept Design Methodologies (DCDM)** are herein contextualized and used to design two digital-based OTAs and one digital-based biosignal amplifier. During the whole DCDM investigation, this thesis produced interesting contributions, which are listed below:

- an ultra-low-voltage/power fully-integrated Digital-Based Operational Transconductance Amplifier (DB-OTA) is demonstrated on silicon in 180 nm CMOS for the first time. Before that, it had been demonstrated using off-the-shelf components. To the best of this thesis author's knowledge, the power achieved

by this demonstration is the lowest reported to date in an OTA, reaching the figures of merit that are the best in sub-500 mV OTAs registered so far;

- then, as a second contribution, a new passive-less fully-digital operational transconductance amplifier (DIGOTA) for energy- and area-constrained systems is proposed and silicon-proven. What differentiates the new DIGOTA from the previous one is that the latter has passive-less self-oscillating common-mode compensation, making the circuit less noisy and more compatible with the digital flow;
- using the second OTA version, i.e., the DIGOTA, a power-efficient ultra-low voltage and ultra-low area fully-differential, digital-based Operational Transconductance Amplifier (OTA), suitable for microscale biosensing applications (BioDIGOTA), is proposed and silicon-proven.

The rest of the thesis is organized as follows. The next chapter (i.e., chapter 2) presents a Digital-Based OTA implementation for ultra-low-power/voltage/area applications, followed by a passive-less version with better robustness, area, and signal-to-noise performance in chapter 3. In the chapter 4, the operation principle and the silicon characterization of a power-efficient ultra-low voltage and ultra-low area fully-differential, digital-based Operational Transconductance Amplifier (OTA), suitable for microscale biosensing applications (BioDIGOTA), is discussed. The last chapter draws the conclusion and possible future works to further improve the circuit's performance.

Chapter 2

Digital-Based OTA

This chapter shows a silicon demonstration of an embryonic Digital-Based OTA (DB-OTA) published in 2013 [159], targeting Ultra Low Power (ULP) and Ultra Low Power (ULP) performance. In the section 2.1, a brief review of the current state-of-the-art for ULP and ULV OTAs is presented, categorizing the OTA topologies in classes and comparing their performance. In the section 2.2, the DB-OTA circuit analysis and design are detailed, followed by its layout description, simulation and measurement results in the sections 2.3, 2.4, and 2.5, respectively.

2.1 Previous art of ULV/ULP OTA Design

In general, ULV OTAs can be classified as gate-driven, bulk-driven, inverter-based, VCO-based, and digital-based topologies.

In [28][29] gate-driven MOS transistors working in subthreshold regime are exploited (Fig. 2.1a). The minimum power supply and Common-Mode Input Range (CMIR) are limited by $V_{DD} = 3V_{sat} \approx 300mV$ and $V_{CM} = V_{DD} - 2V_{sat} - V_{TH}$, respectively, being V_{sat} the minimum drain-source voltage required to operate a MOS device in saturation and V_{TH} is the threshold voltage. Typically the V_{sat} is deemed to be around $3 \sim 4 \cdot KT/q$ in subthreshold regime [108].

On the other hand, in [30] (see Fig. 2.1b), bulk-driven input devices are exploited to mitigate the CMIR limitation at the cost of reduced efficiency due to the lower values of the bulk transconductance g_{mb} compared to the gate one g_{mg}. There are

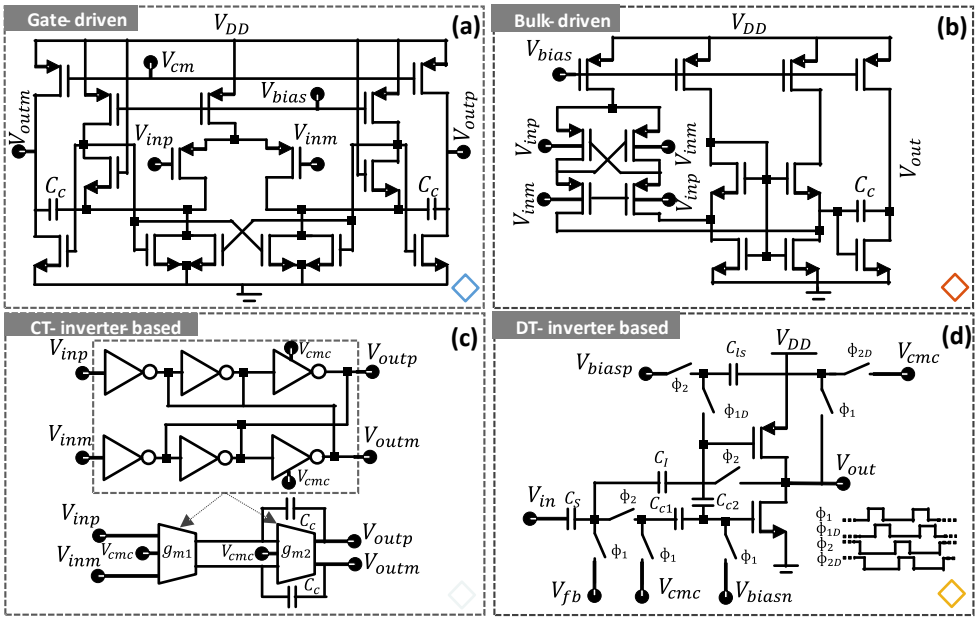


Fig. 2.1 a) Gate-driven [28, 29], b) Bulk-driven [30] c,d) Inverter-based [31, 32].

many others bulk-driven OTAs proposed in the literature [177–180], especially after [181] has been published. Inverter-based amplifiers [31, 32, 182, 160] (Fig. 2.1c,d) have been proposed to achieve a large equivalent transconductance ($g_{m_{TOTAL}} = g_{m_{PMOS}} + g_{m_{NMOS}}$) under low V_{DD} and voltage headroom. However, they suffer of limited intrinsic gain and common-mode rejection.

Recently, an alternative approach that aims to implement analog functions by digital means (as illustrated in Fig. 2.1a,b) has been proposed for OTA design [183, 159, 33, 35, 161]. Both OTAs in Fig. 2.1a,b, VCO-based OTA [183] and a digital-based [159] OTA, exploit time-domain information processing and prove to be very good candidates for efficient ULV operation. Figs. 2.3 a, b and c compare V_{DD} versus FOM_S (as defined in Eq. (2.1)), C_L versus power and area versus power between all schematics depicted in Fig. 2.1 and 2.2. Such figure shows that the digital-based OTA consumes less area and power compared among the OTAs considered in the comparison. The following section 2.2 presents the circuit analysis and design of a Digital-Based OTA (DB-OTA) and its silicon measurements.

$$FOM_S = 100\frac{GBWC_L}{I_{DD}} \tag{2.1}$$

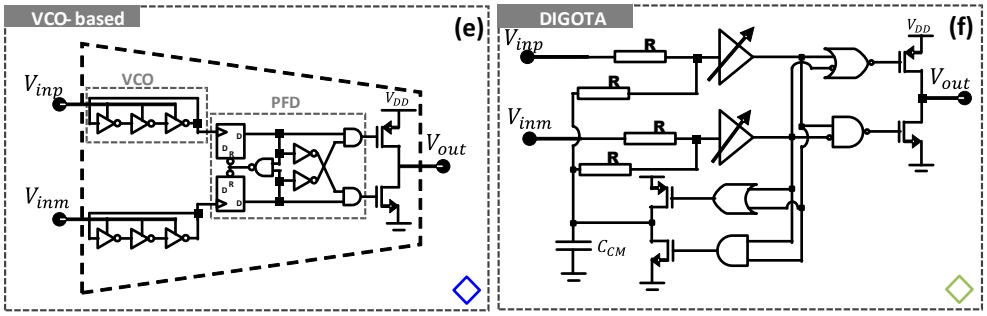


Fig. 2.2 a) VCO-based [33, 34] b) Digital-based [35] topologies.

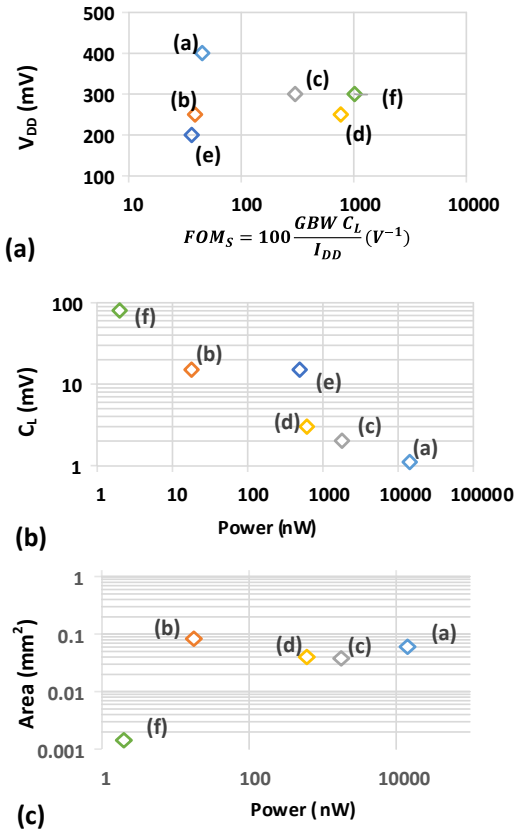


Fig. 2.3 ULV OTA state-of-art comparison plots: V_{DD} (mV) versus $FOM_S = 100\frac{GBWC_L}{I_{DD}}$ (V^{-1}), C_L (pF) versus Power (nW) and Area (mm^2) versus Power (nW). (a) Gate-driven, (b) Bulk-driven, (c)(d) Inverter-based from the Fig. 2.1, (e) VCO-based and (f) Digital-based from the Fig. 2.2.

2.2 Circuit Analysis and Design

2.2.1 Qualitative Circuit Analysis

In [159], the possibility to translate into digital the operation of a MOS differential pair has been explored. To do this emulation, understanding how the common-mode signal is tracked and attenuated in traditional architecture like the MOS differential pair [184], as shown in Fig. 2.4, is very helpful.

In a standard NMOS differential pair, the Common-Mode (CM) signal is tracked by the voltage V_S of the common-source node S, and is subtracted from the external inputs in the gate-source voltages of the input devices, so that the control voltages of the input devices are CM-voltage independent and their drain currents are proportional to the differential mode input v_d [185]. In other words, V_S node continuously-time follows the $V_{CM} = \frac{V_{IN+}+V_{IN-}}{2}$, while remains static when $v_d = V_{IN+} - V_{IN-} \neq 0$.

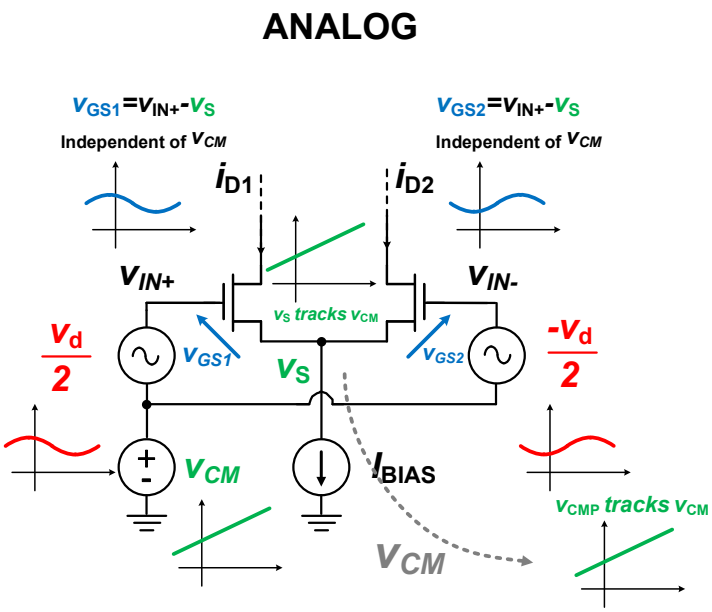


Fig. 2.4 Traditional gate-driven NMOS differential pair.

In [159], it was demonstrated that a similar behavior can be obtained from two digital buffers after adding a CM signal tracker and summing network (i.e., to mimic similar V_S behavior of a traditional differential pair).

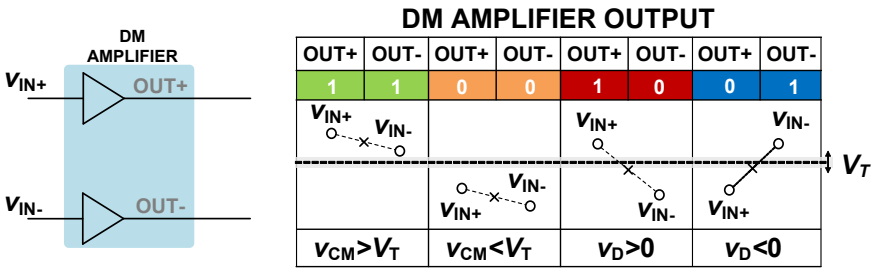


Fig. 2.5 Differential Mode Amplifier.

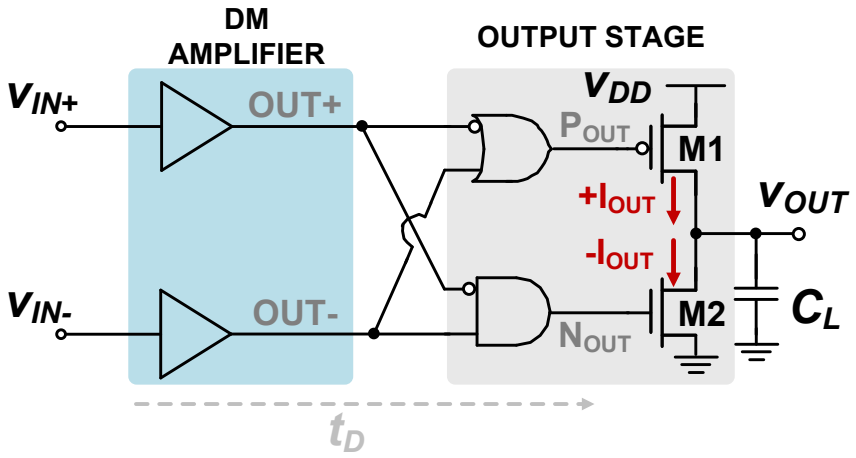


Fig. 2.6 Differential Mode Amplifier and Output stage.

To sense the analog input signal, a Differential-Mode (DM) Amplifer (see Fig. 2.5) is used. The DM is formed by two digital buffers and the level of the input voltages w.r.t. the buffers voltage tripping points (V_{T}) is analyzed through their four possible logical outputs: $(OUT_+, OUT_-) = (0,0),(1,1),(1,0),(0,1)$.

As detailed in Fig. 2.5, whenever $(OUT_+, OUT_-) = (0,1),(1,0)$, it follows that $v_{\mathrm{d}} > 0$ or $v_{\mathrm{d}} < 0$ respectively, and the logic values of the buffers reflects the sign of th DM signal. From the table within Fig. 2.5, it can be seen that this happens when $|v_{\mathrm{d}}/2| > |v_{\mathrm{CM}} - V_{\mathrm{T}}|$. This is the moment that it can be claimed that the CM signal is negligible and the output can be driven according to the DM signal. To do that, the output stage is added as shown in Fig. 2.6. The latter is activated and V_{out} is increased/decreased depending on v_{d}, i.e., according to the codes $(OUT_+, OUT_-) = (0,1),(1,0)$. Otherwise, when $(OUT_+, OUT_-) = (0,0),(1,1)$, the output node is configured to be in high-impedance configuration. The Boolean expressions (2.2) and (2.3) show the logic to implement that.

$$\mathrm{P_{OUT}} = \overline{\mathrm{OUT_+}\,\overline{\mathrm{OUT_-}}} = \overline{\mathrm{OUT_+}} + \mathrm{OUT_-} \tag{2.2}$$

$$\mathrm{N_{OUT}} = \mathrm{OUT_-}\,\overline{\mathrm{OUT_+}} = \overline{\mathrm{OUT_-} + \mathrm{OUT_+}} \tag{2.3}$$

Look that from buffer input to the gate voltages of three-state buffer it is needed to wait a delay of t_D to updade V_out.

For $(OUT_+, OUT_-) = (0,0),(1,1)$, i.e., $|v_\mathrm{d}/2| < |v_\mathrm{CM} - V_\mathrm{T}|$, an auxiliary circuit is needed to track and subtract the common mode from the buffer inputs. Using (OUT_+, OUT_-) as common mode sensing, a CM Extractor is deployed on the loop along with a summing network to correct the input CM signal, as shown in Fig. 2.7. In this case, the logic implemented to do that is given by

$$\mathrm{P_{CMP}} = \mathrm{OUT_+} + \mathrm{OUT_-} \tag{2.4}$$

$$\mathrm{N_{CMP}} = \mathrm{OUT_+}\,\mathrm{OUT_-} \tag{2.5}$$

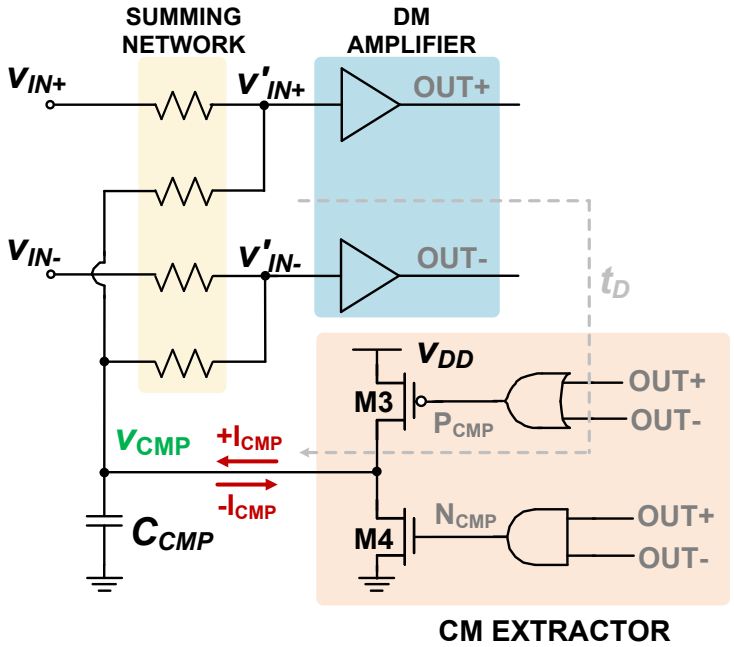


Fig. 2.7 Differential Mode Amplifier and Common Mode Extractor.

The CM Extractor includes its own logic, from Eqs. (2.4) and (2.5), a three state buffer, and a common mode capacitor C_{CM}. Concerning the summing network, a voltage divider made by resistors is adopted. Similar delay of t_D is needed to update V_{CMP} from buffer inputs.

Fig.2.8 depicts the first version of DB-OTA proposed by Crovetti in 2013 [159]. In summary, DB-OTA has four parts: summing network, DM Amplifier, CM Extractor and Output stage. The DM signal flows from summing network, passing through the DM Amplifier, until the output stage, while CM signal flows from summing network, passing through the DM Amplifier, until the CM Extractor.

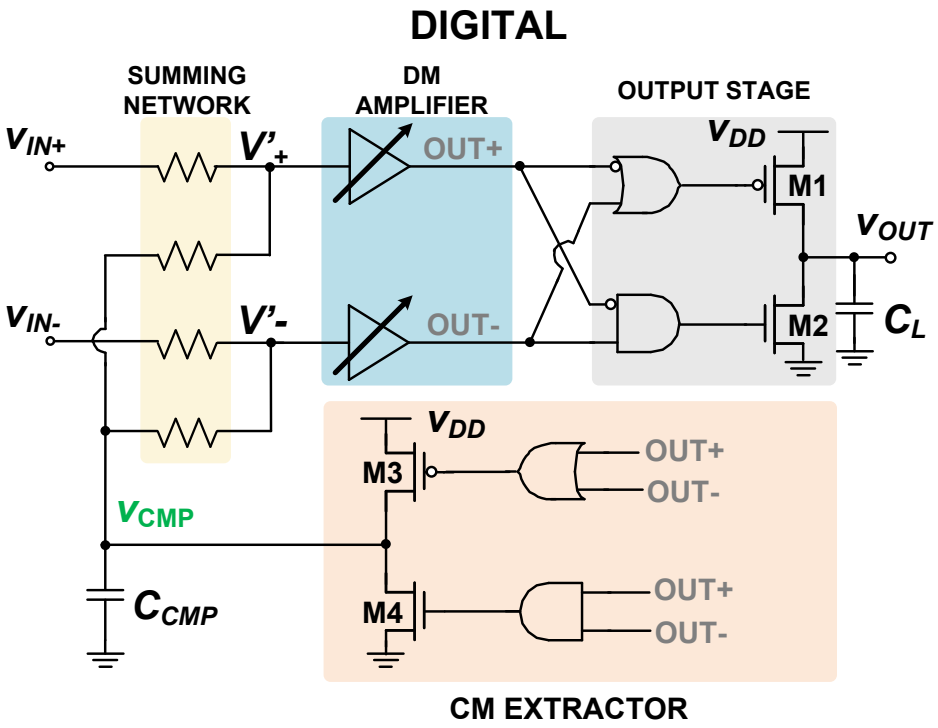


Fig. 2.8 Digital-Based Operational Trasnconductance Amplifier.

2.2.2 Quantitative Circuit Analysis

To analyze the DB-OTA operation and its performance, it is crucial to look into its internal waveforms. For equal resistance values within summing network and using the superposition theorem of linear circuits, the voltage seen at each buffer input is given by

$$V'_{IN+}(t) = \frac{R}{R+R}(v_{CMP}(t) + V_{IN+}(t)) = \frac{v_{CMP}(t) + V_{IN+}(t)}{2} \tag{2.6}$$

$$V'_{IN-}(t) = \frac{R}{R+R}(v_{CMP}(t) + V_{IN-}(t)) = \frac{v_{CMP}(t) + V_{IN-}(t)}{2} \tag{2.7}$$

where R is the each resistance within the summing network, $v_{CMP}(t)$ is voltage node that is used to track CM mode input signal (similar role done by V_S) and, $V'_{IN+(-)}(t)$ are the voltages at buffers input. $v_{CMP}(t)$ can be estimated assuming that the three-state buffer in the *CM extractor* pushes and pulls charge by ideal current sources, giving

$$\frac{dv_{CMP}(t)}{dt} = \pm\frac{I_{CMP}}{C_{CMP}} \quad \therefore \quad v_{CMP}(t) = \pm\frac{I_{CMP}}{C_{CMP}}t \tag{2.8}$$

Substituting (2.8) in (2.6) and (2.7), then

$$V'_{IN+(-)}(t) = \frac{1}{2}\left(\pm\frac{I_{CMP}}{C_{CMP}}t + V_{IN+(-)}(t)\right) \tag{2.9}$$

If a fixed DC CM signal is applied, i.e., $V_{IN+}(t) = V_{IN-}(t)$, then, due to the feedback logic inside of *CM extractor*, $V'_{IN+(-)}(t)$ oscillates around the buffer trip points V_T with a period

$$T_0 = \frac{1}{f_0} = 4t_{\mathrm{D}} \tag{2.10}$$

where f_0 is the internal natural oscillation frequency of the DB-OTA.

Fig. 2.9a shows the DB-OTA state transition graph under a pure CM signal stimulus, i.e., $v_d = 0$. Note that the circuit does not have a static bias point; Instead, it tracks the CM signal, oscillating around the V_T of the buffer. In contrast, when the circuit is differential input stimulated, it means that $|v_{\mathrm{d}}/2| < |v_{\mathrm{CM}} - V_{\mathrm{T}}|$ holds. This mechanism can be thought of as a kind of dynamic bias point. This eliminates the need of a constant bias current, hence lowering the total power consumption. Fig. 2.9b draws the waveforms of the main node voltages within the DB-OTA, when modeled by a first order approach.

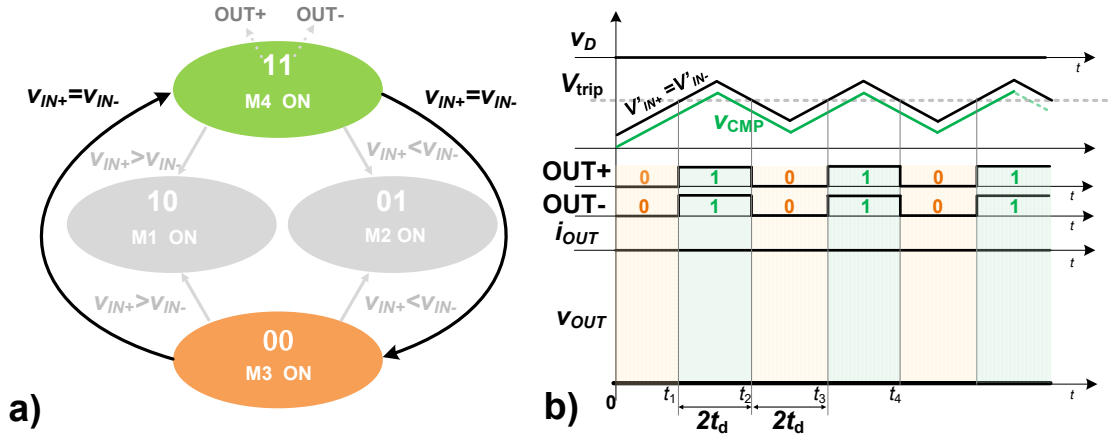


Fig. 2.9 a) DB-OTA state transition graph under only CM mode signal stimulus ($v_d = 0$) b) time-domain DB-OTA waveforms

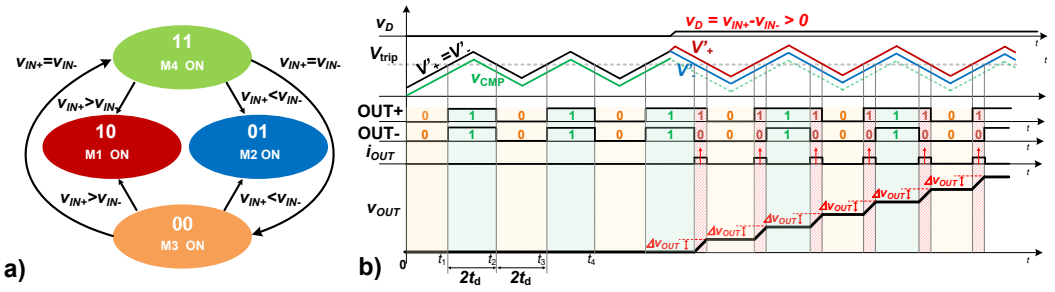


Fig. 2.10 a) Complete DB-OTA state transition graph b) time-domain DB-OTA waveforms

When $v_d(t) = V_{IN+}(t) - V_{IN-}(t) \neq 0$, two more states appear in DB-OTA state transition graph as shown in Fig. 2.10a. From Eq. (2.9), for $V'_{IN+(-)}(t) = V_T$ which makes $V'_{IN+}(t) - V'_{IN-}(t) = 0$, the $\Delta t(t)$ due to v_d can be estimated by

$$0 = \frac{I_{CMP}}{C_{CMP}} \Delta t(t) - v_d(t) \quad \therefore \quad \Delta t(t) = \frac{C_{CMP}}{I_{CMP}} v_d(t) \tag{2.11}$$

Applying the Laplace transform in Eq. (2.11), then

$$\Delta T(s) = \frac{C_{CMP}}{I_{CMP}} \cdot V_d(s) \tag{2.12}$$

Since zero crossings occur every half period, the voltage-to-time conversion takes place every $T_0/2$ and leads to the generation of a signed time difference $\Delta t(t)$

given by Eq. (2.11), and its width is proportional to v_d evaluated at $kT_0/2$. Hence, the internal DB-OTA loop acts as a self-oscillating threshold sampler [186] with a natural sampling frequency of $2f_0$. Based on that, the three-state buffer of the *output stage* receives such pulses $\Delta t(t)$ every pushing/pulling current in its output node. Assuming that time pulses $\Delta t(t)$ take place exactly every $T_0/2$, the output stage current $i_{OUT}(t)$ driving C_L can be written as

$$i_{OUT}(t) = \sum_{k=0}^{+\infty} I_{OUT}\Delta t(t)\delta\left(t - \frac{k}{2f_0}\right) = \sum_{k=0}^{+\infty} I_{OUT}\Delta t(t)\delta\left(t - k2t_D\right) \quad (2.13)$$

The Laplace of the Eq. (2.13) for frequencies much lower than f_0 gives

$$I_{OUT}(s) = \frac{I_{OUT}}{2t_D}\Delta T(s) = \frac{I_{OUT}}{2t_D}\frac{C_{CMP}}{2I_{CMP}}V_d(s) \quad (2.14)$$

Since

$$V_{OUT}(s) = \frac{r_{OUT}}{sr_{OUT}C_L + 1}I_{OUT}(s) \quad (2.15)$$

the DB-OTA transfer function can be estimated as

$$A_D(s) = \frac{V_{OUT}(s)}{V_d(s)} = \frac{1}{2}\cdot\frac{I_{OUT}}{2t_D}\frac{C_{CMP}}{I_{CMP}}\frac{r_{OUT}}{(sr_{OUT}C_L + 1)} \quad (2.16)$$

From Eq. (2.16), the low frequency DC gain in dB of the DB-OTA as well as its unit gain bandwidth (GBW) can be calculated as shown by Eq. (2.17) and Eq. (2.18), respectively.

$$A_{d,dB} = 20\log_{10}\left(\frac{1}{2}\cdot\frac{I_{OUT}r_{OUT}}{2t_D}\frac{C_{CMP}}{I_{CMP}}\right) = -6\text{dB} + 20\log_{10}\left(\frac{I_{OUT}r_{OUT}}{2t_D}\frac{C_{CMP}}{I_{CMP}}\right) \quad (2.17)$$

and

$$f_{GBW} = \frac{f_0}{2\cdot\pi}\cdot\frac{I_{OUT}}{I_{CMP}}\frac{C_{CMP}}{C_L} \quad (2.18)$$

once its dominant pole is given by

$$s_p = -\frac{1}{r_{OUT}C_{\mathrm{L}}} \tag{2.19}$$

The DB-OTA power consumption is the sum of the power consumption of the active power P_{gates} of the logic gates involved in the self-oscillating loop (i.e., *DM Amplifier* and *CM Extractor*), the contribution P_{out} of the output stage, and the overall leakage power P_{lkg}

$$P_{DB-OTA} = P_{gates} + P_{out} + P_{lkg} \approx P_{gates} + P_{out} \tag{2.20}$$

In Eq. (2.20), P_{gates} is given by the dynamic power of the internal logic gates with overall switched capacitance C_{int} operating at frequency $2/T_0$, which can be expressed as

$$P_{gates} = \frac{2}{T_0}C_{int}V_{DD}^2 \tag{2.21}$$

and P_{out} is the power needed to (dis)charge the load capacitance C_L, which can be expressed as

$$P_{out} = f_S C_L V_{OUT}^2 \tag{2.22}$$

where a sinewave output with peak-to-peak amplitude V_{OUT} at frequency f_S is assumed.

From the above quantitative analysis, some points are worthy to be highlighted. Eq. (2.16) shows that the DB-OTA behaves as a first-order system with negative real pole at $1/(2\pi r_{OUT}C_L)$ consuming a total power of

$$P_{DB-OTA} \approx (2C_{int} + \alpha C_L) f_0 V_{DD}^2 \tag{2.23}$$

under rail-to-rail input signal, where $\alpha = \frac{f_S}{f_0}$. In the case that $f_S = f_{GBW}$ from Eq. (2.18) and consequently

$$\alpha = \frac{I_{OUT} C_{CMP}}{2\pi I_{CMP} C_L} \tag{2.24}$$

then

$$P_{DB-OTA,GBW} \approx C_{DB-OTA,GBW} f_0 V_{DD}^2 \tag{2.25}$$

where $C_{DB-OTA,GBW} = 2C_{int} + \frac{I_{OUT}}{2\pi I_{CMP}} C_{CMP}$. $C_{DB-OTA,GBW}$ is here defined as DB-OTA equivalent capacitance. For the presented DB-OTA, $C_{DB-OTA,GBW} f_0 V_{DD}^2$ power consumption demonstrates that V_{DD} can be used as a design knob to reduce the power consumption as typically adopted in DVS low power digital circuit [99]. In the next section 2.2.3, low V_{DD} is chosen to reduce the total power consumption targeting low power IoT applications.

Another point is that, based on Eq. (2.16), DB-OTA should have a phase margin (PM) of 90^o in unit gain configuration. However, as it will be shown in section 2.4, simulations results demonstrate PM between 57 and 76 depending on C_L, indicating a relevant non-dominant pole for low values of C_L. The non-dominant pole effect on the PM can be interpreted by the relevant parasitic output capacitance seen from the DM amplifier's total equivalent input capacitor and high values of resistance from the pseudo-resistor working in weak inversion. Furthermore, for low frequencies, DB-OTA has an intrinsic gain loss of -6 dB as shown in (2.17), due to the voltage divider of the summing network as seen in (2.6) and (2.7). Indeed, the summing network of the DB-OTA is the root of the above limitations, and it will be replaced by a different input stage in the chapter 3, providing a new digital-based OTA.

2.2.3 Circuit Design

The proposed ULV DB-OTA has been designed in 180nm following digital design criteria. CMOS static logic is adopted for most the gates in Fig.2.8. Moreover, as usual in ULP digital design, the power supply voltage is set to the Minimum Energy Point (MEP) [187], which turns out to be about $V_{\mathrm{DD}} = 300\mathrm{mV}$ for the target technology and switching activity (f_0).

The strength of the output stage is set by considering the maximum capacitive load (80pF in the proposed design) and slew rate requirements, taking into account

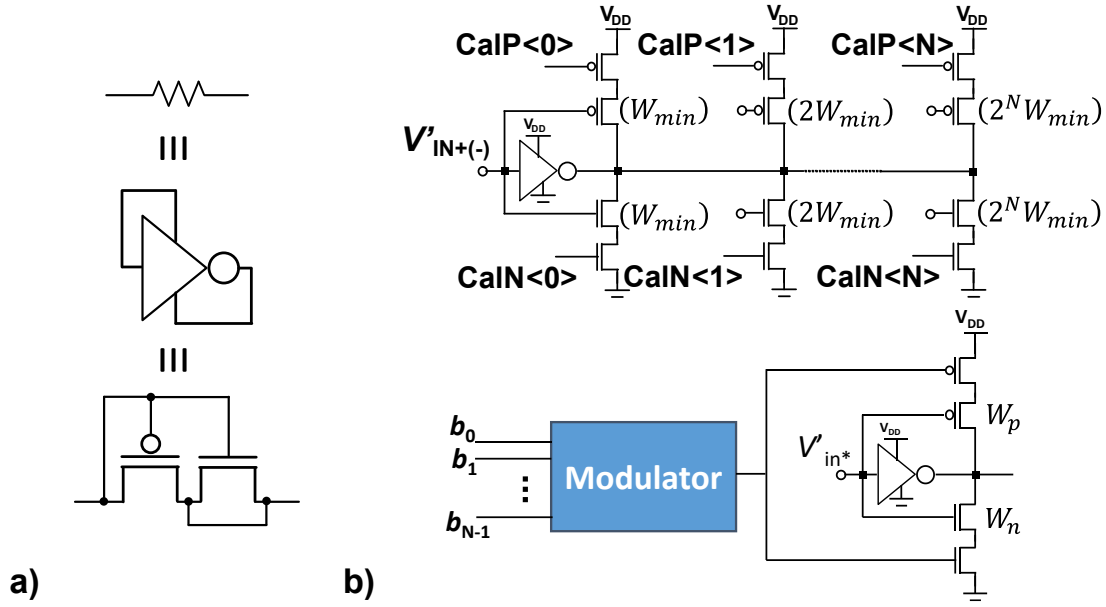


Fig. 2.11 a) inverter-based pseudo-resistor b) Static digital calibration (SDC) and dynamic digital calibration (DDC).

also that a minimum capacitive load (10pF in the proposed design) is needed in the DB-OTA for low-distortion analog signal reconstruction. The strength of the other gates is consequently designed as cascaded drivers to guarantee digital signal integrity. Minimum-size devices have been used in the CM extractor stage, and the capacitance C_{CMP} has been set to reduce Total Harmonic Distortion (THD), supported by the analysis of the simulation results.

Two parts of the circuit deserve a special care due to their analog function, i.e. the summing network and the first inverters of the DM amplifier.

The summing network has been implemented using inverter-based pseudo-resistors as voltage dividers. Large area ($\approx 270\mu m^2$) has been adopted in PMOS devices in Fig. 2.11a, to achieve a good matching leveraging Pelgrom's law [188].

For what concerns the DM amplifier in Fig. 2.8, mismatch in the buffers V_{T} decides the DB-OTA input offset voltage and it has been mitigated by the calibration network as the ones shown in Fig. 2.11b. Eq. (2.26) shows the voltage offset of DB-OTA.

$$V_{\mathrm{OFF}} \approx \Delta V_{\mathrm{T}} \tag{2.26}$$

where

$$\Delta V_{\mathrm{T}} = V_{\mathrm{T1}} - V_{\mathrm{T2}} \tag{2.27}$$

is the difference of the trip points V_{T1} and V_{T2} of the first inverters of each buffer, both expressed in terms of technology and geometrical parameters in subthreshold regime as [189]:

$$V_{\mathrm{T}} = \frac{\frac{\kappa T}{q}\log\left(\frac{I_{\mathrm{D0_P}}\left(\frac{W}{L}\right)_{\mathrm{P}}}{I_{\mathrm{D0_N}}\left(\frac{W}{L}\right)_{\mathrm{N}}}\right) + \frac{V_{\mathrm{DD}}}{n_{\mathrm{P}}}}{\frac{1}{n_{\mathrm{P}}} + \frac{1}{n_{\mathrm{N}}}}, \tag{2.28}$$

$I_{\mathrm{D0_{N(P)}}}$ is the zero-v_{GS} drain current of nMOS (pMOS) in weak inversion and it is process parameter dependent, $n_{N(P)}$ is the subthreshold slope factor of the nMOS (pMOS) device. All the other symbols have their usual meaning [189].

For minimum size devices, the offset predicted by (2.26) can be easily large enough to saturate the DB-OTA, thus fully impairing the DB-OTA operation, and needs to be compensated. For this purpose, the dependence of the trip points of a CMOS inverter on the aspect ratios of the pull-up and pull-down devices, given by Eq. (2.28), can be used for calibration.

In this implementation, two methods have been adopted in the DB-OTA calibration: Static Digital Calibration (SDC) and Dynamic Digital Calibration (DDC).

The SDC (see Fig. 2.11b top) procedure has been applied in [35], which has made the calibration possible tuning the effective aspect ratio of either the pull-up or the pull-down branch by enabling/disabling binary weighted $2^i W_{min}$ transistors in parallel to first inverter of the DM amplifier, based on a 8-bit calibration code $b_{i,n}$ with $i = 0...N-1$. This calibration procedure, however, is not compatible with a pure digital flow and requires extra area and analog design effort.

Given these limitations, all-Digital DDC techniques based on Digital Pulse Width Modulation (DPWM) and Dyadic Digital Pulse Modulation (DDPM) have been explored in [190] and [36], respectively.A DDC network, which consists of only one enabled-inverter driven by the input signals ($V_{in-(+)}$) and also connected in parallel to the first stage of each branch in the DM amplifier, is depicted in Fig. 2.11b bottom. A modulator applying a particular modulation technique is then connected to the DDC network to modulate the input signal adjusting the DM amplifier V_T.

The calibration network operation is described next. The pull-up (pull-down) network of the calibration inverter can be connected to the supply (to ground) through

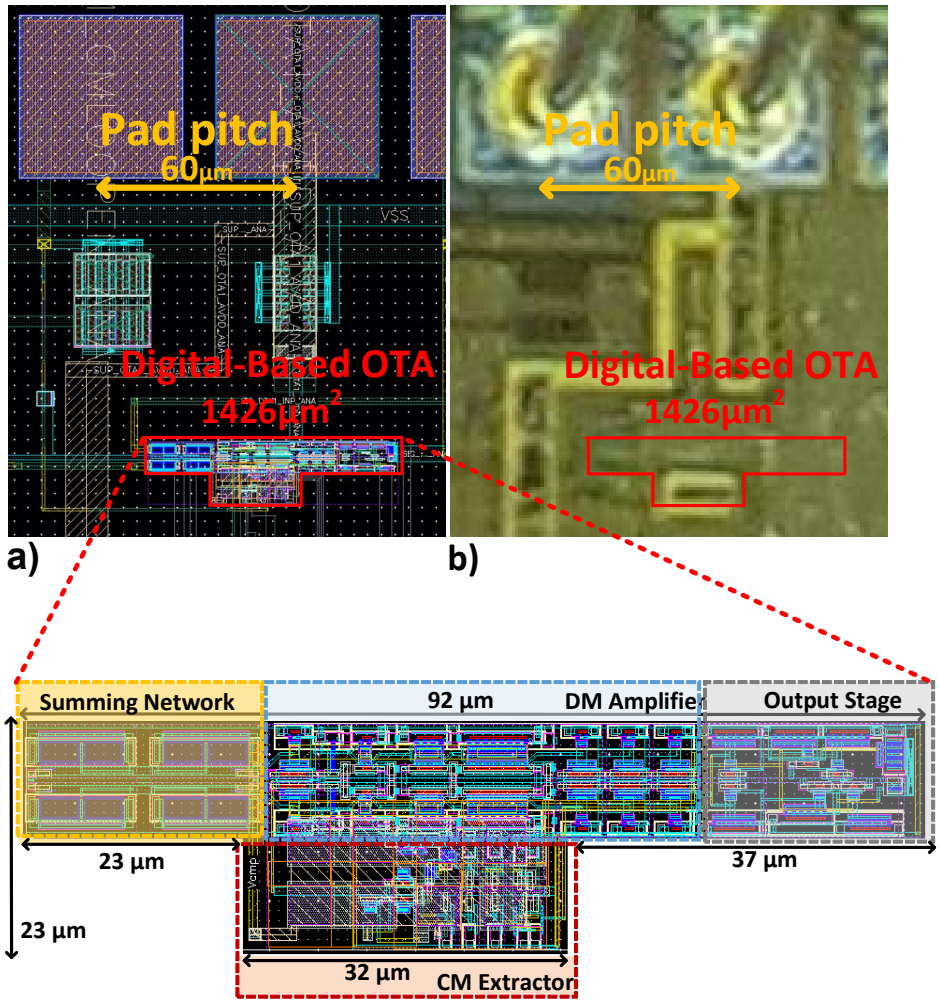


Fig. 2.12 a) DB-OTA layout. Total area of 1,426 μm^2 b) Micrograph of the 180-nm test-chip.

a pMOS (nMOS) power gating switch. When the pMOS (nMOS) gating switch is on, the pMOS (nMOS) of the calibration inverter, with width W_n (W_p) is enabled and connected in parallel to the nMOS (pMOS) device in the first stage of the DM amplifier, thus effectively increasing its width and significantly reducing (increasing) its trip point according to Eq. (2.28).

When the gating switches are periodically operated with a certain frequency larger than the DB-OTA GBW, it is observed that periodically enabling the gating switches has the same net effect on the trip points of the DM amplifier gates as increasing the width of the DM amplifier devices by a fraction DW_n (DW_p) of the

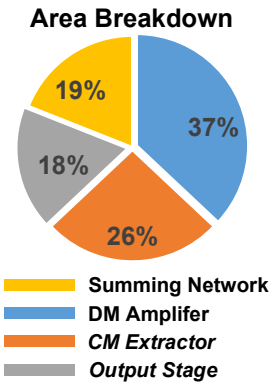


Fig. 2.13 DB-OTA Area Breakdown not containing the DDC; only SDC.

calibration inverter width W_n (W_p), being $D = \frac{T_{EN}}{T}$ the effective enabling duty cycle, where T_{EN} is the overall time the calibration inverter is enabled over the period T. This approach is adopted for dynamic offset calibration of the OTA, considering both DPWM and DDPM streams as gating signals for the calibration inverter. Results for all calibration strategies will be shown in section 2.4.

2.3 Layout

The DB-OTA has been laid out in 180nm CMOS to match the delays of the non-inverting and inverting signal paths. Logic gates from the standard cell library have been placed, reducing the layout design effort. The layout of the circuit, including the calibration network, occupies just 1,426 μm^2, and it is shown in Fig. 2.12a. Its area breakdown is depicted in Fig. 2.13. 37% of the area is occupied by the DM Amplifier which contains the SDC network.

The ULV DB-OTA operation and performance have been evaluated by post-layout simulations [35, 36] and tested by measurements [191]. Fig 2.12b shows a microphotograph of the 180nm test-chip. In the sections 2.4 and 2.5, all simulations and measurements results are plotted and compared with ULV OTAs presented in recent literature, respectively.

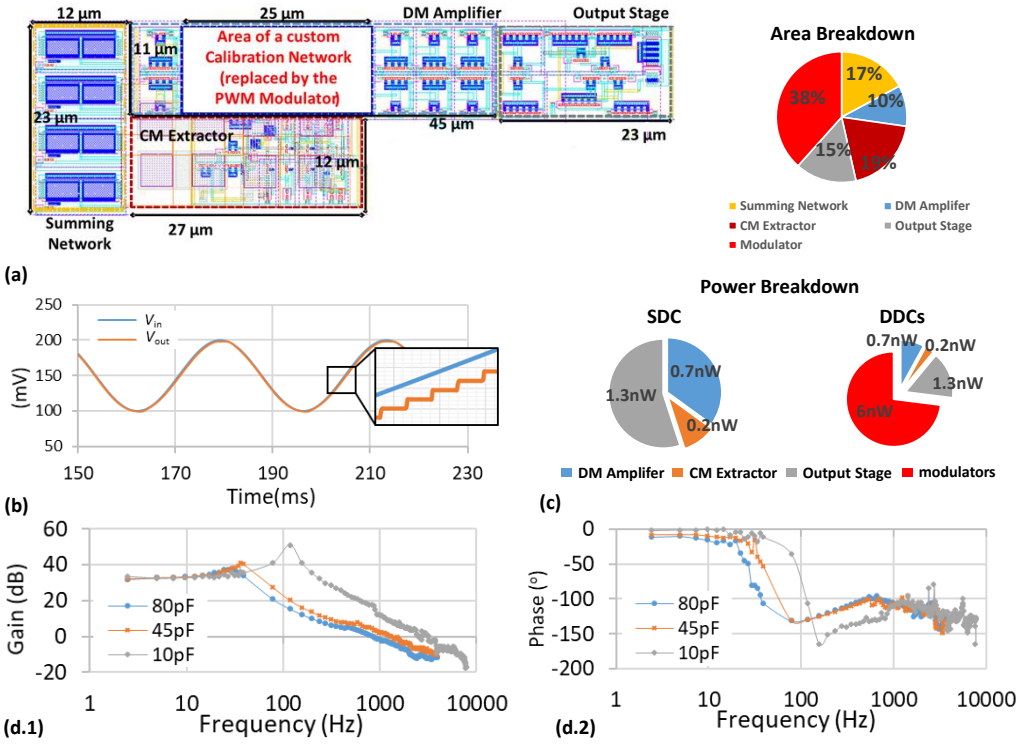


Fig. 2.14 [SIMULATION]a) DB-OTA layout and Area breakdown containing DDC b) V_{in} and V_{out} at 30 Hz frequency, 50 mV peak amplitude and $C_{out} = 80\,pF$ c) Power breakdown d) ULV DB-OTA frequency response [36].

2.4 Simulations Results

The ULV DB-OTA input and output waveforms with a sine wave input at 30 Hz frequency, 50mV peak amplitude and $C_L = 80\,pF$ are reported in Fig. 2.14b for $V_{DD} = 300mV$ and in voltage follower configuration. In this configuration, a THD less than 2% and 2 nW power consumption are achieved. Also in this picture, a zoom in the output voltage waveform reveals the step-wise changes in v_{out}; the intrinsic digital characteristic of the DB-OTA (see Fig. 2.10b). The ULV DB-OTA frequency response, calculated through Fast Fourier Transform (FFT) analysis of transient simulations, as done in [35], is reported in Figure 2.14d for $C_L = 10, 45, 80$ pF. Note that no quiescent bias is available, impairing any AC analysis. According to that, DB-OTA shows 35dB DC gain and $0.85, 1.3$ and $2.48\,kHz$ Gain Bandwidth Product (GBW) with phase margins $76°, 68.5°$ and $57°$, respectively.

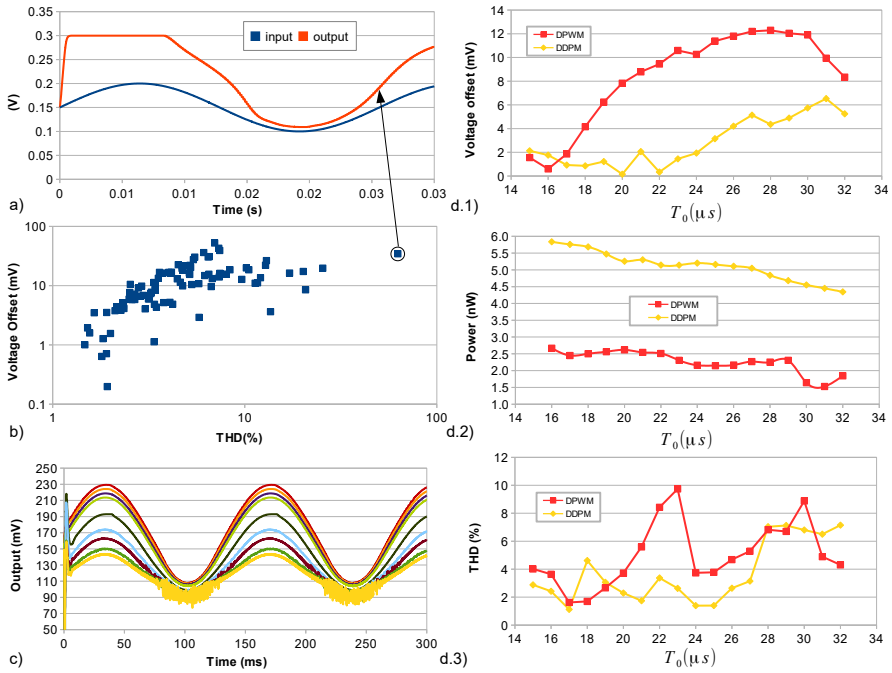


Fig. 2.15 [SIMULATION] a) V_{in} and V_{out} of a bad sample from the MC analysis with 30 Hz frequency, 50 mV peak amplitude and $C_{\text{out}} = 80\,\text{pF}$ b) Thumbnail plot between THD (%) and input offset voltage (mV)—each point is a sampe of the MC simulation c) Changing the BD-OTA offset through DDC using the DPWM modulator d) Trade-off between power and signal integrity (THD) versus T [36].

In the same voltage follower configuration, the DB-OTA without calibration has been verified under process variations for $V_{\text{amp}} = 50\,\text{mV}$, $C_{\text{L}} = 80\,\text{pF}$ and $f_{\text{in}} = 30\,\text{Hz}$ by Montecarlo (MC) simulations on 100 samples. Figure 2.15a shows the V_{in} and V_{out} of a bad sample from this analysis. Mainly due to the mismatch of the DM amplifier first inverter as highlighted before, the output signal of this sample is pushed towards V_{DD} distorting the signal and increasing the offset voltage.

To have a fully insight about this issue, a thumbnail plot between THD (%) and Voltage offset for 100 samples, in which each point is a sample of the MC, is depicted in Figure 2.15b. Pearson's coefficient is applied for the same uncalibrated samples, resulting in 40% of correlation between THD and offset; i.e., if the offset is attenuated, the THD is also improved. The SDC and DDC are used though to tweak the offset of the DB-OTA as shown Figure 2.15c; in this case, the DPWM modulator was chosen.

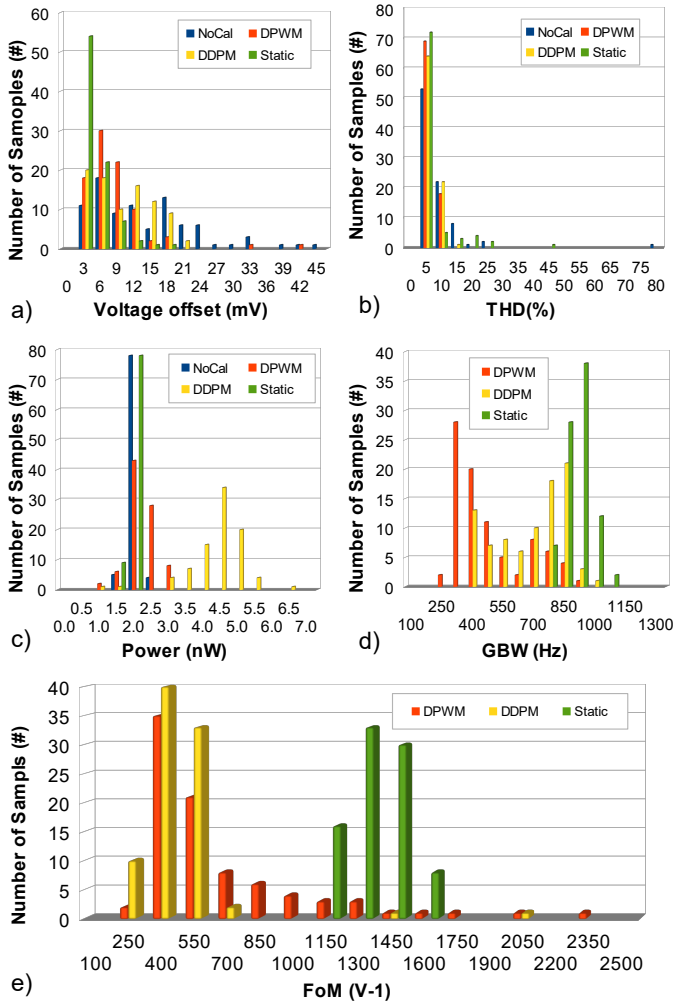


Fig. 2.16 [SIMULATION] a) Voltage offset b) THD c) Power d) GBW e) and $FOM_S = 100\frac{GBWC_{Load}}{I_{DD}}$ histograms [36] .

Both for SDC and DDC, each sample has been recovered by adequately choosing a 3-bit calibration code (to be applied as an input decoder enabling the calibration network in SDC and as the DPWM/DDPM modulators input words for DDC) so that to minimize the simulated input offset voltage. Calibration signals applied just to the non-inverting input branch have been considered to reduce power and area overhead.

In Fig. 2.15d, the calibrated DB-OTA input offset voltage, power (DB-OTA alone), and THD are plotted for one representative sample versus the period T of DDPM and DPWM calibration patterns applied to the enabling transistors in Fig. 2.11b, revealing that improved offset and THD (both slightly better for DDPM

Table 2.1 Monte Carlo simulation results: statistics parameters.

Peformance	No calibration	Static	DPWM	DDPM
Offset Voltage (mV)	$\mu = 12.26$, $\sigma = 9.29$	$\mu = 3.15$, $\sigma = 2.9$	$\mu = 6.86$, $\sigma = 5.8$	$\mu = 8.19$, $\sigma = 5.34$
THD (%)	$\mu = 6.17$, $\sigma = 8.65$	$\mu = 4.6$, $\sigma = 6.18$	$\mu = 3.61$, $\sigma = 1.82$	$\mu = 4.16$, $\sigma = 2.04$
Power (nW)	$\mu = 1.73$, $\sigma = 0.15$	$\mu = 1.65$, $\sigma = 0.13$	$\mu = 1.95$, $\sigma = 0.41$	$\mu = 4.12$, $\sigma = 0.78$
GBW (nW)	-	$\mu = 865.9$, $\sigma = 63.3$	$\mu = 434.4$, $\sigma = 174.28$	$\mu = 643.99$, $\sigma = 166.65$
FoM (V^{-1})	-	$\mu = 1269.5$, $\sigma = 127.7$	$\mu = 592.11$, $\sigma = 385.17$	$\mu = 402.13$, $\sigma = 227.21$

compared to DPWM) can be achieved at lower T at the cost of increased power consumption, which is more relevant for DDPM. An extra power overhead of around 6nW and silicon area of 25 μm $\times$ 25 μm should also be taken into account for DPWM, and DDPM modulators [190].

Trading off power and accuracy, a different period $T = 24$ μs for DPWM and 32 μs for DDPM have been considered as an optimal choice for the two DDC strategies.

To make a fair comparison over different samples, SDC and DDCs have been considered to trim a population of 100 samples keeping the same seed for random number generation in the MC simulations used in Figure 2.15b. Optimal 3-bit calibration words leading to minimum input offset voltage have been first identified for each sample for SDC, and both the DPWM and the DDPM DDC techniques. Then, such optimal calibration words have been applied in simulations to compare the performance statistics of the calibrated samples.

The histogram of the DB-OTA input offset voltage is reported in Figure 2.16a before and after calibration. Without calibration (blue bars), the mean (μ) and standard deviation (σ) are 12.26 mV and 9.29 mV, respectively. Using the SDC (green bars), $\mu = 3.15$ mV and $\sigma = 2.9$ mV have been achieved. While, for the DPWM (red bars) and DDPM (yellow bars), (μ, σ) are (6.86,5.8) mV and (8.19,5.34) mV, respectively. Figures 2.16b–e show the histograms for the THD, Power, GBW and FOM_S.

Table 2.1 lists the mean and the standard deviation (μ, σ) for each performance before and after the static and dynamic calibrations. The DDC shows an average offset reduction of $\times$1.79 for DPWM and $\times$1.5 for DDPM modulation, increasing the THD yield by $\times$1.3 and $\times$1.2, respectively, for 5% THD as threshold.

DDCs are more compatible with a pure digital flow, and they can be easily implemented into the digital part of IoT systems such as the general one in Figure 1.4. However, the power and area overhead intrinsically linked to the dynamical calibration does not bring better results than the SDC (i.e., lower spread over MC

analysis). Consequently, in the following section 2.5 regarding measurements, just SDC is reported.

2.5 Measurements Results

The DB-OTA's measured input and output waveforms are reported in Fig. 2.17a for sample #3, which exhibits the most pronounced non-linearity and hence the highest THD. In this figure, the measurements are taken at a supply voltage of V_{DD}=300mV under a 3-Hz input sine wave with 50-mV amplitude and a significant capacitive load of C_L=80pF. The measurements in Fig. 2.17 reveal that a THD of 1.26% and power consumption of 591 pW are achieved under the above conditions. For the same die, the input offset voltage was measured to be 1.1 mV and the root mean square (r.m.s.) input noise integrated over the 500 Hz input bandwidth is 2.9 mV.

DB-OTA is the first OTA operating in a sub-nW power regime to the best of this thesis author's knowledge. Fig. 2.18a shows the power breakdown among the DB-OTA sub-blocks, in which the most significant contribution is associated with the output stage (55%) followed by the DM amplifier (35%). In contrast, the CM extractor is expected to consume less due to the small size of transistors and capacitor.

The slew rate was evaluated from the response to a square wave input, as shown in in Fig. 2.17b. In particular, for the same input amplitude and load considered above, a positive slew rate (SR_+) of 0.278 V/ms and a negative (SR_-) of 0.25 V/ms were measured.

Fig. 2.19a compares the measured THD to the simulation results in section 2.4. The measured common-mode input range of DB-OTA was found to be lower than 100 mV in the measured samples. The mismatch mainly induces the increased distortion at higher input amplitudes in the input inverters due to their operation in the sub-threshold region. Such dominant mismatch contribution ultimately gives rise to a reduction in the input swing even after calibration.

The DB-GOTA was tested in the closed-loop voltage follower configuration with 50-mV amplitude sine wave input at different frequencies f. The differential voltage gain frequency response was measured in magnitude and phase by taking the ratio of the Fast Fourier Transform (FFT) at each f of the output, and the differential input

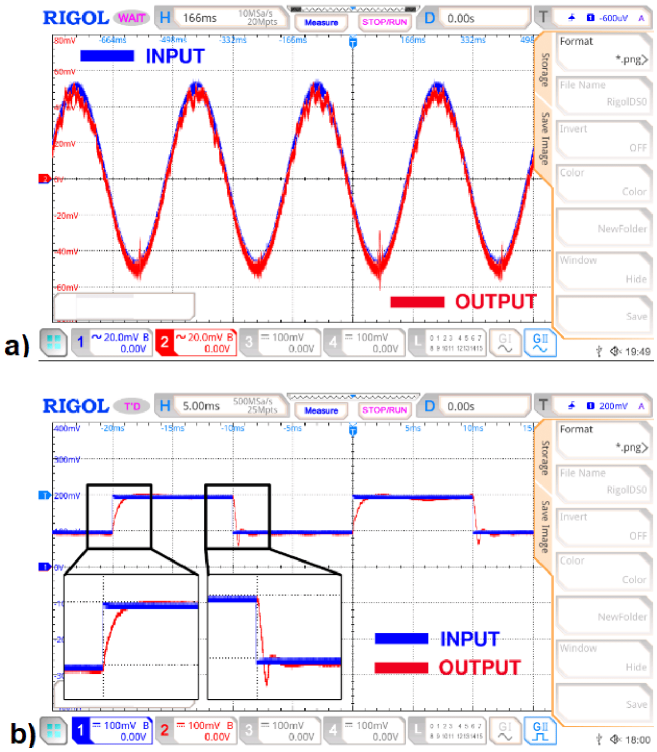


Fig. 2.17 [MEASUREMENTS] a) V_{IN} and V_{OUT} sine waves for C_L=80pF, input amplitude V_{amp}=50mV and frequency f_{in}=3Hz, b) transient response for a square wave input, C_L=80pF, V_{amp}=50mV and f_{in}= 50Hz. The settling time measured at the rising (falling) edge is 1.15 (0.9) ms.

voltage. The DB-OTA frequency response of the measured samples is reported in Figs. 2.19b,c, and exhibits a 29dB DC gain in the considered sample #3, whereas all other samples have larger DC gain up to 31 dB. Also, a Gain Bandwidth Product GBW of 518 Hz was measured, along with a phase margin of 57.3º (51.4º-57.3º over the three dice). The highest measured GBW of 518 Hz across dice is 200 Hz and is below the minimum value presented in previous subsection based on Monte Carlo simulations over 100 runs, which showed a μ_{GBW} =865Hz and σ_{GBW}=63 Hz. The self-oscillation frequency was measured to be 10 kHz (f_0).

The power consumption for a 3-Hz sine wave input with 50-mV amplitude under C_L=80pF was found to be 590 pW, and always lower than 1 nW across all samples (from 407 pW to 697 pW).

The usual small-signal figure of merit in Eq. (2.29) was adopted to evaluate the power efficiency at small inputs:

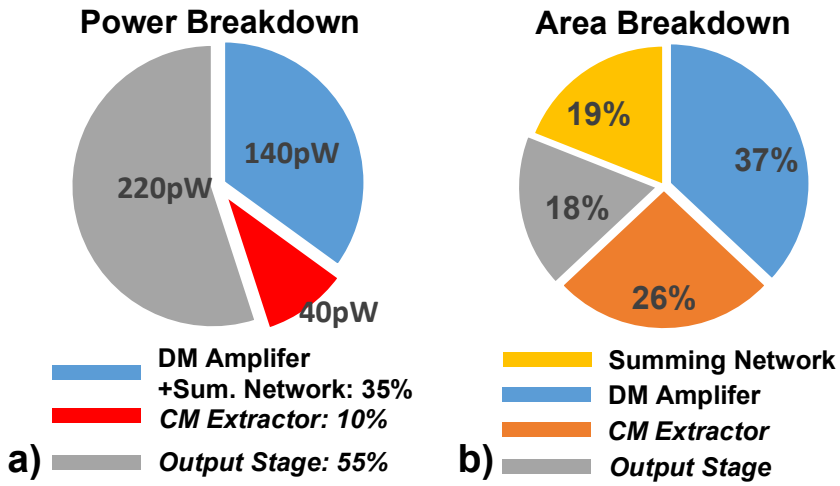


Fig. 2.18 [MEASUREMENTS] a) Power and b) Area breakdown

Table 2.2 PERFORMANCE COMPARISON WITH THE STATE OF THE ART (**BEST PERFORMANCE IN BOLD**)

Performance	**DB-OTA+**		[1]+	[2]+	[3]+	[4]+	[5]* MC-OTA	[5]* FFC-OTA	**DIGOTA+**
	Min	Max							
Architecture	**Digital**		Bulk-driven	Bulk-driven	Bulk-driven	Bulk-driven	Inverter-based	Inverter-based	**Digital**
technology	180		130	65	180	350	130	130	180
V_{DD} [V]	0.3		**0.25**	**0.25**	0.5	0.6	0.3	0.3	0.3
C_{LOAD}[pF]	80		15	15	20	15	2	2	**150**
area [μm^2]	1,426		83,000	2,000	26,000	60,000	-	-	**982**
DC Gain [dB]	31	29	60	**70**	52	69	46.2	49.8	30
GBW [kHz]	0.229	0.518	1.88	9.5	1,200	11.4	2,450	**9,100**	0.25
Slew Rate [V/ms]	0.097	0.264	0.7	0.2	2,890	14.6	2,400	**3,800**	0.085
THD [%]	1.26++	2.82++	**0.2**	-	1	0.08	-	-	2
Phase Margin [^{o}]	51.4	57.3	52.5	89.5	-	65	57	76	90
Power [nW]	**0.407++**	0.591++	18	26	110,000	550	1,800	1,800	2.4
FOMS [V^{-1}]	1352	**2,101**	29	137	0.11	0.18	81	303	468
FOML [-]	573	**1,071**	14.6	3	22.27	23.9	80	140	159

[1] [30]+, [2] [192]+, [3] [181]+, [4] [193]+, [5][31]
+Experimental, *Simulation

$$FOM_S = 100\frac{GBW \cdot C_L}{I_{DD}} \tag{2.29}$$

where $I_{DD} = power/V_{DD}$, evaluates to 2,101 V^{-1} (from 1,352 to 2,101 V^{-1} across the three dice). Analogously, the usual large-signal figure of merit in Eq. (2.30) was evaluated to quantify the power efficiency at large inputs:

$$FOM_L = 100\frac{SR \cdot C_L}{I_{DD}} \tag{2.30}$$

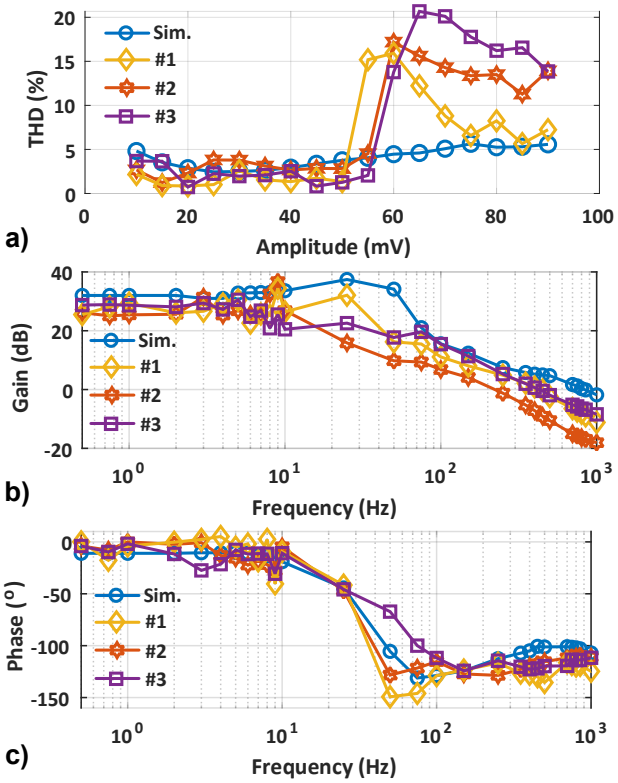


Fig. 2.19 [MEASUREMENTS] a) THD (%) versus peak Vamp for 3Hz frequency b,c) ULV DIGOTA frequency response

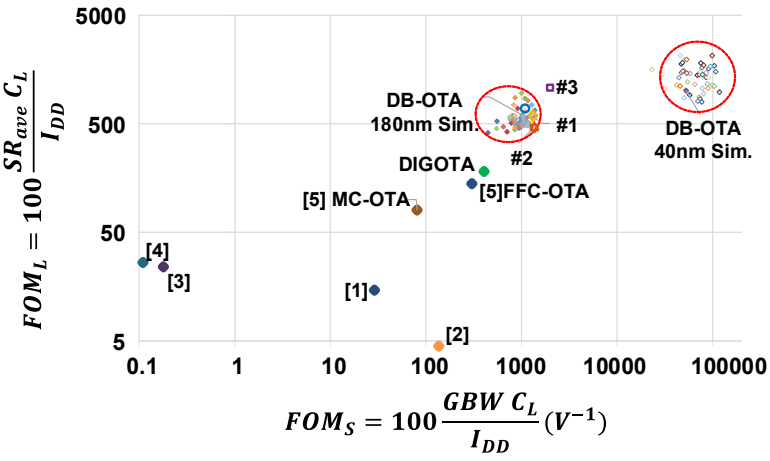


Fig. 2.20 [MEASUREMENTS and SIMULATION] . State-of-art of ultra-low voltage OTAs. #1,#2 and #3 are the three die samples measured in this work. The remaining points within the cloud are results from the Monte Carlo simulation from [35].

where SR is the average between SR_+ and SR_-. The figures of merit in Eq. (2.30) evaluates to 1,071 (from 468 to 1071 across the three dice). Both figures of merit reveal a highly-efficient operation of the DB-OTA circuit, as discussed before.

Compared to prior OTAs proposed in the recent literature in Table 2.2, the DB-OTA drives the second largest output capacitance $C_L = 80$pF at the lowest power consumption. In detail, the DB-OTA power is 4X lower than DIGOTA (see the next subsection), in spite of the area penalty of the calibration network and the pseudo-resistors, and a more pronounced distortion. Interestingly, the proposed DB-OTA is the most power-efficient OTA reported to date, and in particular has a 4.5X improved FOM_S metric compared to the DIGOTA. The comparison in terms of both FOM_S and FOM_L is also illustrated in Fig. 2.20, which shows the power efficiency improvement enabled by DB-OTA over prior art. As done in [35], the results of preliminary transistor-level simulations performed on the circuit ported to 40nm CMOS are also shown in Fig. 2.20, demonstrating the potential benefits brought by technology scaling, based on the digital nature of DB-OTA compared to traditional analog OTAs.

Chapter 3

DIGOTA

This chapter presents a passive-less fully-digital operational transconductance amplifier (DIGOTA) for energy- and area-constrained systems. What differentiates the new DIGOTA from previously presented DB-OTA (chapter 2) is that the former has passive-less self-oscillating common-mode compensation, making the circuit less noisy, more robust to mismatch variations, and more compatible with the digital flow. The chapter organization follows the same structure of the previous one: circuit analysis and design in section 3.1, its layout description in section 3.2, simulation in section 3.3, and measurements in section 3.4.

3.1 Circuit Analysis and Design

As any other OTA, DIGOTAs amplify the differential input $v_D = v_{IN+} - v_{IN-}$, while rejecting the common-mode component $v_{CM} = (v_{IN+} + v_{IN-})/2$ of the input voltages v_{IN+} and v_{IN-}. Like the DB-OTA, the DIGOTA reliance on logic gates inherently reduces the power floor imposed by bias currents and reference circuits necessary in conventional analog OTAs, enabling power savings well beyond their analog counterparts.

In the previous DB-OTAs, a common-mode compensation loop was added to the primary inputs via a passive summing network implemented by on-chip resistors, pseudo-resistors, or quasi-floating gate transistors, at the cost of substantial area overhead (e.g., 45%) and voltage gain degradation (-6dB, see Eq. (2.17)). On the other hand, in the DIGOTA, as shown in Fig. 3.1, the *summing network* is suppressed

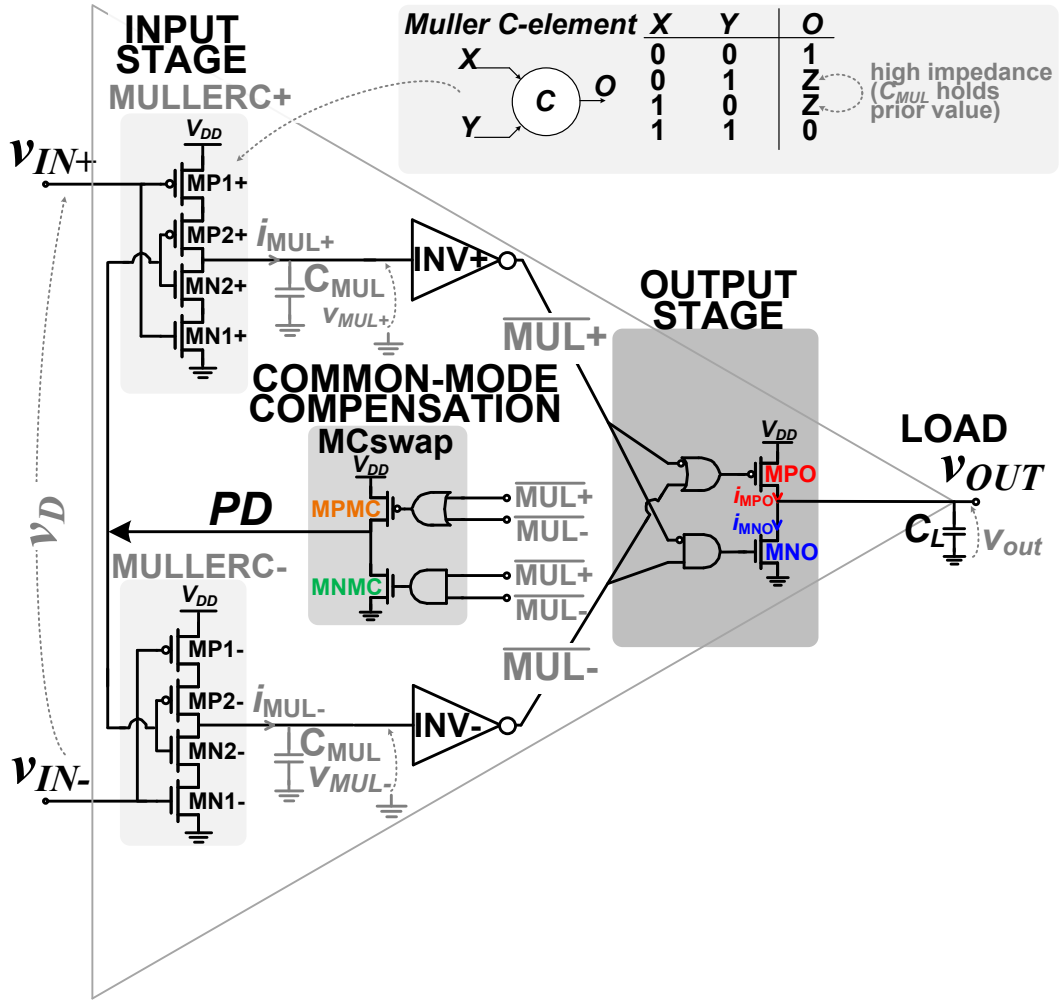
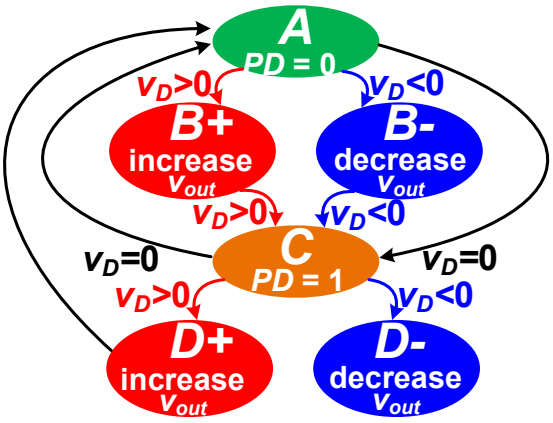


Fig. 3.1 DIGOTA schematic

by introducing an input stage based on the *Muller C-elements* [194]. The *Muller C-element* output is 1 when its inputs are (0,0), 0 when they are (1,1) and held (high impedance mode) at the previous value when they are (0,1) or (1,0) as in Fig. 3.1 top-right.

The two *Muller-C elements* are driven by the two OTA input voltages v_{IN+} and v_{IN-}, and their remaining input is driven by the digital common-mode compensation signal *PD*. *PD* comes from the *Muller-C (MC) swap* subblock. From Fig. 3.1, PD=1 (PD=0) activates the pull-down (pull-up) network of the *Muller C-elements*, and hence leads to a monotonically decreasing (increasing) waveform in their output voltages v_{MUL+} and v_{MUL-}. In turn, these voltages respectively drive the *inverters*,



LOGIC STATES

A	$\overline{MUL_+}$=1 $\overline{MUL_-}$=1	enable MCSwap pull-up (*PD* = 0)
B+	$\overline{MUL_+}$=1 $\overline{MUL_-}$=0	increase v_{out}
B-	$\overline{MUL_+}$=0 $\overline{MUL_-}$=1	decrease v_{out}
C	$\overline{MUL_+}$=0 $\overline{MUL_-}$=0	enable MCSwap pull-down (*PD* = 1)
D+	$\overline{MUL_+}$=1 $\overline{MUL_-}$=0	increase v_{out}
D-	$\overline{MUL_+}$=0 $\overline{MUL_-}$=1	decrease v_{out}

Fig. 3.2 Logic states and state transition graph.

$INV+$ and $INV-$, whose digital outputs ($\overline{MUL_+}$) and ($\overline{MUL_-}$) determine the output PD of the swapping circuit *MCswap* to close the common-mode compensation loop. Similar to the DB-OTA, DIGOTA has the same *output stage* in charge to detect the lag of signals caused by a $v_D \neq 0$.

In summary, while the DB-OTA is comprised by *summing network*, *DM amplifier*, *CM extractor* and *output stages*, the DIGOTA has *Muller C-elements*, *inverters*, *MCswap* and *output stages* as sub-blocks.

3.1.1 Qualitative Circuit Analysis

When a common-mode input is applied (i.e., $v_D = 0$), *MCswap* in Fig. 3.1 detects the conditions (0,0) and (1,1), as described previously for the DB-OTA in the table of Fig. 2.5. Then, it dynamically compensates the common-mode at nodes v_{MUL+} and v_{MUL-} to maintain it around the trip point voltage V_T of the inverter gates $INV+$ and $INV-$. In detail, the conditions ($\overline{MUL_+}$, $\overline{MUL_-}$) equal to (0,0) and (1,1) alternatively enable the pull-up and the pull-down networks of the Muller C-elements via *PD*, based on the state transition diagram in Fig. 3.2. When v_{MUL+} and v_{MUL-} are both lower than V_T (i.e., ($\overline{MUL_+}$, $\overline{MUL_-}$)=(1,1)), DIGOTA operates in state A in Fig. 3.2, and MCswap sets $PD = 0$ to activate the pull-up networks of the *Muller C-elements* as in Fig. 3.3a. This increases v_{MUL+} and v_{MUL-}, bringing their common-mode closer to V_T as desired.

Conversely, when v_{MUL+} and v_{MUL-} are higher than V_T (i.e., ($\overline{MUL_+}$, $\overline{MUL_-}$) = (0,0)), DIGOTA operates in state C (Fig. 3.2), *MCswap* sets $PD = 1$, and the pull-down networks of the *Muller C-element*s are activated (Fig. 3.3c). This brings the common mode of v_{MUL+} and v_{MUL-} again closer to V_T, as desired. Hence, the *MCswap* circuit implements a passive-less self-oscillating loop (see Figs. 3.3a-c) dynamically tracking the effect of the common-mode input on v_{MUL+} and v_{MUL-}, as needed by $INV+$ and $INV-$ to sense the differential input (table of Fig. 2.5).

When a non-zero differential input $v_D = v_{IN+} - v_{IN-}$ is applied, the two input voltages v_{IN+} and v_{IN-} driving the *Muller C-elements* determine the currents i_{MUL+} and i_{MUL-} charging (discharging) the capacitance C_{MUL} at their output, as in Fig. 3.1. Starting from state A as discussed above, a small-signal differential input $v_D > 0$ makes $i_{MUL+} < i_{MUL-}$, generating a proportional differential voltage at their outputs v_{MUL+} and v_{MUL-} as in Fig. 3.3b, while moving to state B+ in Fig. 3.2 (all is reversed if $v_D < 0$, moving to state B-). Once the common-mode of these two voltages is brought close to V_T (i.e., within $V_T \pm v_D/2$) by the above self-oscillating loop, their difference can be discriminated by $INV+$ and $INV-$, respecting the condition $|v_{\rm d}/2| > |v_{\rm CM} - V_{\rm T}|$. In this case, the inverter digital outputs ($\overline{MUL_+}$, $\overline{MUL_-}$) become (1,0) for $v_D > 0$ ((0,1) for $v_D < 0$), triggering operation in state B+ (B-). The same considerations hold when starting from state C in Fig. 3.2, in this case, the circuit moves to state D+ for $v_D > 0$ (D- for $v_D < 0$). The overall DIGOTA state transition graph is summarized in Fig. 3.2 [23].

Finally, the inverter outputs ($\overline{MUL_+}$, $\overline{MUL_-}$) defining the DIGOTA state in Fig. 3.2 drive the output stage, and hence determine the output voltage v_{OUT}. When operating in states B+/D+ (i.e., $v_D > 0$), (($\overline{MUL_+}$, $\overline{MUL_-}$)=(1,0) turns on the pull-up transistor MPO as in Fig. 2a, and correctly raises v_{OUT} as depicted in Figs. 3.3b and 3.3d. The opposite happens in states B-/D- (i.e., $v_D < 0$), which turns on the pull-down MNO transistor to lower v_{OUT}. In practical cases where the DIGOTA is used in a negative-feedback loop configuration (e.g., voltage buffer), v_{OUT} ultimately settles to the value that makes $v_D \approx 0$ Finally, no change in v_{OUT} is observed in states A and C where common-mode compensation is solely performed, as observed in Figs. 3.3a and 3.3c.

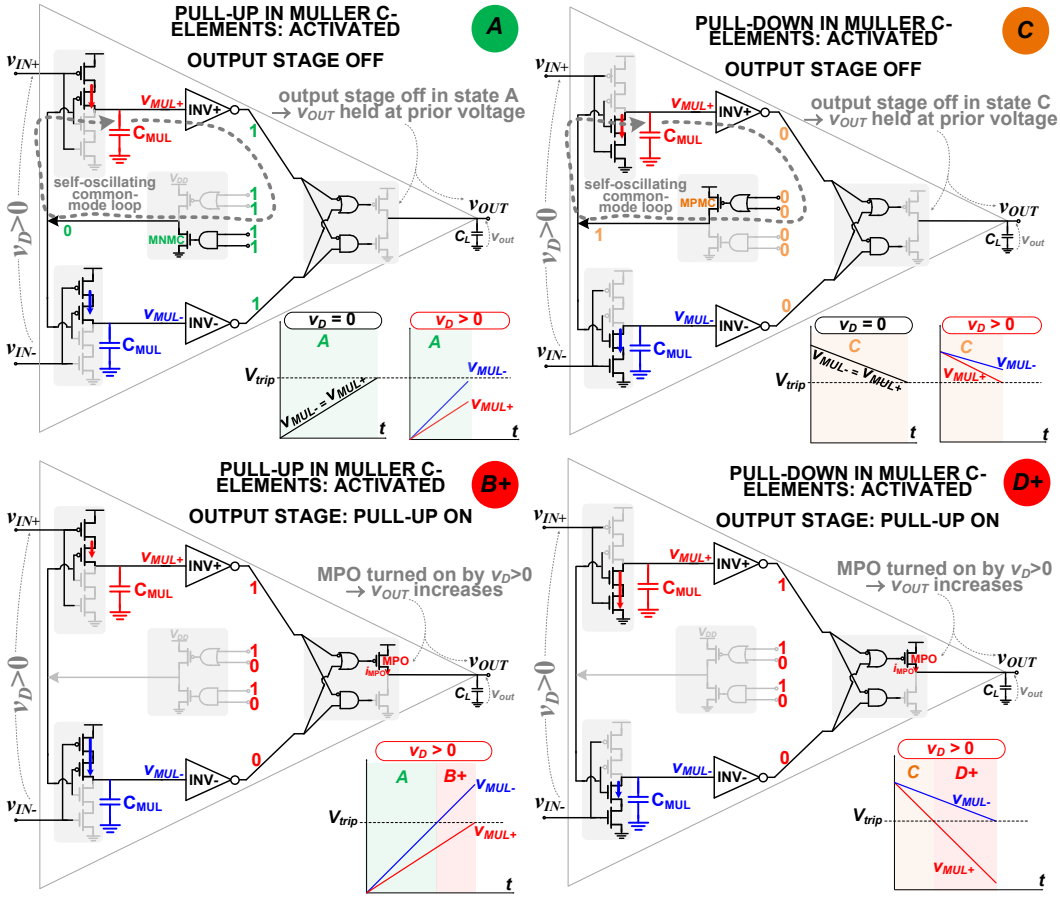


Fig. 3.3 DIGOTA circuit details vs logic state under $v_D > 0$ (reverse all directions for $v_D < 0$). The state sequence follows the transition graph in Fig. 2b: a) A, b) B+, c) C and d) D+. The subscript + (-) refers to the case $v_D > 0$ ($v_D < 0$).

3.1.2 Quantitative Circuit Analysis

A model of the DIGOTA circuit has been developed as done for the DB-OTA. Under a pure common-mode input $v_{IN+} = v_{IN-} = v_{CM}$, only the transitions between state A and C are allowed from Fig. 3.2.

Assuming the initial state A and the initial condition $v_{MUL+} = v_{MUL-} = V_{min}$, the output voltages of the *Muller C elements* v_{MUL+} and v_{MUL-} equally increase due to circuit symmetry (see Figs. 3.1, 3.3a and 3.4). In particular, transistors MN2+ and MN2- in Fig. 3.1 are OFF, MP2+ and MP2- are ON (or less OFF), and MP1- and MP1+ are in certain inversion level (see Figs. 3.1 and 3.3a).

The inversion level of a MOS transistor is extracted by a non-linear expression, called Unified Charge-Control Model (UCCM) [18, 19], where it is linked with the transistor terminal voltages as shown in Eq. (3.1).

$$\frac{V_{GB}-V_{T0}}{n}-V_{S(D)}=\phi_t\left[\sqrt{1+i_{f(r)}}-2+ln\left(\sqrt{1+i_{f(r)}}-1\right)\right] \tag{3.1}$$

where V_{GB},V_{SB}, and V_{DB} are gate, source and drain to bulk voltages, V_{T0} is threshold voltage, ϕ_t is the thermal voltage and $i_{f(r)}$ is the forward (reverse) inversion level. The i_f and i_r define the equivalent MOS transistor drain current (I_D) through Eq. (3.2),

$$I_D=\mu C'_{ox}n\frac{\phi_t^2}{2}\frac{W}{L}(i_f-i_r) \tag{3.2}$$

where μ is the low field mobility, C'_{ox} is the oxide capacitance per unit of area, n is defined as slope factor, W is transistor width, L is channel length. To achieve ultra-low power operation, the transistors inside of DIGOTA operate in weak inversion and saturation (p.s., for internal waverforms around middle V_{DD}) due to the low voltage supply, i.e., $0.1 > i_f >> i_r$ leading to

$$I_D=\mu C_{ox}n\phi_t^2 e\left(\frac{W}{L}\right)e^{(\frac{V_{GB}-V_{T0}}{n}-V_S)/\phi_t}(1-e^{V_{DS}/\phi_t})\approx\mu C_{ox}n\phi_t^2 e\left(\frac{W}{L}\right)e^{(\frac{V_{SG}-V_{T0}}{n\phi_t})} \tag{3.3}$$

Note that, for saturation, $V_{DS} > 4\cdot\phi_t$ leads to $(1-1/e^4)=0.9817\approx 1$.

Since $v_{IN+}=v_{IN-}=v_{CM}$, the drain current i_{MUL+} (i_{MUL-}) of MP1+ (MP1-) charging the capacitance C_{MUL} in Fig. 3.1 is given by Eq. (3.3). Assuming that the input is nearly constant during state A, from Fig. 3.4, C_{MUL} is charged at the constant current $I_{CM,A}$ given by Eq. (3.3) with $v_{SG}=V_{DD}-v_{CM}$, leading to a ramp-like increase in v_{MUL+} and v_{MUL-} from V_{min} to V_T over the period of time τ_{MUL} in (3.4)

$$\tau_{MUL}=(V_T-V_{min})\cdot\frac{C_{\mathrm{MUL}}}{I_{CM,A}}=(V_T-V_{min})\frac{C_{\mathrm{MUL}}}{\mu C_{ox}n\phi_t^2 e\left(\frac{W}{L}\right)e^{\frac{V_{DD}-v_{CM}-V_{T0}}{nkT/q}}} \tag{3.4}$$

Once $v_{MUL+} = v_{MUL-} = V_T$, the subsequent inverters *INV+* and *INV-* switch their output from 1 to 0 after a gate delay τ_{INV}, as in Fig. 3.4. Then, the *PD* signal is updated and makes a $0 \rightarrow 1$ transition after an *MCswap* gate delay τ_{MCswap}, thus moving from state A to C as in Fig. 3.4.

From the above considerations and Fig. 3.4, the resulting overall duration T_A of state A is hence equal to

$$T_A = (V_T - V_{min}) \cdot \frac{C_{\mathrm{MUL}}}{I_{CM,A}} + \tau_{INV} + \tau_{MCswap} \tag{3.5}$$

at the end of which v_{MUL+} and v_{MUL-} have kept increasing to their maximum value V_{max} due to the uninterrupted charge of C_{MUL} during the *inverter* and the *MCswap* delay. The above analysis can be repeated for state C by considering that v_{MUL+} and v_{MUL-} will now decrease from V_{max} down to V_T due to the discharge of C_{MUL} through the *Muller C-element* NMOS current $I_{CM,C}$ in state C (instead of PMOS, see Fig. 3.3c), trigger the transition of *INV+* and *INV-* after τ_{INV}, and the $0 \rightarrow 1$ transition of *PD* after τ_{MCswap} to return to state A. Hence, the overall duration T_C of state C results to

$$T_C = (V_{max} - V_T) \cdot \frac{C_{\mathrm{MUL}}}{I_{CM,C}} + \tau_{INV} + \tau_{MCswap}. \tag{3.6}$$

Therefore, the overall self-oscillation period $T_0 = T_A + T_C$ is given by

$$T_0 = (V_T - V_{min}) \cdot \frac{C_{\mathrm{MUL}}}{I_{CM,A}} (V_{max} - V_T) + \frac{C_{\mathrm{MUL}}}{I_{CM,C}} + 2\left(\tau_{INV} + \tau_{MCswap}\right) \tag{3.7}$$

Assuming $V_{min} = 0$, $V_{max} = V_{DD}$ and $V_T = V_{DD}/2$, which are reasonable approximations for ultra low voltage, then

$$T_0 = \frac{1}{f_0} = V_{DD} \cdot \frac{C_{\mathrm{MUL}}}{I_{CM}} + 2\left(\tau_{INV} + \tau_{MCswap}\right) \tag{3.8}$$

where

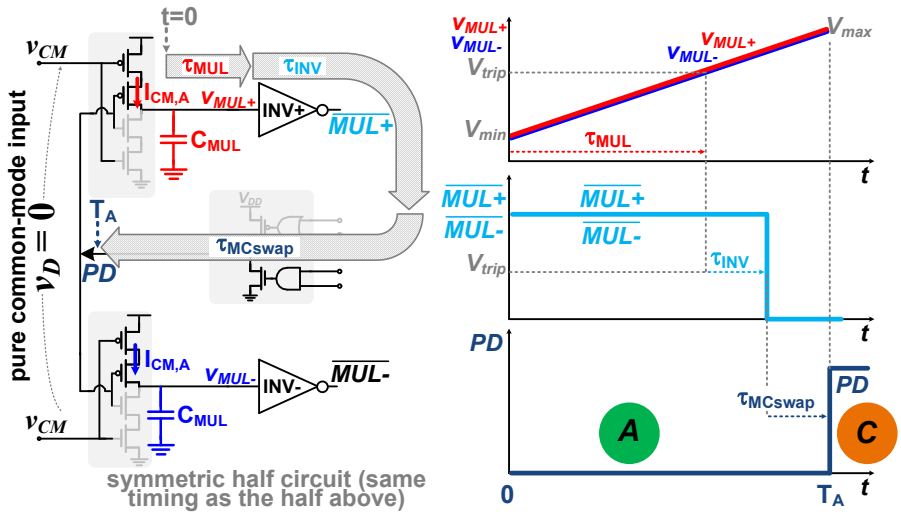


Fig. 3.4 Timing analysis of the self-oscillating loop timing under pure common-mode inputs, and evaluation of the time T_A spent in state A.

$$I_{CM} = \frac{2}{\frac{1}{I_{CM,A}} + \frac{1}{I_{CM,C}}} = \frac{2}{\frac{1}{I_0 e^{\frac{V_{DD}-v_{CM}}{\frac{nkT}{q}}}} + \frac{1}{I_0 e^{\frac{v_{CM}}{\frac{nkT}{q}}}}} = \frac{I_0 e^{\frac{V_{DD}/2}{nkT/q}}}{\cosh\left(\frac{v_{CM}-\frac{V_{DD}}{2}}{nkT/q}\right)} \tag{3.9}$$

From Eq. (3.8), T_0 is set by the sum of the (typically dominant) delay associated with the Muller C-element, the inverters *INV+* and *INV-*, and the *MCswap* gate delay. In summary, T_0 is the natural the self-oscillation period of DIGOTA and has the well-understood digital logic-like dependence on voltage, temperature, and gate sizing [83].

When a small-signal differential input voltage v_D is added to the common-mode component v_{CM}, its effect can be analyzed as a perturbation to the self-oscillatory circuit behavior [195]. The assumption of slow-varying input signals compared to the self-oscillation frequency allows to average out the fluctuations of small-signal parameters during each period. This makes it possible to rely on straightforward small-signal analysis, as detailed in the following.

The circuit in Fig. 3.1 can be linearized as shown in Fig. 3.5. The first stage describes the equal small- signal currents $i_+ = i_-$ with opposite directions coming from the *Muller C-elements*, as determined by the opposite small-signal components of $v_{IN+} = v_D/2$ and $v_{IN-} = -v_D/2$. Being small-signal components, these currents are superimposed to the common-mode, Eq.(3.9), and g_m can be expressed as the

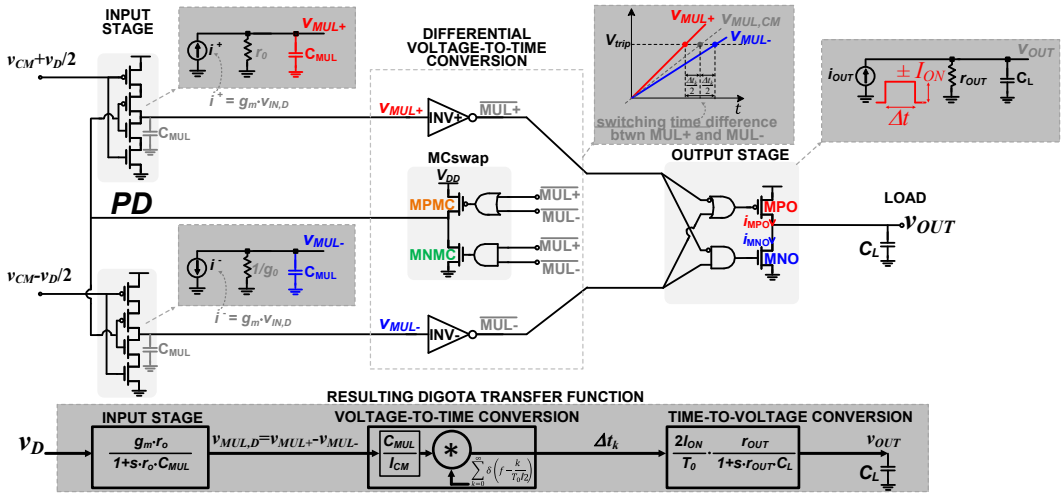


Fig. 3.5 DIGOTA equivalent circuit and transfer function under differential input v_D.

weighted sum of the transconductances $g_{m,A}$ and $g_{m,C}$ of the DIGOTA circuit in state A and C. The weight is given by the fraction of the period spent in each state, thus leading to

$$g_m = g_{m,A}\frac{T_A}{T_0} + g_{m,C}\frac{T_C}{T_0} \approx \frac{I_{CM,A}}{nkT/q}\frac{I_{CM}}{2I_{CM,A}} + \frac{I_{CM,B}}{nkT/q}\frac{I_{CM}}{2I_{CM,B}} = \frac{I_{CM}}{nkT/q} \tag{3.10}$$

The same approach can be done for r_o, leading to a $r_o = \frac{nkT/q}{\lambda_{DIBL} I_{CM}}$. λ_{DIBL} is the drain induced barrier lowering (DIBL) coefficient.

Qualitatively, from Fig. 3.5 the opposite small-signal currents i_{MUL+} and i_{MUL-} at the outputs of the Muller C-elements lead to different slopes in voltages v_{MUL+} and v_{MUL-}, during state A (same for C). This leads to a small-signal difference of the time when v_{MUL+} and v_{MUL-} reach V_T, and hence to the signed difference Δt between the switching of the $INV+$ and the $INV-$ output. Under small-signal analysis, such time difference Δt is inherently proportional to v_D. As exemplified in Fig. 3.6, during states B and D the time difference Δt activates the output stage transistor MPO if $v_D > 0$ (MNO if $v_D < 0$), which charges (discharges) the capacitive load C_L. This translates into a small-signal change in v_{OUT} that is proportional to v_D, and has the same sign, as expected from an OTA (see Fig. 3.6). From the small-signal circuit in Fig. 3.5, the transfer function from v_D to the differential output at the Muller-C elements is

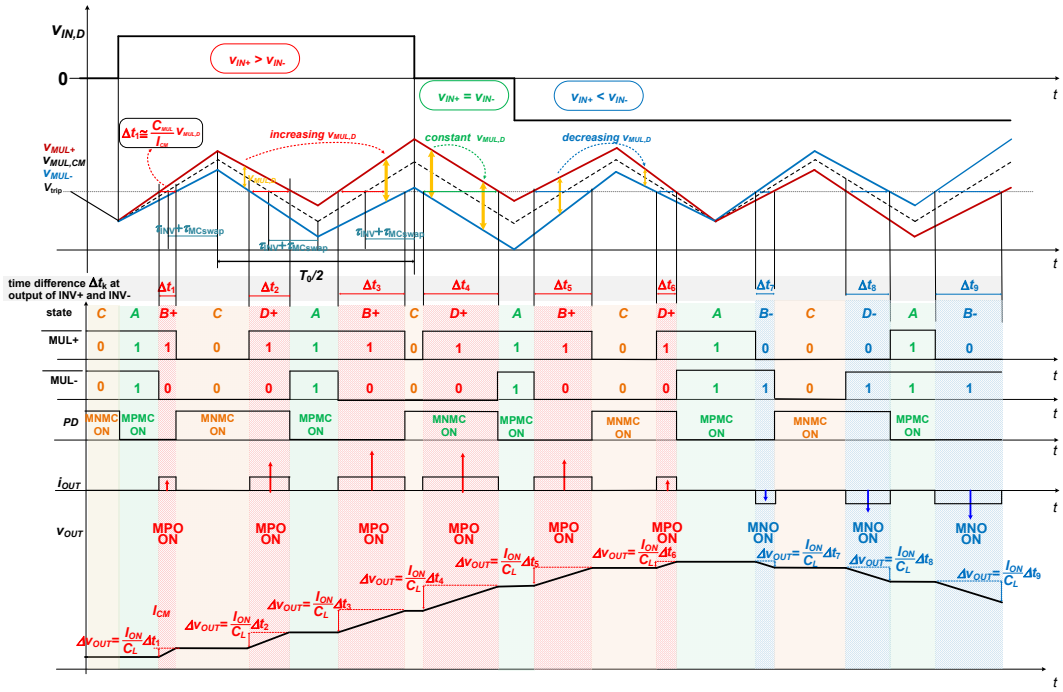


Fig. 3.6 Operation of DIGOTA under positive and negative input differential voltages.

$$\frac{v_{MUL,D}(s)}{v_D(s)} = \frac{v_{MUL+}(s) - v_{MUL-}(s)}{v_D(s)} = \frac{g_m r_o}{1 + s \cdot r_o C_{MUL}}. \tag{3.11}$$

From Eq. (3.11), the input stage has a first-order transfer function whose low frequency gain is equal to the transistor intrinsic gain $g_m r_o$.

The impact of v_D on the differential output of the *Muller-C elements* determines a difference Δt in the point of time when V_T of $INV+$ and $INV-$ are crossed by v_{MUL+} and v_{MUL-}, as shown in Fig. 3.5 and exemplified in Fig. 3.6. The difference Δt_k at a given cycle k of the common-mode self-oscillation with the period $T_{CM,k}$ in Eq. (3.8) stems from the voltage-to-time conversion performed by the $INV+$ and $INV-$, and is crucial for the DIGOTA circuit operation. In detail, the DIGOTA circuit operates in state B (D) during the time interval $(T_{CM,k} - \Delta t_k/2, T_{CM,k} + \Delta t_k/2)$ right after being in state A (C), thus enabling the output stage as in Fig. 3.6. During this interval, the load capacitance C_L is charged (discharged) for a time proportional to Δt_k if $v_D > 0$ ($v_D < 0$). Assuming again that the input varies slowly and is nearly constant during T_0, v_{MUL+} and v_{MUL-} around V_T can be expressed through linear interpolation, thus yielding

$$v_{MUL+}\left(T_{CM,k}-\frac{\Delta t_k}{2}\right)=v_{MUL,CM}\left(T_{CM,k}-\frac{\Delta t_k}{2}\right)+\frac{v_{MUL,D}(T_{CM,k})}{2}$$

$$=v_{MUL,CM}\left(T_{CM,k}\right)-\left.\frac{\partial v_{MUL,CM}}{\partial t}\right|_{T_{CM,k}}\frac{\Delta t_k}{2}+\frac{v_{MUL,D}(T_{CM,k})}{2} \tag{3.12}$$

$$v_{MUL-}\left(T_{CM,k}+\frac{\Delta t_k}{2}\right)=v_{MUL,CM}\left(T_{CM,k}+\frac{\Delta t_k}{2}\right)-\frac{v_{MUL,D}(T_{CM,k})}{2}$$

$$=v_{MUL,CM}\left(T_{CM,k}\right)+\left.\frac{\partial v_{MUL,CM}}{\partial t}\right|_{T_{CM,k}}\frac{\Delta t_k}{2}-\frac{v_{MUL,D}(T_{CM,k})}{2} \tag{3.13}$$

The common-mode voltage contribution $v_{MUL+}=v_{MUL-}=v_{MUL,CM}$ in Eq. (3.12) and 3.13 is due to the discharge of capacitors through the common-mode current I_{CM} in Eq. (3.9) at the constant rate I_{CM}/C_{MUL}. This makes $\left.\frac{\partial v_{MUL,CM}}{\partial t}\right|_{T_{CM,k}}$ equal to I_{CM}/C_{MUL} in Eq. (3.12) and (3.13). Also, $v_{MUL,CM}(T_{CM,k})=V_T$ since $T_{CM,k}$ is defined as the time at which $v_{MUL,CM}$ crosses V_T. Accordingly, Eq. (3.12) and (3.13) lead to the following $\Delta t_k/v_{MUL,D}$ transfer function

$$\frac{\Delta t_k}{v_{MUL,D}(T_{CM,k})}=\frac{C_{\mathrm{MUL}}}{I_{CM}} \tag{3.14}$$

which quantifies the small-signal voltage-to-time conversion performed by $INV+$ and $INV-$ in Fig. 3.5. Since zero crossings occur every half period, voltage-to-time conversion takes place every $T_0/2$ and leads to the generation of a signed time difference Δt_k whose sign is the same as v_D, and its width is proportional to $v_{MUL,D}$ evaluated at $kT_0/2$. In other words, the input is effectively sampled with a sampling period $T_0/2$, where T_0 is expressed in Eq. (3.8). Hence, as in the DB-OTA, the negative feedback in DIGOTA through the *MCswap* circuit acts such as a self-oscillating threshold sampler [186] with a natural sampling frequency of $2/T_0$.

In the output stage in Fig. 3.5, the pulses Δt_k turn on the MPO (MNO) if $v_D>0$ ($v_D<0$) for a duration Δt_k. When the time difference Δt_k is non-zero, MPO (MNO)

generates a current $I_{ON}(-I_{ON})$ driving the capacitive load, as MPO and MNO are sized to deliver the same current to C_L. Since time pulses Δt_k take place every $T_0/2$, the output stage current $i_{OUT}(t)$ driving C_L can be written as

$$i_{OUT}(t) = \sum_{k=0}^{+\infty} I_{ON} \Delta t(t) \delta \left(t - \frac{k}{2f_0} \right) \tag{3.15}$$

where the sign of the output current was incorporated in Δt_k, from the above considerations. The Laplace transform of Eq. (3.15) can be evaluated as in [34] from the z transform of Δt_k evaluated in $z = e^{(sT_0/2)}$. Assuming that the input signal frequency is much lower (10X less) than the self-oscillation frequency $2/T_0$ (e.g., by at least an order of magnitude), the output current $I_{out}(s)$ is evaluated by putting together the Eqs. (3.11), (3.14), and (3.15). Straightforward calculations reveal that $I_{out}(s)$ is related to the input differential voltage $V_D(s)$ as in a first-order continuous-time linear circuit, as demonstrated in the previous chapter for the DB-OTA.

More specifically, considering that I_{out} flows through the impedance defined by r_{OUT} in parallel with C_L from Fig. 3.5, the differential voltage gain transfer function of DIGOTA is

$$A_D(s) = \frac{V_{OUT}(s)}{V_D(s)} = \frac{2 g_m r_o \cdot \frac{I_{ON}}{I_{CM}} \cdot \frac{r_{OUT} C_{\mathrm{MUL}}}{T_0}}{(1 + s \cdot r_{OUT} C_L) \cdot (1 + s \cdot r_o C_{MUL})} \tag{3.16}$$

From Eq. (3.16), DIGOTA has a second-order transfer function when a differential input is applied and the its DC gain is

$$A_{V0} = 2 g_m r_o \cdot I_{ON} \cdot \frac{r_{OUT} C_{\mathrm{MUL}}}{T_0 \cdot I_{CM}} \tag{3.17}$$

and is much higher than one. Indeed, $g_m r_o > 1$ since it is the intrinsic transistor gain, whereas $I_{ON}/I_{CM} > 1$ since the output stage always sees a full-swing input and is hence fully ON, whereas I_{CM} in Eq. (3.9) is much lower than the transistor ON current.

The frequency response in Eq. (3.16) has two real negative poles:

$$s_{p1} = -\frac{1}{r_{OUT} C_{\mathrm{L}}} \quad \therefore \quad s_{p2} = -\frac{1}{r_o C_{\mathrm{MUL}}} \tag{3.18}$$

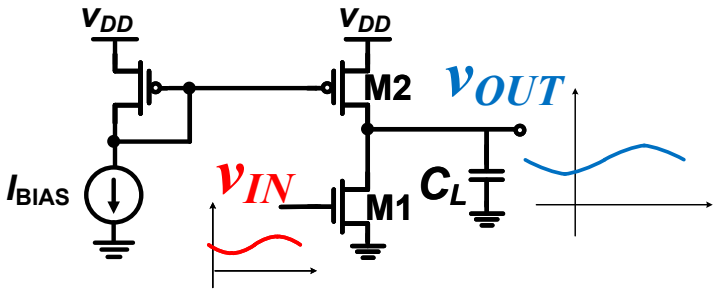


Fig. 3.7 Common-Source amplifier biased in weak inversion. During the calculation the required I_Q, the current of left side of the current mirror is neglected.

where s_{p1} is dominant, since the load capacitance C_L is orders of magnitude larger than the transistor parasitic capacitance C_{MUL}, whereas r_{OUT} and r_o are small-signal transistor output resistances and are hence much closer to each other. The resulting gain-bandwidth product f_{GBW} is

$$f_{GBW} = \frac{1}{2\pi} \cdot \frac{2}{T_0} \cdot \frac{I_{ON}}{I_{CM}} \cdot g_m r_o \cdot \frac{C_{MUL}}{C_L} \tag{3.19}$$

The expression of the power consumption of DIGOTA is similar to the DB-OTA one. It is re-written here below just as matter of the convenience.

$$P_{DIGOTA} \approx \frac{2}{T_0} C_{int} V_{DD}^2 + f_S C_L V_{OUT}^2 \tag{3.20}$$

Interestingly, DIGOTA is inherently more power-efficient than a conventional common-source (CS) amplifier biased in weak inversion [118] keeping the same gain-bandwidth product (see Fig. 3.7). This is shown by comparing the DIGOTA power in Eq. (3.20), and the power P_{CS} of the common-source stage in Eq. (3.21)

$$P_{CS} = V_{DD}\, I_Q|_{f_{GBW}} = 2\pi f_{GBW} C_L \frac{nkT}{q} V_{DD} \tag{3.21}$$

which was evaluated as the product of the supply voltage and the quiescent current I_Q required to match the same f_{GBW}. The resulting power ratio leads to

$$\frac{P_{DIGOTA}}{P_{CS}} \approx \frac{P_{gates}}{P_{CS}} = \frac{1}{4\pi g_m r_o} \frac{C_{int}}{C_{MUL}} \frac{I_{CM}}{I_{ON}} \frac{V_{DD}}{nkT/q} \tag{3.22}$$

Table 3.1 Parameters From Simulations, DIGOTA Transistor Sizes

Transistor	W (μm)	L (μm)	Transistor	W (μm)	L (μm)
$MN1_{\pm}$	3.9	0.18	$MP1_{\pm}$	9	0.18
$MN2_{\pm}$	5	0.18	$MP2_{\pm}$	6.85	0.18
MNMC	1	0.18	MPMC	2.5	0.18
MNO	1	0.18		8.48	0.18
	strength			strength	
$INV_{\pm}$	5X		AND/OR	5X	
NegNOR	5X		NegAND	5X	
parameter	value	unit	parameter	value	unit
T_0	13	μs	r_{OUT}	7.8	nS
g_m	27	nS	C_{MUL}	8	fF
g_0	1.35	nS	C_{int}	170	fF
I_{CM}	930	pA	C_L	150	pF
I_{ON}	9.15	nA			

when the P_{DIGOTA} is dominated by internal oscillation f_0.

Simulations in 180 nm CMOS at $V_{DD} = 0.3V$ for $f_S = 2$Hz lead to the effective small-signal parameter values (averaged over the common-mode input values) in Table 3.1, from which the ratio in Eq. (3.22) makes the DIGOTA power 23X lower than the conventional CS stage (without counting the extra circuit needed to bias the CS). This improvement is achieved thanks to the suppression of the constant power required by a bias current, in view of the digital nature of DIGOTA.

When the DIGOTA power is dominated by the P_{out} (e.g., large C_L, signal amplitude ΔV_{OUT}, and frequency $f_S \approx f_{GBW}$), the expression of the power ratio becomes

$$\frac{P_{DIGOTA}}{P_{CS}} \approx \frac{1}{g_m r_o} \cdot \frac{1}{nkT/q} \frac{V_{OUT}^2}{V_{DD}} \tag{3.23}$$

which corresponds to a 16X power saving under full-swing output $V_{OUT} = V_{DD}/2$. DIGOTA has an intrinsic advantage in power efficiency regardless of the specific load and input signal.

3.1.3 Circuit Design

The DIGOTA architecture in Fig. 3.1 is fully digital and can hence be designed with digital standard cells and no passives, drastically reducing the design and the

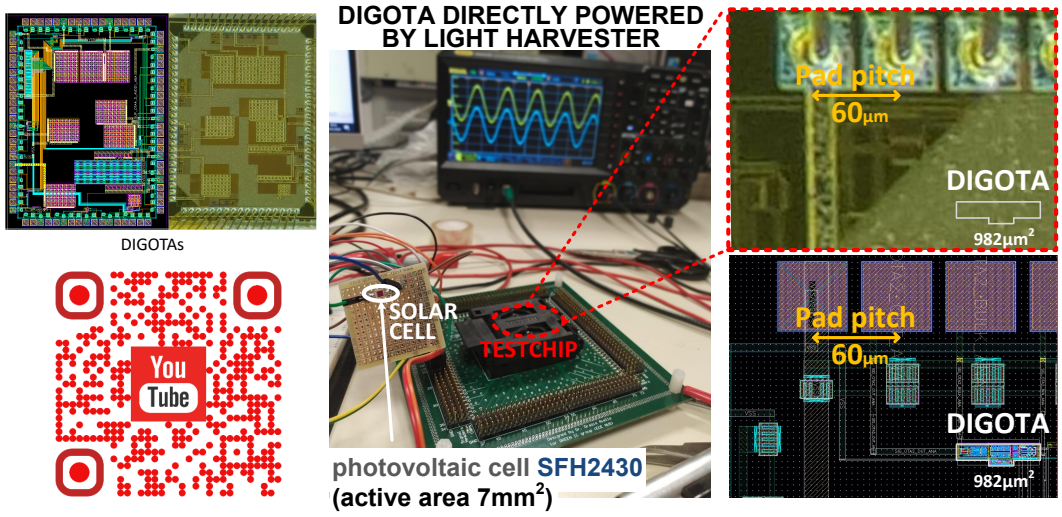


Fig. 3.8 Test bench, micrograph of the DIGOTA 180-nm testchip and layout. Use the QR code to watch the demo video of the DIGOTA working powered by light harvester (7 mm^2).

system integration effort. Compared to conventional analog design, DIGOTA enables digital-like area scaling across technology generations, and design and technology portability. As main limitation, the adoption of standard cells restricts the choice of transistor sizes to the discrete set of strengths available in the adopted library. Also, Muller-C cells might not be directly available in the library, although they can be easily implemented by merging an open-drain NAND and NOR gate, as shown in Fig. 3.1 top-right.

In the 180-nm testchip designed to experimentally validate DIGOTA models (see Fig. 3.8), cells were sized to pursue high power efficiency, as quantified by the small-signal and the large-signal figures of merit in Eqs. (3.24) and (3.25) [25] :

$$FOM_S = \frac{GBW \cdot C_L}{Power} \tag{3.24}$$

$$FOM_L = \frac{SR \cdot C_L}{Power} \tag{3.25}$$

where $SR = I_{ON}/C_L$ is the slew rate averaged between the rising and falling transitions. FOM_S is used to demonstrate how efficient the OTA is, showing for a fixed load C_L how much Hz of bandwidth is achieved per unit of power. On the other hand,

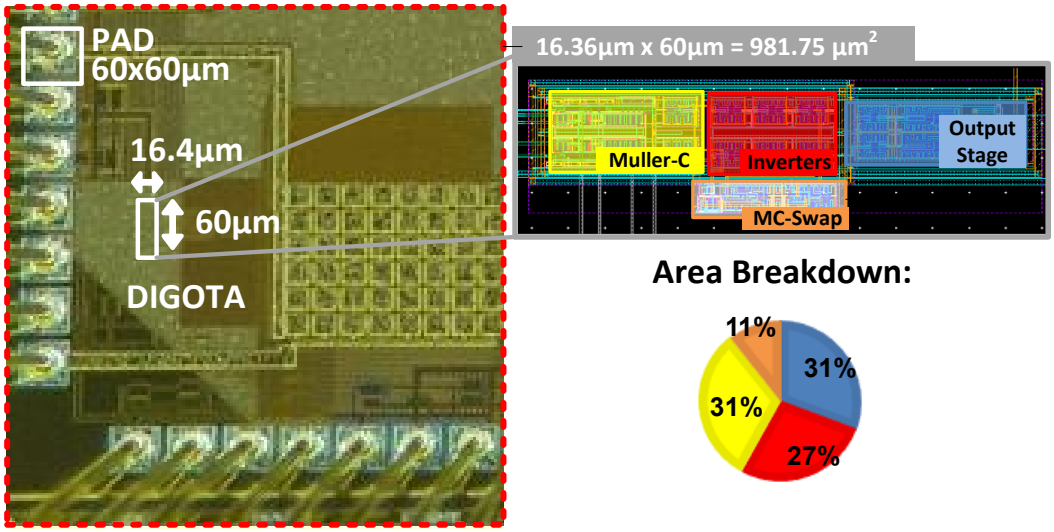


Fig. 3.9 Micrograph of the DIGOTA 180 nm testchip and area breakdown.

for the same fixed load, FOM_L expresses the ability of the OTA to vary its output voltage under large-signal operation normalized to its power consumption. Note that $SR = dv_{out}/dt$.

By substituting (3.19) and (3.20) in (3.24) and (3.25), the figures of merit can be simplified as

$$FOM_S = \left(\frac{g_m r_o}{2\pi C_{int} V_{DD}^2} \frac{C_{MUL}}{I_{CM}}\right) \cdot I_{ON} \tag{3.26}$$

$$FOM_L = \left(\frac{1}{C_{int} V_{DD}} \frac{C_{MUL}}{I_{CM}}\right) \cdot I_{ON} \tag{3.27}$$

Both FOMs are inversely proportional to C_{int} and the slope I_{CM}/C_{MUL} of the *Muller-C element* output voltage. Hence, the FOMs expectedly benefit from the adoption of minimum-sized logic gates and the reduction in the self-oscillation frequency in Eq. (3.8), as they both reduce the consumption associated with the logic gates in the self-oscillating loop.

Regarding the output stage, higher strength and I_{ON} in the output stage directly improve both figures of merit. The cell strengths within the self-oscillating loop were chosen as a tradeoff between the offset voltage (decided by the Muller-C area accoring to Pelgrom's law [188]), the bandwidth, and the input-referred noise

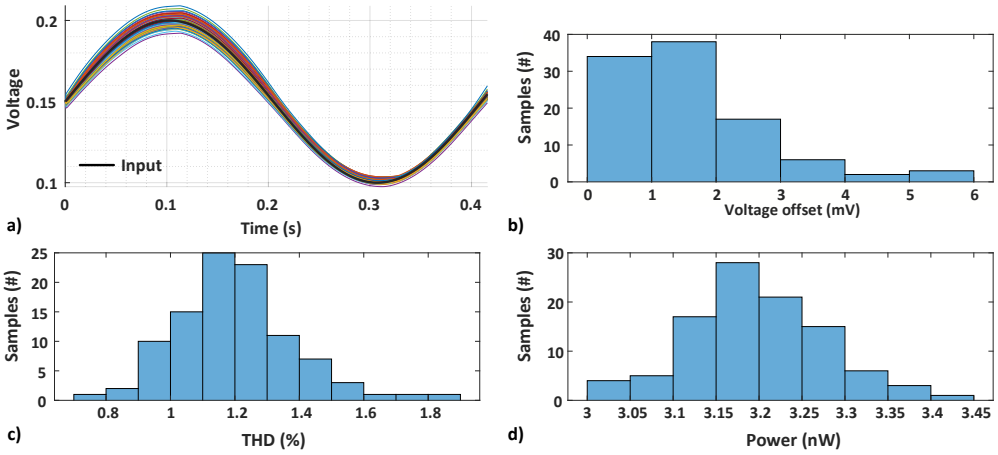


Fig. 3.10 [SIMULATIONS] a) Input and Output waveform in voltage follower configuration for a 100 samples MC analysis. b) Voltage offset c) THD d) Power histograms for a 100 samples MC analysis.

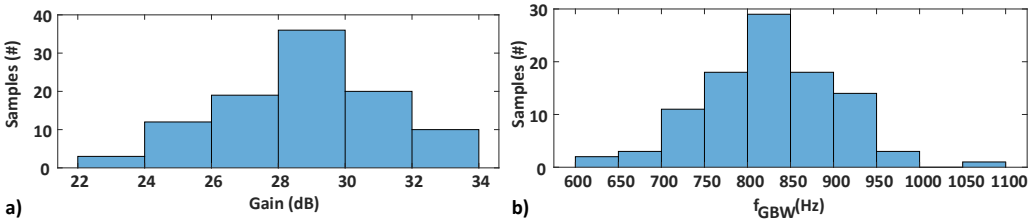


Fig. 3.11 [SIMULATIONS] a) DC gain and b) f_{GBW} histograms for a 100 samples MC analysis.

(decided by the Muller-C area and power). In particular, reducing offset voltage and noise requires transistor up-sizing in the first stage, whereas improving f_{GBW} requires transistor up-sizing in the output stage so that a higher I_{ON} is delivered. The strength of the output stage cell was set to drive a load capacitance of C_L=150 pF at f_{GBW}=800 Hz, to demonstrate the power efficiency of DIGOTA even under heavy capacitive loads.

3.2 Layout

The DIGOTA core occupies an area of 982 μm^2, as shown in Fig. 3.9. The DIGOTA area breakdown is also shown in Fig. 3.9, highlighting that *Muller-C* occupies 31%

of total area as well as the *output stage*. Inverters spend 27% of silicon area, while the *MCSwap* only 11%.

3.3 Simulations Results

Unlike the DB-OTA in which its voltage offset is strongly dependent on the inverter trip point mismatch (see Eqs. (2.26) - (2.28)), the *Muller-C* first stage gain given by the Eq. (3.11) is found to be less sensitive to device mismatch. Eq. (3.28) shows that the more relevant terms for the total offset voltage are the mismatch of *Muller-C element*. Moreover, the mismatch from the summing network is eliminated.

$$\sigma_{V_{\mathrm{OS}}} \approx \sqrt{\frac{\sigma^2_{\mathrm{I_N}}}{g_m^2} + \frac{\sigma^2_{\mathrm{I_P}}}{g_m^2} + \frac{\sigma^2_{C_{MUL}} \cdot I^2_{CM,TP}}{\left(g_m C_{MUL}\right)^2} + \frac{\sigma^2_{V_T}}{\left(g_m r_o\right)^2}} \approx \sqrt{\frac{\sigma^2_{\mathrm{I_N}}}{g_m^2} + \frac{\sigma^2_{\mathrm{I_P}}}{g_m^2} + \frac{\sigma^2_{C_{MUL}} \cdot I^2_{CM,TP}}{\left(g_m C_{MUL}\right)^2}} \tag{3.28}$$

where σ represents the the local variations w.r.t. each parameter already presented.

The mismatch contribution simulation in the Cadence environment reveals that less than 5% of the total offset comes from the trip point mismatch for DIGOTA, whereas in DB-OTA their contribution accounts for more than the 80%. Fig. 3.10a shows the input and output waveform in voltage follower configuration for a 100 samples MC analysis and Fig. 3.10b, the OTA offset voltage for the same study. No signal saturation is found, proving that the DIGOTA is more robust to process variations than DB-OTA, even working in weak inversion where the matching issues are more critical [196]. For the same MC analysis, THD, Power, DC gain and GBW are shown in Fig. 3.10c, Fig. 3.10d, Fig. 3.11a, and Fig.3.11b, respectively.

Regarding the impact of temperature, from Fig. 3.12 the DC gain A_{V0} is relatively independent of the temperature with a maximum fluctuation of 5 dB over the highest value of 34.3 dB. From the same figure, f_{GBW} increases exponentially at a rate α of 2.8%/^{o}C, where the exponential growth rate α is defined as:

$$\alpha = \left(\frac{f_{GBW}|_{T_1}}{f_{GBW}|_{T_0}} \right)^{\frac{1^\circ\mathrm{C}}{T_1 - T_0}} - 1 \tag{3.29}$$

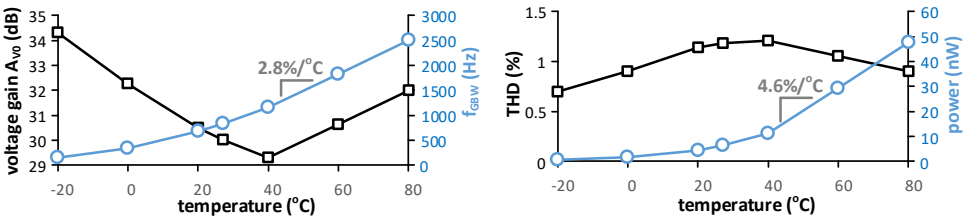


Fig. 3.12 [SIMULATIONS] Temperature dependence of DC voltage gain and gain-bandwidth product vs. temperature, total harmonic distortion and power.

in which $f_{GBW}|_{T_1}$, $f_{GBW}|_{T_0}$ are the f_{GBW} values at T_0=-20^{o}C and T_1=80^{o}C, respectively.

From the same Fig. 3.12, the total harmonic distortion (THD) is nearly independent of the temperature, due to the minor temperature effect on the static characteristics of CMOS logic gates. The power expectedly increases exponentially with the temperature at a rate of 4.6%/^{o}C defined as in Eq. (3.29), as determined by the adopted technology since leakage increases by the very same rate.

3.4 Measurements Results

The measured response of the DIGOTA circuit in the voltage follower configuration to sine and square wave inputs is shown in Fig. 3.13 under a 0.3-V supply generated directly by a mm-scale solar cell. The measurements in the following were carried out by setting the supply voltage with a source meter, to assure repeatable and well-defined testing conditions.

The DIGOTA open-loop frequency response is plotted in Fig. 3.14, as evaluated from testchip characterization and the model in Eq. (3.16). At the low voltage of 0.3 V and a heavy capacitive load of 150 pF, this figure shows a 30-dB DC gain, a 250-Hz gain-bandwidth product, and a 90^o phase margin. Fig. 3.14 shows good agreement between model and the measurements, with an average (maximum) error of 1.13dB (3.4dB) for the magnitude, and 4.6^o (11 ^{o}) degrees for the phase. For DC inputs, the measured CMRR is 41dB, whereas the measured PSRR is 30dB at the same 0.3-V supply. The open-loop output resistance r_{OUT} is 21MΩ.

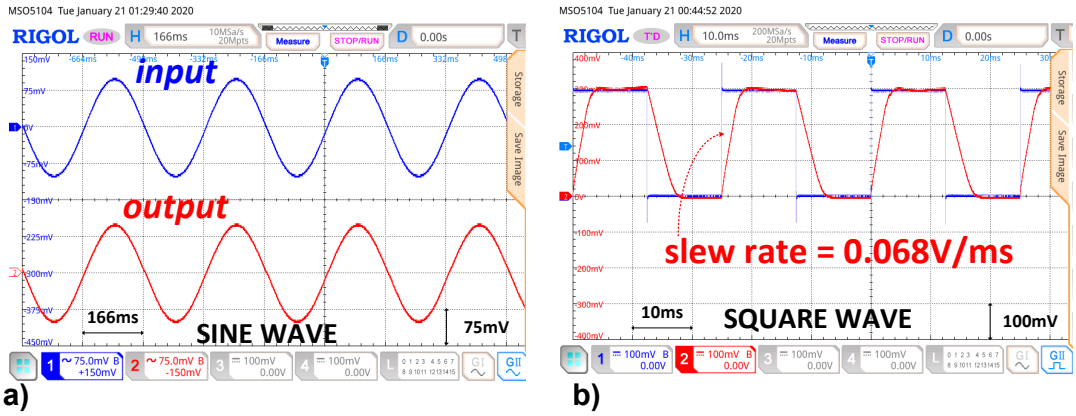


Fig. 3.13 [MEASUREMENTS] a) sine and b) square wave response when directly powered by a 1-mm2 solar cell at <100 lux (dark overcast day) (2.5-Hz frequency, 75-mV amplitude).

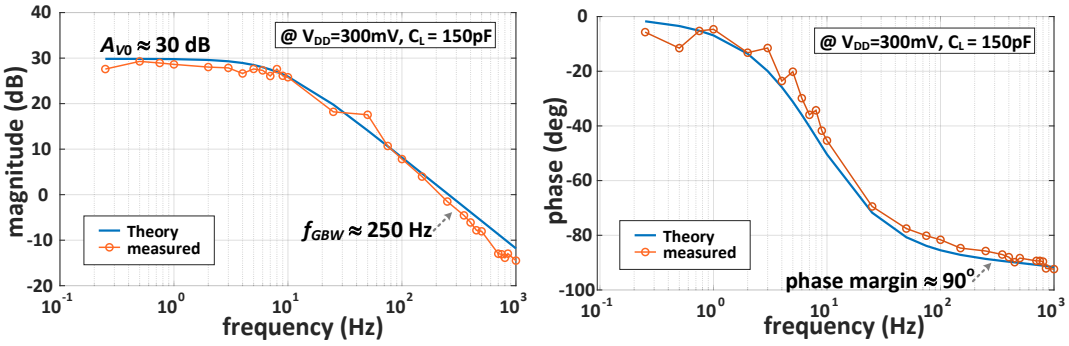


Fig. 3.14 [MEASUREMENTS] Open-loop frequency response at V_{DD}=0.3 V, C_L=150 pF: a) magnitude and b) phase from testchip measurements and model in Eq. (3.16).

The measured spectrum of the DIGOTA output for a 2.5-Hz sine wave with 75-mV amplitude is reported in Fig. 3.15, which shows the harmonics due to distortion and the out-of-band self-oscillation frequency tone at 8kHz. The resulting total harmonic distortion THD in Fig. 3.15 is less than 2% for input amplitudes exceeding 90% of the rail-to-rail swing, corresponding to 7-bit linearity (no noise included). The THD was found to slightly increase by 0.1% at higher frequencies. Hence, linearity sets the ultimate limit to the resolution of sensor interfaces based on DIGOTA, rather than noise.

The power consumption at 0.25-0.5 V supply and 150-pF capacitive load range from 850 pW to 107 nW, as plotted in Fig. 3.16a. The power model in Eq. (3.20) agrees with measurements with an average error of 9%. From the same figure,

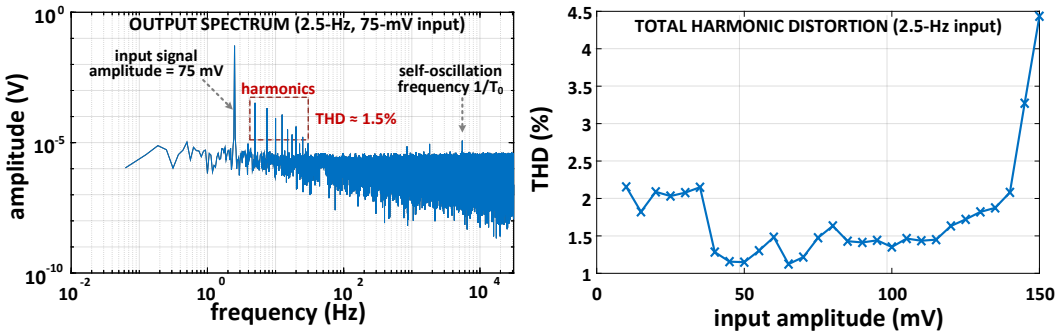


Fig. 3.15 [MEASUREMENTS] a) Output spectrum under sine wave input (2.5 Hz, 75-mV), b) THD vs amplitude under sine wave input (2.5 Hz), at V_{DD}=0.3 V, C_L=150 pF.

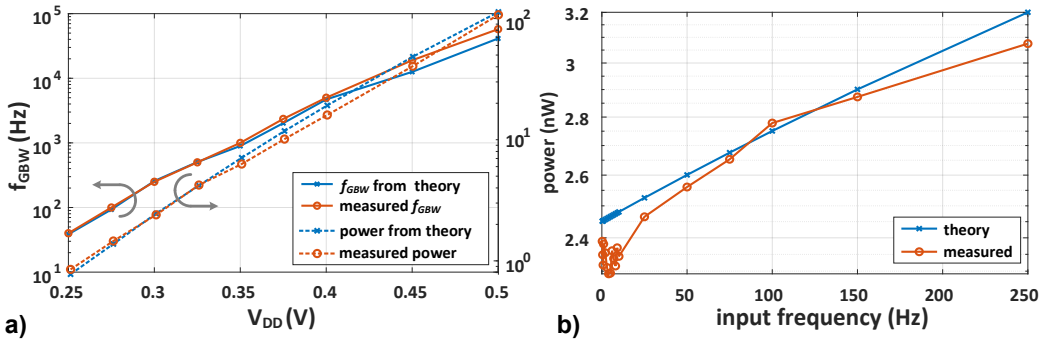


Fig. 3.16 [MEASUREMENTS] a) Power (Eq. (3.20)) and gain-bandwidth product (Eq. (3.19)) vs V_{DD}, b) power (Eq. (3.20)) vs input frequency (50-mV amplitude, V_{DD}=0.3V).

the gain-bandwidth product ranges from 40 Hz to 57.5 kHz, which is modeled by Eq. (3.20) with an average error of 15%. The exponential increase of power and f_{GBW} with V_{DD} in Fig. 3.16a is due to the exponential increase in the transistor sub-threshold current I_{ON} in Eq. (3.19), and consequently in the frequency $1/T_0$. Also, Fig. 3.16b shows the nearly-linear dependence of the power consumption on the input frequency f_S, as expected from the power contribution of the output stage in Eq. (3.20).

The resulting figures of merit FOM_S in Eq. (3.24) and FOM_L in Eq. (3.25) are in the 7.1-80.2 MHz$\cdot$pF/μW and 4.2-26.5 (V/μs)pF/μW range. The average error of the model in Eqs. (3.26) and (3.27) with respect to the measurements is respectively 25% and 12%. Regarding the voltage dependence, Fig. 11c confirms that FOM_S

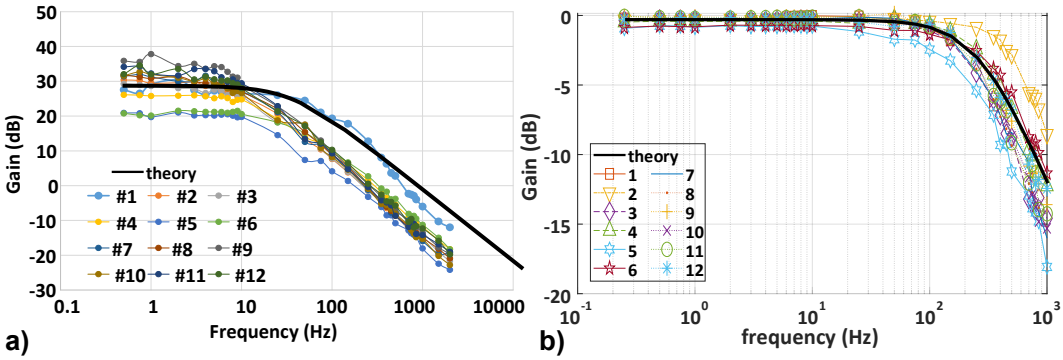


Fig. 3.17 [MEASUREMENTS] a) Magnitude Open-loop frequency response across twelve DIGOTA dices b) Magnitude response of the closed-loop transfer function of twelve DIGOTA dices in the voltage follower configuration.

is proportional to $e^{(2V_{DD}/(nkT/q))}/V_{DD}^2$ as in Eq. (3.26), and FOM_L is proportional to $e^{(2V_{DD}/(nkT/q))}/V_{DD}^2$ as in Eq. (3.27), at low voltages that keep transistors in the sub-threshold region.

The consistency of the above results under process variations was validated through the characterization of twelve DIGOTA die samples, as plotted in Fig. 3.17 for the open and closed-loop frequency response. At the voltage of 0.3 V and without the support of any bias circuitry, the mean value and standard deviation of the DC gain are respectively -0.33 and 0.23 dB (in closed-loop). The mean value and the standard deviation for the –3dB cutoff frequency are respectively 265 Hz and 99 Hz (closed-loop), leading to variability of 37%. This confirms reasonable consistency without the need for calibration, unlike previously proposed DB-OTA.

The gain-bandwidth product, the slew rate, and the power consumption for the measured samples are reported in Fig. 3.18. This figure confirms fairly consistent performance across dice, despite operation at very low voltage and the absence of a bias current reference. From Fig. 3.18, the variability of f_{GBW}, SR, and power is respectively 37.7%, 15.7%, and 34%. As a reference, the variability of the technology is quantified by the 51% variability of the FO4 delay at V_{DD}=0.3 V. Accordingly, the variability of f_{GBW}, SR, and power is lower than the FO4 variability, confirming the resilience of the DIGOTA architecture against process variations. At 0.5 V, the variability of f_{GBW}, SR, and power become 15%, 64%, and 30%, respectively.

The input offset voltage standard deviation across the twelve dice is 4.7 mV, from the available samples in Fig. 3.19a.

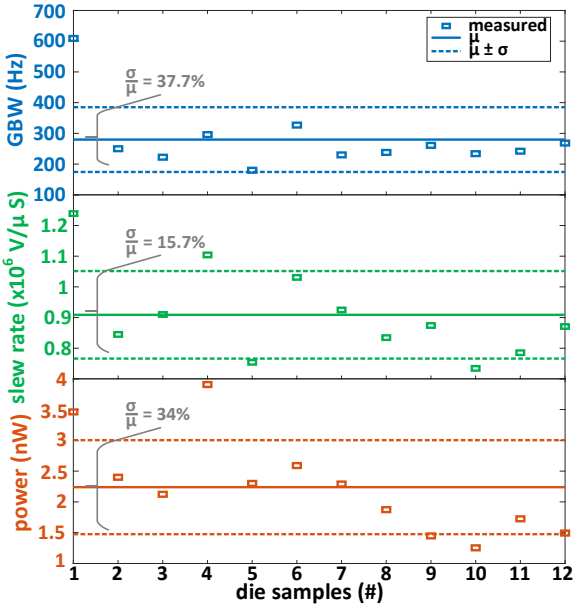


Fig. 3.18 [MEASUREMENTS] a) Measurement results across twelve dice and effect of process variations on gain-bandwidth product, slew rate and power consumption (V_{DD}=0.3 V).

The total harmonic distortion in Fig. 3.19b has a variability of 23.1-25.5%, across the range of moderate to large amplitudes, above 50 mV and up to 125 mV.

From Fig. 3.20, the large-signal and small-signal power efficiency figure of merit has a 23.3% and 29.6% variability, indicating that nearly power efficiency is fairly consistent across process variations.

The DIGOTA performance is compared with state-of-the-art ultra-low-voltage and ultra-low power OTAs in Table 3.2 (see Fig. 3.21). At the supply voltage of 0.3 V, DIGOTA operates at the nW-range power, which is at least an order of magnitude lower than prior art (nor counting DB-OTA). Such power is also efficiently used when driving heavy capacitive loads, as indicated by the small-signal FOM_S=15.6 $MHz \cdot pF/\mu W$, which is 1.5-34X better than prior OTAs operating in the same supply voltage range. As intrinsic limitations of DIGOTA, the DC gain is 19.8-30 dB lower than prior art and the CMRR is accordingly lower by 21.5-37 dB, the PSRR is 8-46 dB lower, and the THD is 1% higher.

The digital nature of DIGOTA reduces the area by 2-85X over prior art (not counting DB-OTA). Combining power and area efficiency, the area-normalized figure

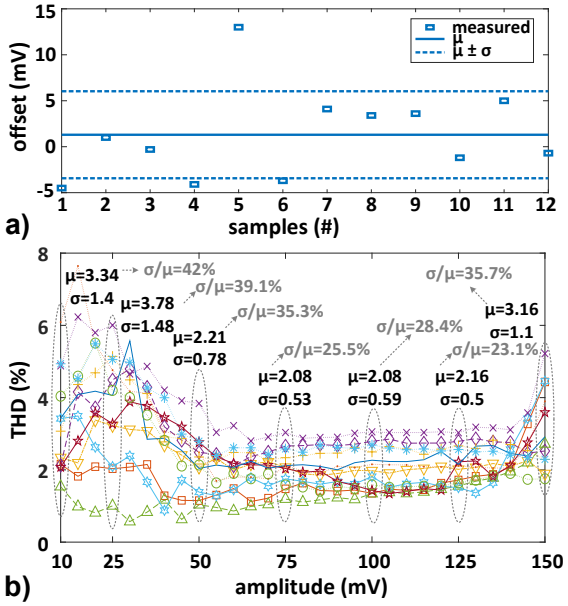


Fig. 3.19 [MEASUREMENTS] a) Measured input offset voltage of twelve DIGOTA dice and resulting mean value and standard deviation b) Measured total harmonic distortion (THD) of twelve DIGOTA dice, their mean value, and standard deviation vs input sinewave amplitude (2.5 Hz input, V_{DD}=0.3 V, C_L=150 pF).

of merit $FOM_{S,A}$ in Table 3.2 is improved by >6X. Similarly, the area-normalized large-signal figure of merit $FOM_{L,A}$ is improved by >9X, compared to the prior art in the same supply voltage range.

At 0.5 V, the DIGOTA performance improves to 73-dB DC gain, f_{GBW}=57.5 kHz, and 19 V/ms slew rate. The PSRR is increased to 50 dB. Compared to OTAs with much higher supply in the 1.1-2 V range, Table 3.2 shows that DIGOTA still maintains the second-best FOM_S and $FOM_{L,A}$, and the best $FOM_{S,A}$.

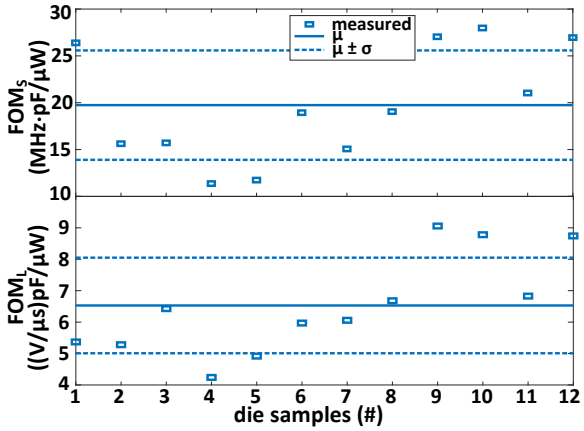


Fig. 3.20 [MEASUREMENTS] Measured figures of merit FOM_S and FOM_L across DIGOTA dice. Power has been measured for sine wave (2.5 Hz input, V_{DD}=0.3 V, C_L=150 pF) .

Table 3.2 PERFORMANCE COMPARISON WITH STATE-OF-THE-ART OTAS (**BEST PERFORMANCE IN BOLD**)

	$V_{DD} < 500mV$					$V_{DD} > 500mV$				
	[1]	[2]	[8]	[4]	**This work**	[5]	[6]	[7]	[8]	**This work**
V_{DD} [V]	0.5	0.3	0.25	0.25	0.3	1.1	1.2	2	0.9	0.5
$V_{DD,MIN}$ [V]	0.45	0.3	**0.25**	**0.25**	**0.25**	1.1	1.2	2	0.9	**0.25**
design	custom	custom	custom	custom	**std cell**	custom	custom	custom	custom	**std cell**
OTA architecture	bulk-driven	gate-driven	bulk-driven	bulk-driven	digital	PSS amplifiers	Miller	folded Cascode	bulk-biased	digital
ext. CR needed (Y/N)	Y	**N**	Y	Y	**N**	Y	Y	Y	Y	**N**
technology [nm]	180	130	130	65	180	180	180	500	350	180
area [mm^2]	26,000	-	83,000	2,000	**982**	2,100	13,000	30,000	14,000	**982**
normalized area (10^3F^{-2})	802.47	-	4,911	473	30.3	64.81	401.23	120	114.28	30.3
C_L [pF]	20	2	15	15	150	100	18,000	70	10	150
power [μW]	110	1.8	0.018	0.026	**0.0024**	7.4	69.6	100	18.9	0.1075
DC gain [dB]	52	49.8	60	70	30	**100**	**100**	76.8	65	73
GBW [kHz]	2,500	**9,100**	1.88	9.5	0.25	1,660	1,180	3,400	1,000	57.5
ave. slew rate SR [$V/\mu s$]	2.89	3.8	0.0007	0.002	0.000085	8.67	0.22	**19.25**	0.25	0.019
input noise [μV]	442.7	105.6	143	-	**21**	-	-	42.41	65	122
CMRR [dB]	78	-	-	62.5	41	-	-	**112**	45	65
PSRR [dB]	76	-	-	38	30	-	-	**92**	50	50
THD [%]	1	-	1	-	2	-	-	-	0.2	1
FOM_S	0.45	10	1.6	5.48	15.6	22.4	**305.2**	2.4	0.52	80.2
FOM_L	0.52	4.2	0.58	1.15	5.3	**117.2**	56.9	13.5	0.13	26.5
$FOM_{S,A}$	17.3	-	19	2,750	15,885	10,666	23,477	80	37.15	**81,724**
$FOM_{L,A}$	20.2	-	7	575	5,397	**55,792**	4,377	450	9.45	27,000
passives needed	Y	**N**	Y	Y	**N**	Y	Y	Y	Y	**N**

[1][181]+, [2][31]*, [3][30]+, [4][192]+, [5] [197]+, [6] [198]+
[7] [199]+, [8] [200]+,+Experimental, *Simulation

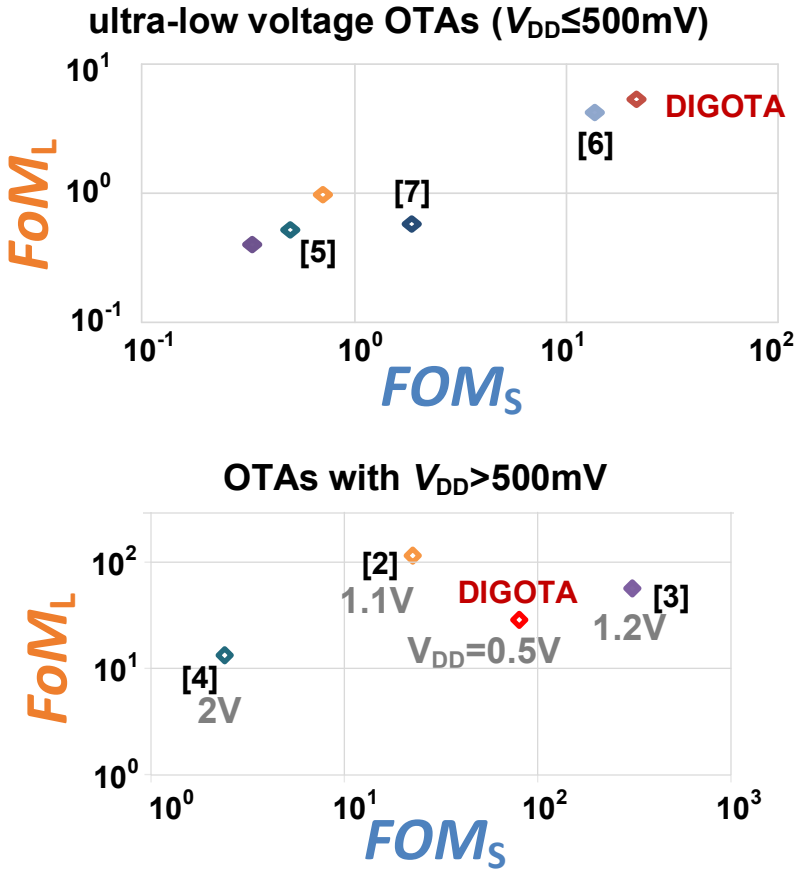


Fig. 3.21 [MEASUREMENTS] FOM_S and FOM_L energy efficiency: comparison with OTAs with V_{DD}<500mV and V_{DD}>500mV.

Chapter 4

Digital-Based Biosignal Amplifier

The OTAs presented in chapters 2 and 3 have been mainly conceived to explore the implementation of analog functions by digital blocks and the potential of such an approach. In this chapter, the new concepts are applied in a biomedical signal amplifier. Considering the advantages in terms of area and power, the digital-based design methodology can be valuable in the biomedical field to enable *Body Dust* applications [38]. Being *Body Dust* as one of the biomedical applications which demands the lowest area and power, the DIGOTA is then chosen as a building block to be part of a biomedical amplifier.

Body Dust, which refers to envisioned drinkable, autonomous bio-electronic circuits with dimensions suitable to be internalized into the human body to sense and transmit clinical pieces of information, is emerging as the new frontier of electronics for biomedical applications [37, 38] (see Fig. 4.1). The concept of Smart Dust has been proposed and investigated in deep over the last 20 years. Even though the very first paper about this subject was presented at a conference held in 1999 [201], the first real device was just demonstrated in the body of mammalian in 2016 [202]. The presented device is still reasonably large with respect to the typical sizes promised in this area of research (typically, sub-mm devices).

Concentrating on the analog signal acquisition, the stringent requirements in terms of low noise and distortion need to be met under ultra-low area, low voltage, and power consumption restrictions. In particular, these constraints are hard to be achieved by analog, and mixed signal circuit design techniques at the state of the art [203, 40, 41, 204–208]. For instance, *Body Dust* ICs for temperature [209], pH

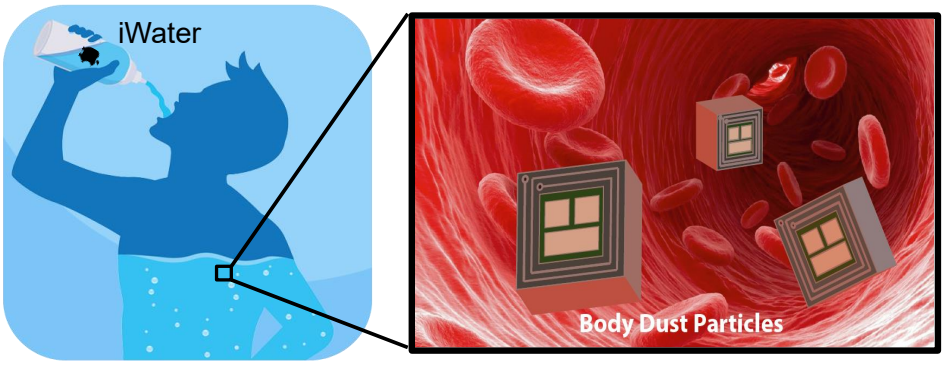


Fig. 4.1 Body dust illustration [37, 38].

SPECIFICATION		TYPICAL	COMMENT
Recording performance	Noise (μV rms)	< 5	Including both electrode and instrumentation noise
	Bandwidth (Hz)	1–3,000	Broadband to include local-field-potential (LFP) and extracullar action potential (EAP) signals
	dc rejection (mV)	> 100	Offset across different electrodes
	DR (dB)	> 50	Relating to the front-end amplifier, data converter
	CMRR (dB)	> 70	For interference/stimulation artefact suppression
	PSRR (dB)	> 70	Voltage regulation can relax this requirement
	Input impedance (Ω)	> 5M	Large compared to the electrode impedance
Resource per channel	Area (mm^2)	0.01–0.1	To allow for large channel counts
	Power (μW)	10	Limited by heat dissipation in tissue

PSRR: power supply rejection ratio; CMRR: common mode rejection ratio; DR: dynamic range.

Fig. 4.2 Typical requirements for Bioelectronic Interfaces [39].

[42] and drugs/biomarkers concentration [210] monitoring applications demand sub-$0.1mm^3$ silicon volume (mainly due to its own application nature), which accordingly constrains the available harvested power (state-of-the-art human body-based thermal and vibration energy harvesters offering $7.4\mu W/cm^3$ power density [211] translate to sub-nW power for 0.1 mm^3 silicon volume. See also Fig. 1.12 for a more general view). In [39], Fig. 4.2 illustrates the typical requirements for bio-electronic interfaces.

In this chapter, a digital-based fully differential amplifier for biomedical signal processing (BioDIGOTA) circuit is proposed based on the single-ended DIGOTA topology of chapter 3. The necessary modifications to achieve fully-differential operation and meet the biosignal acquisition requirements are explored and explained. The DIGOTA concept described in chapter 3 is exploited to design a fully differential biosignal amplifier targeting the requirements of electrocardiogram (ECG) ampli-

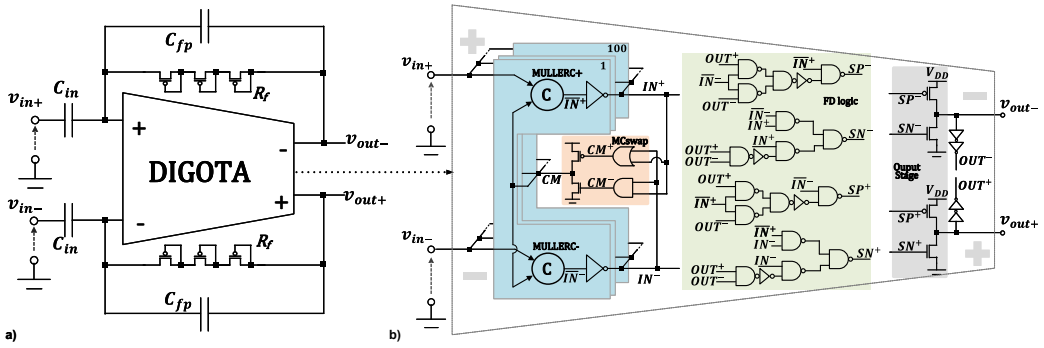


Fig. 4.3 a) BioDIGOTA schematic b) Fully differential DIGOTA.

fication [203, 40, 41, 204–208], whose schematic is shown in Fig 4.3a and whose design is described next.

The chapter organization follows a similar structure as seen in the previous ones. Circuit analysis and design is shown in section 4.1.1. Its layout is depicted in section 4.2, followed by simulation results in section 4.3, and measurements in section 4.4.

4.1 Circuit Design and Analysis

4.1.1 Circuit Analysis

The proposed fully-Differential (FD) BioDIGOTA includes a FD noise-optimized version of the DIGOTA presented in Chapter 3, as detailed in Fig. 4.3b, and an on-chip capacitive feedback network (C_{in},C_{fp},R_{f} shown in Fig. 4.3a) implemented by Metal-insulator-Metal (MiM) capacitors and MOSFETs as pseudo-resistors.

Aiming to allow FD operation, the proposed FD-DIGOTA includes a Muller-C-based input stage, two inverters, and an MCswap common-mode compensation stage analogous in concept to the corresponding blocks of the single-ended version. But its output stage is now comprised of two three-state inverters so that to generate the positive and negative output voltages $v_{\text{out}+}, v_{\text{out}-}$.

The two inverters of the BioDIGOTA output stage are digitally operated both to amplify the differential input voltage and to keep the common-mode output voltage constant. For this purpose, they are driven based on the digital signals IN^+, IN^-, equivalent in concept to $(\overline{\text{MUL}+}, \overline{\text{MUL}-})$ in the single-ended version presented in

Table 4.1 Fully-Differential DIGOTA Combinational Logic Truth Table

DIGITAL INPUTS				DIGITAL OUTPUTS					
IN^+	IN^-	OUT^+	OUT^-	CM^+	CM^-	SP^+	SN^+	SP^-	SN^-
0	0	0	0	ON	OFF	ON	OFF	ON	OFF
0	0	0	1	ON	OFF	OFF	OFF	OFF	OFF
0	0	1	0	ON	OFF	OFF	OFF	OFF	OFF
0	0	1	1	ON	OFF	OFF	ON	OFF	ON
0	**1**	0	0	OFF	OFF	OFF	ON	ON	OFF
0	**1**	0	1	OFF	OFF	OFF	ON	ON	OFF
0	**1**	1	0	OFF	OFF	OFF	ON	ON	OFF
0	**1**	1	1	OFF	OFF	OFF	ON	ON	OFF
1	**0**	0	0	OFF	OFF	ON	OFF	OFF	ON
1	**0**	0	1	OFF	OFF	ON	OFF	OFF	ON
1	**0**	1	0	OFF	OFF	ON	OFF	OFF	ON
1	**0**	1	1	OFF	OFF	ON	OFF	OFF	ON
1	1	0	0	OFF	ON	ON	OFF	ON	OFF
1	1	0	1	OFF	ON	OFF	OFF	OFF	OFF
1	1	1	0	OFF	ON	OFF	OFF	OFF	OFF
1	1	1	1	OFF	ON	OFF	ON	OFF	ON

section 3.1, and based on the additional digital signals OUT^+ and OUT^-, obtained by two digital buffers driven by the analog outputs $v_{\text{out}+}$ and $v_{\text{out}-}$, respectively, so that OUT^+ (OUT^-), is high or low when the corresponding analog output voltage $v_{\text{out}+}$ ($v_{\text{out}-}$) is above or below the trip point $V_{\text{T}} \simeq V_{\text{DD}}/2$. The operation of the two output buffers and of the MCswap stage based on the IN^+, IN^-, OUT^+ and OUT^- digital signals is defined as in the truth table reported in Tab.4.1 and is described next.

Whenever $IN^+ \neq IN^-$ (highlighted in bold in Tab.4.1), the sign of the differential input signal can be detected and amplified, and the output stages are operated accordingly. In details, if $IN^+ = 1$ and $IN^- = 0$ ($IN^+ = 0$ and $IN^- = 1$), the pull-up device of the buffer driving the non-inverting (inverting) output is operated, whereas the pull-down device of the buffer driving the inverting (non-inverting) output is operated, so that to increase (decrease) the differential output component $v_{\text{d,out}} = v_{\text{out}+} - v_{\text{out}-}$, regardless the OUT^+ and OUT^- values. In the meantime, the MCswap block is kept inactive (i.e., in a high impedance state).

On the other hand, when $IN^+ = IN^-$ and the sign of the differential input signal cannot be detected, the *MCSwap* stage is activated as in the single-ended DIGOTA circuit, and the output common mode signal is also corrected, if needed. In particular, when $OUT^+ = OUT^- = 0$ ($OUT^+ = OUT^- = 1$), the *output stages* are activated so that to increase (decrease) both the output voltages $v_{\text{out}+}$ and $v_{\text{out}-}$ at the same time, as needed to enforce a common-mode output voltage closer to $V_{\text{DD}}/2$. By contrast, whenever $OUT^+ \neq OUT^-$, which implies that the CM output voltage differs from $V_{\text{DD}}/2$ by less than one half of the output differential signal $v_{\text{d,out}}$, both the output stages are kept in a high impedance state.

In essence, from the truth table 4.1 it is observed that whenever IN^+ and IN^- are logically equal, the input common-mode is always compensated as in the single-ended DIGOTA circuit, whereas the output common-mode component is either increased or decreased if OUT^+ and OUT^- are (0,0) or (1,1), and CM output stage is kept at high impedance only when OUT^+ and OUT^- is (1,0) or (0,1). For the sake of completeness, the Boolean equations for each gate of each output stage are:

$$SP^+ = \overline{IN^+} \cdot OUT^+ + IN^- + \overline{IN^+} \cdot OUT^- = \overline{\overline{\overline{IN^+} \cdot OUT^+} \cdot \overline{IN^-} \cdot \overline{\overline{IN^+} \cdot OUT^-}} \tag{4.1}$$

$$SN^+ = \overline{IN^+} \cdot IN^- + IN^- \cdot OUT^+ \cdot OUT^- = \overline{\overline{\overline{IN^+} \cdot IN^-} \cdot \overline{IN^- \cdot OUT^+ \cdot OUT^-}} \tag{4.2}$$

$$SP^- = \overline{IN^-} \cdot OUT^+ + IN^+ + \overline{IN^-} \cdot OUT^- = \overline{\overline{\overline{IN^-} \cdot OUT^+} \cdot \overline{IN^+} \cdot \overline{\overline{IN^-} \cdot OUT^-}} \tag{4.3}$$

$$SN^- = \overline{IN^-} \cdot IN^+ + IN^+ \cdot OUT^+ \cdot OUT^- = \overline{\overline{\overline{IN^-} \cdot IN^+} \cdot \overline{IN^+ \cdot OUT^+ \cdot OUT^-}} \tag{4.4}$$

In the case of CM^+ and CM^-, they follow the same logic as given by Eqs. (2.4) and (2.5), respectively.

4.1.2 Circuit Design

For biosignal amplification, the noise generated by the DIGOTA must be reduced. Then a noise-optimized version of DIGOTA should be designed. Based on the modeling approach adopted for the single-ended DIGOTA circuit in chapter 3 and assuming the circuit is working in weak inversion (Low $V_{\mathrm{DD}}s$), the DIGOTA noise performance is dominated by the shot noise from the input devices within the Muller-C stage, where the in-band integrated input noise is given by

$$\overline{v_{\mathrm{IN}}^2} = 2\pi \frac{2qI_{CM}}{g_m^2} f_{BW} \tag{4.5}$$

where q is the electrical charge, I_{CM} is defined in Eq. (3.9), g_m is the muller-C weighted transconductance defined in (3.10), and f_{BW} is the amplifier bandwidth.

The Noise Efficiency Factor (NEF), described in Eq. (4.6), is a well-known metric to quantify the performance of low noise amplifiers for biomedical applications [39].

$$NEF = v_{\mathrm{IN,RMS}} \sqrt{\frac{2I_{\mathrm{D}}}{\phi_{\mathrm{T}} 4k_{\mathrm{B}} T \pi f_{BW}}} \tag{4.6}$$

where ϕ_{T} is the thermal voltage, k_{B} is the Boltzmann constant, T is the temperature, and I_{D} is current consumption.

Once the DIGOTA is designed to reduce the total noise, most of the power is consumed in the first stage ($I_D \approx I_{CM}$) given by Eq. (4.7) and its g_m is given by Eq. (4.8) for weak inversion regime.

$$I_D = \frac{Power}{V_{DD}} = \frac{2C_{MUL}V_{DD}}{T_0} \tag{4.7}$$

$$g_m = \frac{I_D}{n\phi_T} \tag{4.8}$$

Substituting Eqs (3.8) for $\tau_{INV} = \tau_{MCswap} = 0$, (4.7) and (4.8) in (4.5) and after in (4.6), we have

$$NEF_{DIGOTA} \approx n \tag{4.9}$$

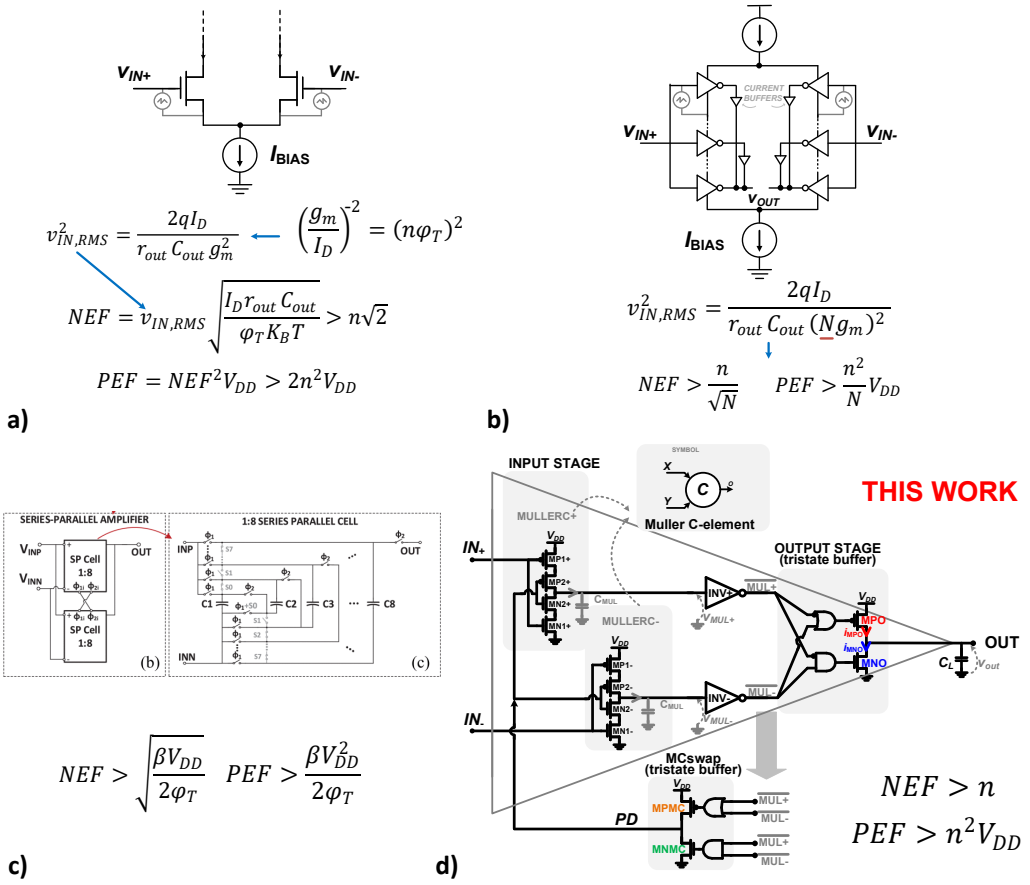


Fig. 4.4 a) NEF and PEF for differential pair, b) for stacked inverter-based [40], c) Switched-capacitor [41], and d) digital based amplifier of section 2.

Fig. 4.4 compares NEF and the power efficiency factor $PEF = NEF^2 V_{DD}$ of current state of the art of low frequency and low noise CMOS amplifier solutions. Among them, the discrete-time low-noise amplifier made by switched-capacitors achieves the best NEF and PEF at the cost of a big silicon area [41]. In [40], current reused is implemented to increase the equivalent transconductance by N stacked inverters and, then, the final NEF is reduced by $\sqrt{N}$. However, the later of approach limits the minimum V_{DD}. In the case of the proposed BioDIGOTA, the NEF is equivalent to the stacked inverters for $N = 1$, but no any bias circuit is needed, the circuit is compatible to digital flow, and the total silicon area is further reduced.

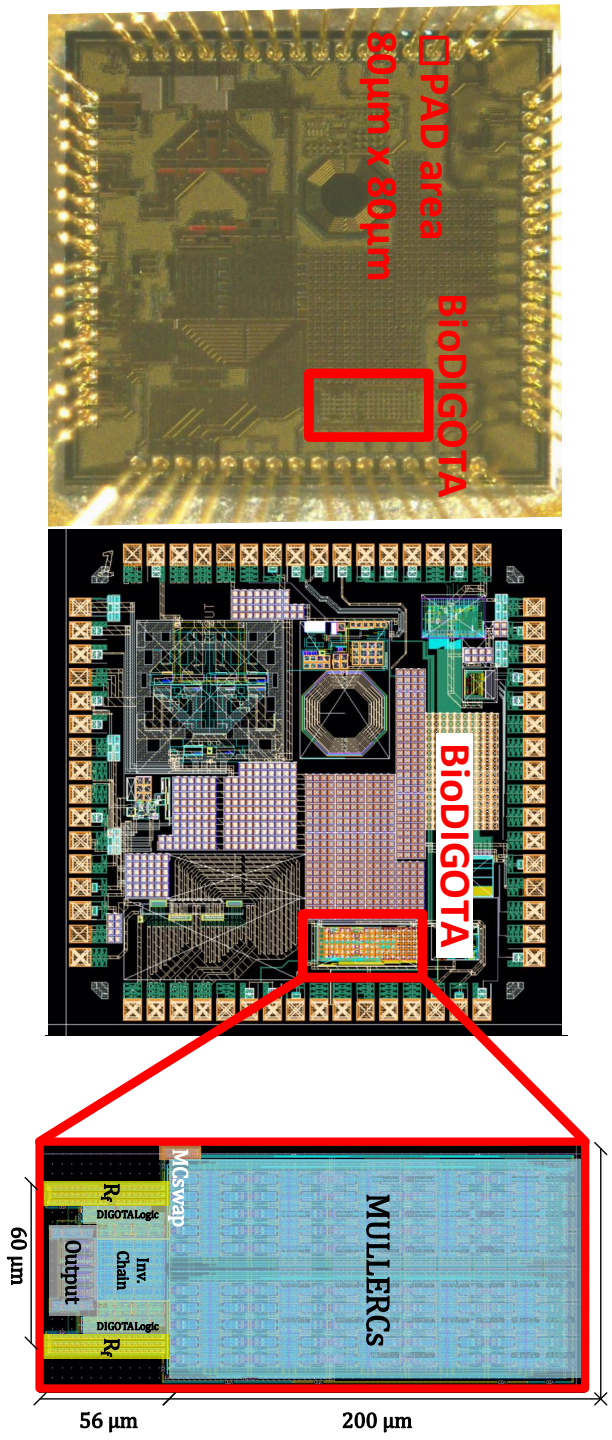


Fig. 4.5 BioDIGOTA final layout in CMOS 180nm and chip picture.

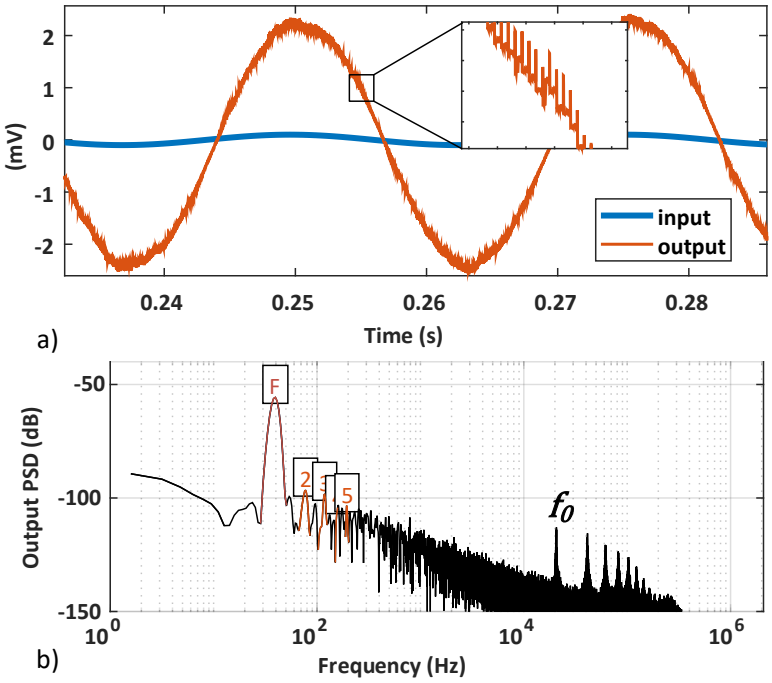


Fig. 4.6 [SIMULATIONS] a) BioDIGOTA transient response. b) Wide spectrum density for output signal from b) for input amplitude of 100 μV at 40 Hz.

4.2 Layout

The proposed FD BioDIGOTA has been designed and fabricated in 180nm CMOS, and its layout is shown in Fig. 4.5 along with its micro-photo. Once most of the noise contribution is related to the input stage, its design has deserved special care to meet the requirements of biomedical signal amplification. For this purpose, the area of the Muller-C is increased one hundred times to reduce noise by connecting one hundred cells in parallel.

The delays of the non-inverting and inverting signal paths have been matched. The active components have been integrated under the MiM capacitors to reduce the layout area further. The circuit layout occupies just 0.022 mm^2, thus achieving 3.322X lower silicon area compared to the minimum size found in the current literature [206]. In Fig. 4.5, the area breakdown shows that the MullerC logic-gates occupy more than 50% of the area. At the same time, almost 40% of the total is

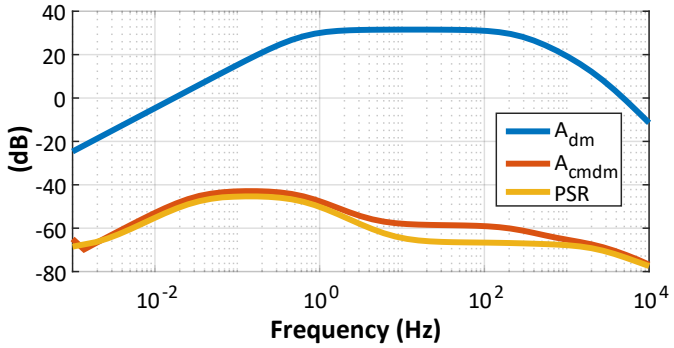


Fig. 4.7 [SIMULATIONS] BioDIGOTA frequency response.

covered by the MiM capacitors of the feedback network. In other words, only 0.018 of 0.022 mm^2 are dedicated to the active devices, including the pseudo-resistors.

4.3 Simulations Results

The time-domain input and output waveforms of the proposed BioDIGOTA at $V_{DD} = 300$mV, with sine wave input at 40Hz frequency, 100 μV peak amplitude and $C_{out} = 20$pF capacitive load are reported in Fig.4.6 and reveal the operation of the circuit as an opamp with less than 2% THD and 150nW of power consumption. A zoom in the output waveform shows the step-wise changes in v_{out} resulting from its intrinsically digital operation [35, 159, 25]. The wideband output spectrum is reported in Fig.4.6b, revealing in-band harmonics (THD=1.5%) and the out-of-band self-oscillation frequency tone at $f_0 \approx 18$kHz.

The circuit frequency response and noise power spectral density (PSD) have been verified by PSS+PAC+PNoise analysis [212] in view of its circuit digital operation, where its linearization is performed around its natural self-oscillation frequency f_0. The ULV BioDIGOTA frequency response reported in Fig.4.7 exhibits 30dB in-band gain and 270Hz bandwidth (BW) under $C_{out} = 20$pF load. In the same plot, the common mode to differential mode (CM-DM) frequency response along with PSR are also depicted showing a CMRR and PSRR of 77 and 80 dB, respectively. Fig. 4.8 shows the power spectral density of the input-refereed noise, revealing an integrated

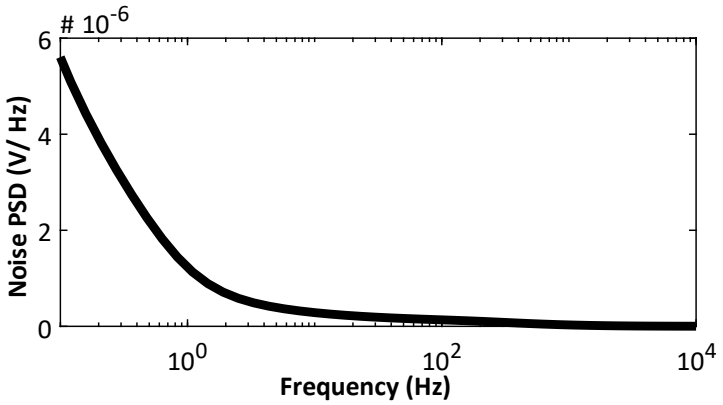


Fig. 4.8 [SIMULATIONS] BioDIGOTA Noise spectrum density.

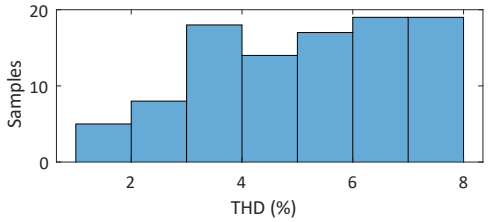


Fig. 4.9 [SIMULATIONS] THD Histogram (μ=5.13% and σ=1.74%) for N=100 samples and input amplitude of 100 μV.

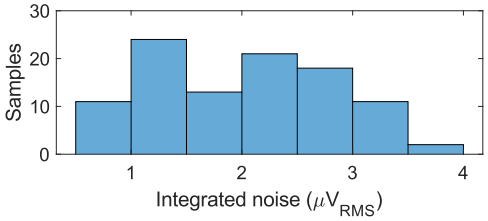


Fig. 4.10 [SIMULATIONS] Integrated Noise Histogram (μ=1.97μV_{RMS} and σ=0.813μV_{RMS}) for N=100 samples and BW from 0.01Hz to 10kHz.

noise of 3.1 μV_{RMS} over the BW from 0.01Hz to 10kHz or 31 nV/$\sqrt{Hz}$ average PSD over the same BW.

Before the tapeout, the BioDIGOTA has been verified under process variations for $V_{\text{DD}} = 300mV$ by Montecarlo (MC) simulations performed on 100 samples and the output THD has been considered in order to evaluate the signal quality degradation. The output THD for an input amplitude of 100 μV histogram reported in Fig.4.9 reveals a mean value of $\mu = 5.13\%$ and standard deviation of $\sigma = 1.74\%$,

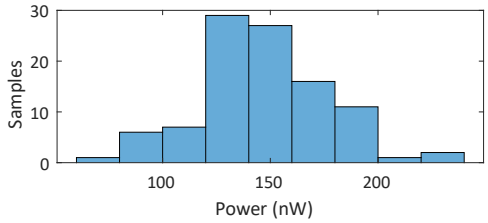


Fig. 4.11 [SIMULATIONS] Power Histogram (μ=146nW and σ=29nW) for N=100 samples.

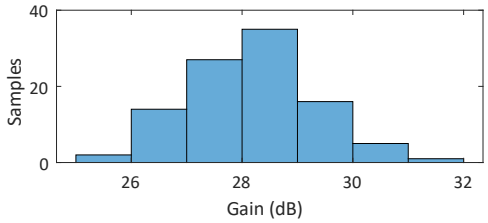


Fig. 4.12 [SIMULATIONS] Gain Histogram (μ=28.2dB and σ=1.13dB) for N=100 samples.

i.e., $\frac{\sigma}{\mu} = 34\%$. Noise is also an relevant specification for low bio-potential signals and the integrated noise histogram is plotted in Fig. 4.10, achieving $\frac{\sigma}{\mu} = 41\%$. Power and middle-band gain histograms are also reveled in Fig. 4.11 and 4.12, reaching $\frac{\sigma}{\mu} = 20.1\%$ and $\frac{\sigma}{\mu} = 4\%$, respectively.

4.4 Measurements Results

Three BioDIGOTA samples have been measured, and their performance has been compared with biosignal amplifiers presented in recent literature. The 3Hz frequency time-domain input and output measured waveforms of the proposed FD BioDIGOTA at $V_{DD} = 400$mV and $C_{out} = 10$pF capacitive load are reported in Fig.4.13b and reveal the operation of the circuit as a filter with less than 2% THD and 100nW power consumption for an input amplitude of 3.5 mV. A voltage gain of 35 dB has been estimated for this configuration. The power breakdown is also included in the Fig.4.13a. A relevant power is consumed in the first stage, as expected, to reduce the noise. The wide-band output spectrum is reported in Fig.4.13c, revealing in-band harmonics (THD=1.8%). Table 4.2 shows THD measured for all three samples.

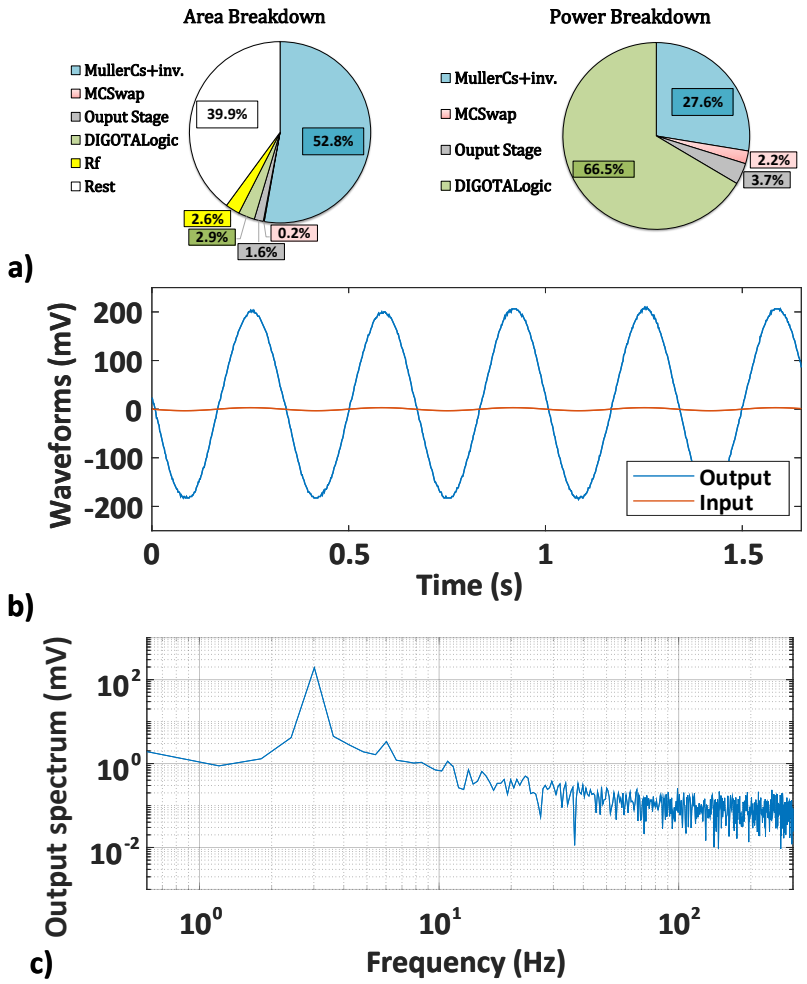


Fig. 4.13 a) Area breakdown and power breakdown of BioDIGOTA b) input and output waveforms and c) Wide spectrum density for output signal for input amplitude of 3.5 mV at 3 Hz.

The measured frequency response of the BioDIGOTA differential amplification is reported in Fig.4.14a and reveals 35dB in-band gain and 10 Hz bandwidth under $C_{\text{out}} = 10$pF load. In the same plot, the common-mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR) are also depicted, revealing a CMRR exceeding 62dB and a PSRR exceeding 55 dB in the signal bandwidth for the best sample (sample #3).

Fig.4.15 shows the measured power spectral density of the input-refereed noise for the three samples. The BioDIGOTA integrated noise over the entire bioDIGOTA

Table 4.2 Measured performance for all three samples @ V_{DD} =400mV, 27 ^{o}C temperature, input amplitude of 3.5mV and frequency of 3 Hz.

Sample Number #	THD (%)	Power (nW)	Gain (dB)	Noise (μV_{RMS})	NEF	PEF
1	1.7	100.84	34.3	2.52	15.69	98.49
2	1.25	78.63	36.84	2.13	11.73	55
3	**1.8**	**95**	**35**	**1.25**	**7.59**	**23**

The measured results of sample #3 (bold) are also presented in the comparison table (Table 4.3).

Table 4.3 Performance Summary and Comparison **(BEST PERFORMANCE IN BOLD)**

Performance	[208]	[204]	[205]	[213]	[207]	[206]	[40]	[41]	[214]	[215]	**This work***	Unit
Design strategy	Analog	Analog	Analog	Analog	Analog	Analog	Analog	Analog	Analog	Analog	**Digital**	-
Technology	180	65	65	180	180	40	180	180	180	130	180	nm
Supply Voltage	0.2/0.8	0.6	0.6	1	0.45	1.2	1.35	1	1	1.2	**0.4**	V
Die Area	1	0.2	0.6	0.29	0.25	0.071	0.24	2.33	0.19	0.1	**0.022**	mm^2
Power	790	**1**	16.8	250	730	2,000	18.7	620	800	35,800	95	nW
Gain	58	32	**51-96**	25	52	26	36	22.3	40.4	39.3	35	dB
BW	670	370	250	10,000	10,000	5,000	240	5,000	5,000	**100,000**	10	Hz
CMRR	85	60	80	84	73	-	**95**	91.8	58	86	62	dB
PSRR	74	63	67	76	80	-	68	**83**	54	67	55	dB
THD	0.3	-	2.8	-	0.53	**0.02**	0.16	0.025	1	1	1.8	%
Input-Referred Noise	36	1,400	253	43	29	40	158	**11.85**	59.18	13	395	$nV/\sqrt{Hz}$
NEF	2.1	2.1	2.64	1.07	1.57	4.9	0.86	**0.45**	2	2.5	7.6	-
PEF	1.6	2.64	4.1	1.14	1.12	28	0.99	**0.2**	4	7.5	23	V
$NEF_{AREA} = NEF \times Area_{mm^2}$	2.1	0.42	1.58	0.31	0.39	0.35	0.2064	1.045	0.38	0.25	**0.15**	mm^2
$PEF_{AREA} = PEF \times Area_{mm^2}$	1.6	0.528	2.46	0.33	0.28	1.98	**0.238**	0.466	0.76	0.75	0.46	$V \cdot mm^2$

bandwidth (0.05 Hz - 10 Hz specify the bandwidth here) is $1.25\mu V_{\mathrm{RMS}}$, corresponding to a 395 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ average PSD over the same bandwidth for sample #3. Power, NEF, and PEF are listed for all samples in Table 4.2. Amongst all samples, the lowest NEF and PEF found are 7.6 and 23, respectively, for the sample #3.

Compared to biosignal amplifiers proposed in recent literature [203, 40, 41, 204–208], whose performance is summarized in Tab. 4.3, the BioDIGOTA presented here is able to work properly at the lowest V_{DD} (2X lower than [204, 205]), at the lowest silicon area (3.22X lower than [206]), keeping acceptable noise performance. These results prove that digital-based analog design is very attractive for body dust applications. The comparison in terms of NEF and PEF versus area is also illustrated in Fig. 4.16. If the NEF and PEF are both multiplied by the total area as shown in Tab. 4.3 by NEF_{AREA} and PEF_{AREA}, the proposed BioDIGOTA achieves the lowest NEF_{AREA}. These measurements results gathered from the proposed BioDIGOTA demonstrate a relevant power-efficiency and area reduction, as previously predicted in Fig. 1.17b.

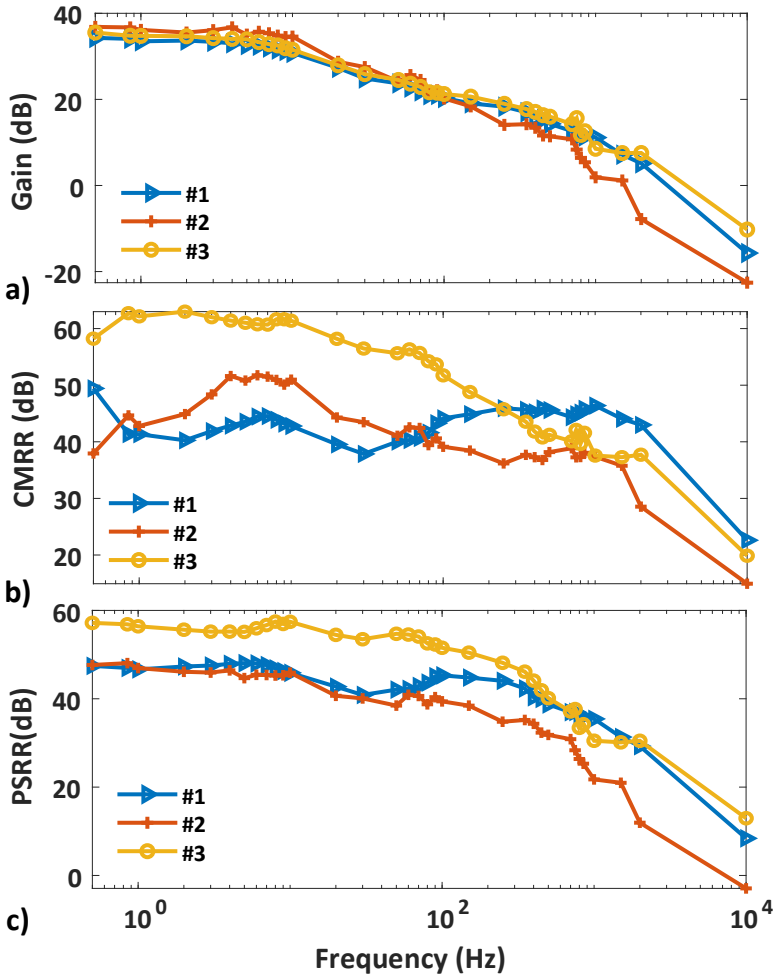


Fig. 4.14 Gain, CMRR and PSRR at $V_{\mathrm{DD}} = 400mV$.

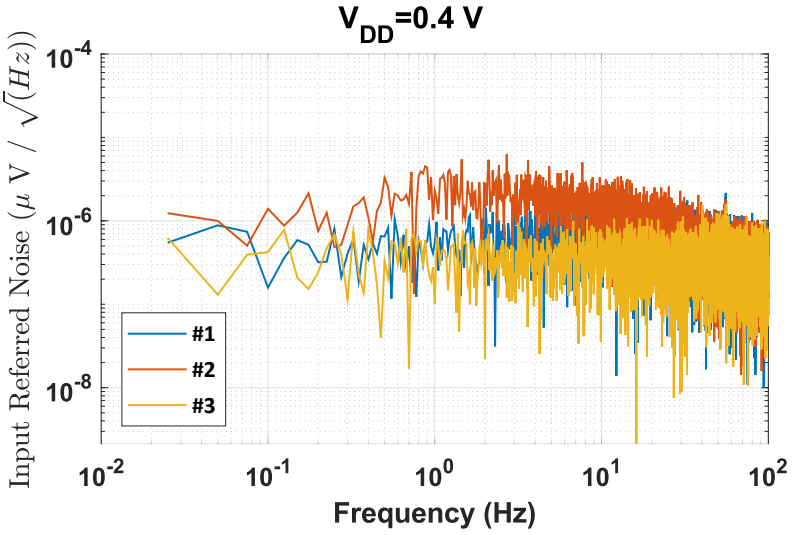


Fig. 4.15 BioDIGOTA measured noise spectrum density for each sample over entire bandwidth at $V_{\mathrm{DD}} = 400mV$.

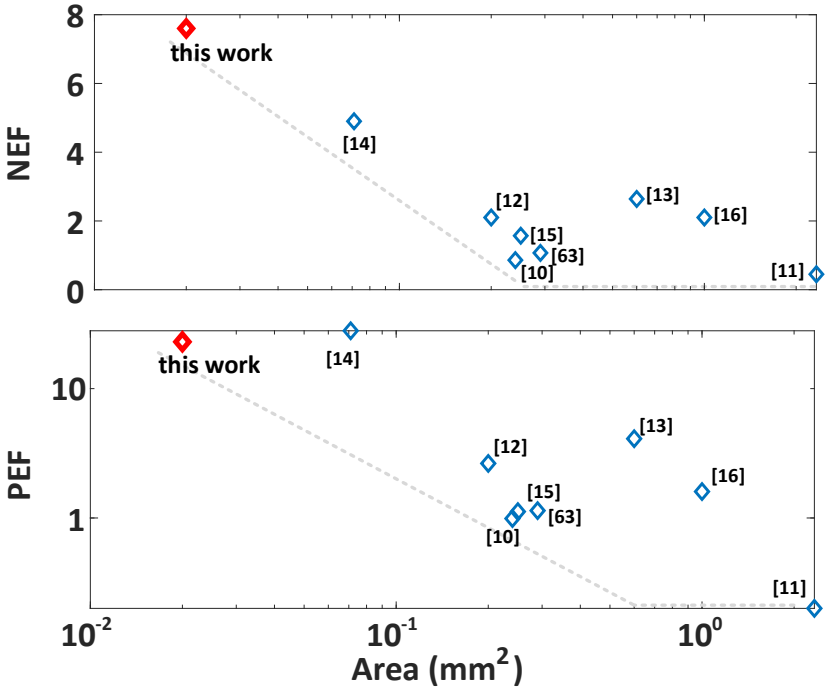


Fig. 4.16 NEF and PEF versus Area.

Chapter 5

Conclusion

Despite the intrinsically analog and smooth perception of our surrounding environment, the achievements of science and technology in the last two centuries have extensively shown that in-depth analysis, which appears to be continuous, proves to be discrete in various forms. The matter is composed of atoms, and all fundamental physical quantities from electric charge to electromagnetic field and angular momentum are also quantized. Not only the inanimate world proves to be discrete, but also in animals and humans. Their information is processed and transmitted as discrete pulses, as discovered and modeled by Hodgkin and Huxley [216]. Then, we may conclude that our everyday life analog feeling is based on an underlying discrete structure.

C.E.Shannon, in his groundbreaking work [217], shows that the *information* is discrete in itself. The maximum amount of data that can be reliably transferred in the unit time (expressed in bit/s) is finite and upper-bounded by the channel capacity $C = B\log_2(1+S/N)$ [217], regardless of whether analog signals or digital signals are adopted. Shannon's reasoning, however, does not apply just to computers and communication networks. They also suit any kind of information, including information processed in sensors, actuators, interfaces, and analog circuits like OTAs and voltage references. This thesis suggests that even these circuits could better understand the discrete nature of information and that digital circuits can perform their functions.

The thesis claims that a "digital revolution" in analog blocks is now happening, and it can be clearly observed in recent publications appearing in analog blocks

ranging from PLLs to voltage references. This shift in the analog/RF design approach is here defined as **Digital-in-Concept Design Methodologies (DCDM)** trend. Furthermore, the thesis demonstrates that the DCDM approach is significantly attractive to IoT applications, coping with two crucial challenges of the next-generation IoT ecosystem: silicon area and power consumption on the edge devices. Such challenges are deeply investigated in chapter 1, examining the entire IoT technological stack and its applications.

Taking advantage of information processing in time domain and digital automated design techniques related to DCDM, two digital OTAs and a bio-signal amplifier have been proposed and validated in silicon.

As the first contribution, silicon demonstration, measurement results, and a qualitative circuit analysis have been presented for a highly digital, ultra-low voltage, and ultra-low power OTA (DB-OTA). By processing the analog input signal digitally via conventional standard cells, the measured power efficiency achieved at V_{DD}=300 mV is quantified by the classical FOM_S figure of merit to be 2,101 V^{-1}, which outperforms the state of the art thanks to the lowest power of 591 pW. DB-OTA measurements also show DC gain and gain-bandwidth between 29 and 31 dB and 229 and 528 Hz, respectively, for 80pF of output load, always keeping THD below 3%. Its area of 1,426 μm^2 is also close to best-in-class. To the best of this thesis author's knowledge, DB-OTA is the first and only sub-nW OTA to date.

Next, a compact and energy-efficient passive-less digital OTA has been proposed and demonstrated in 180 nm. The proposed DIGOTA exhibits a power 2.4nW power consumption (one of the lowest in the literature) and the lowest area (982 μm^2) , and operates down to 250 mV, even if its dc gain, PSRR, CMRR and bandwidth are lower compared to other ultra-low voltage OTAs. At 300 mV, the best figure of merits (such as $FOM_{S,A}$ and $FOM_{L,A}$) are achieved among sub-500-mV OTAs thanks to the improved energy and area efficiency, reaching DC gain and gain-bandwidth of 30 dB and between 200 and 350 Hz for 150pF of output load, respectively. At 500-mV supply, the energy efficiency is still competitive with the previously proposed OTAs operating at above 1-V supplies. The ability to operate at ultra-low voltage and power has been demonstrated in the context of energy-autonomous sensor nodes, as directly powered by a small energy harvester (7 mm^2 solar cell) at dim light <100 lux (dark overcast day).

The BioDIGOTA, i.e. a fully differential digital-based OTA targeting biomedical signal acquisition, is finally presented in this thesis. Such a front-end shows a lower silicon area than its analog counterpart when operating in ULV and ULP conditions. The proposed BioDIGOTA architecture can be implemented using CMOS digital standard cells, available in any fabrication process. The proposed ULV BioDIGOTA has achieved at $V_{DD} = 400\,mV$ a good figure of merits (such as NEF = 7.6 and PEF = 23), while consuming just 95 nW and 0.022 mm^2 of silicon area with 35 dB gain and 395 $nV/\sqrt{Hz}$ power spectral density. Through this implementation, digital-based analog design has been proven to be a good alternative for reducing area, power, and design effort for IoT applications like body dust working in the low voltage domain.

5.1 Future work

There is undoubtedly much work to be done in DCDM or digital-based analog processing: from the architecture perspective to the building block point of view. As shown in Fig. 1.16, digital-based analog and RF processing has become an emerging area of research, and its advantage in the area and power consumption has been showing appealing in IoT applications. Based on the building blocks designed in this thesis, this thesis author lists below some further research challenges to be addressed in future work:

- both proposed digital OTAs have low DC gain as their major drawback. Multi-stage architectures and/or custom output stage, containing for instance Composite Transistors (CT) [218] structures, can be used to boost the final DC gain. Note that the later strategy does not fit into standard-cell-based flow;
- the herein proposed OTAs could be included in several analog systems (e.g., continuous-time sigma-delta ADC [31]), not only using the static CMOS family as used here but using other types like Schmitt-Trigger Logic [219];
- emerging semiconductor devices (flexible technologies, for instance) or ultra-scaled FinFETs or GAAFETs could be used to design digital OTAs and compare with the traditional approach. Their scaliability and reconfigurability could also be investigated;

- from the design flow and EAD perspective, even though the OTAs are digital design flow compatible, they will be used as a building block of a complete analog system, which likely would contain passive devices requiring certain symmetry constraints and requirements. To include such components and rules, the author of the thesis envisions a near future the union between the current automated analog layout synthesis (ALS) [111–114, 39, 115–117] with the current digital design flow, at which mainly guided by digital flow the main building blocks would be standard-cell-based and ALS would be responsible for completing the rest of analog system. In other words, ALS would be included as a feature within the digital design flow backed up by several digital-based analog building blocks, like the ones presented here;

- from a simulation and verification point of view, an analog block/system will always need to be verified using an analog solver once their input and output signal must be continuously monitored to check their final performance. The author of this thesis does not see any improvements to decrease the simulation time of digital-based analog blocks compared to the pure digital ones, where a digital simulator can be used to speed up the verification and static time analysis (STA) to verify the reliability of the circuit.

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Appendix A

Published Papers and Awards

Published Papers regarding the thesis subject:

- **P. Toledo**, P. S. Crovetti, H. D. Klimach, F. Musolino and S. Bampi, "Low-Voltage, Low-Area, nW-Power CMOS Digital-Based Biosignal Amplifier," in IEEE Access, vol. 10, 2022, doi:10.1109/ACCESS.2022.3168603.
- **P. Toledo**, P. Crovetti, O. Aiello and M. Alioto, "Design of Digital OTAs With Operation Down to 0.3 V and nW Power for Direct Harvesting," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 9, pp. 3693-3706, Sept. 2021, doi: 10.1109/TCSI.2021.3089339.
- **P. Toledo**, H. Klimach, S. Bampi and P. Crovetti, "A 300mV-Supply, 144nW-Power, 0.03mm2-Area, 0.2-PEF Digital-Based Biomedical Signal Amplifier in 180nm CMOS," 2021 IEEE International Symposium on Medical Measurements and Applications (MeMeA), 2021, pp. 1-6, doi: 10.1109/MeMeA52024.2021.9478709.
- **P. Toledo**, P. Crovetti, H. Klimach, S. Bampi, O. Aiello and M. Alioto, "A 300mV-Supply, Sub-nW-Power Digital-Based Operational Transconductance Amplifier," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 9, pp. 3073-3077, Sept. 2021, doi: 10.1109/TCSII.2021.3084243.
- **P. Toledo**, R. Rubino, F. Musolino and P. Crovetti, "Re-Thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era,"

in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 3, pp. 816-822, March 2021, doi: 10.1109/TCSII.2021.3049680.

- **Toledo, P.**; Crovetti, P.; Klimach, H.; Bampi, S. Dynamic and Static Calibration of Ultra-Low-Voltage, Digital-Based Operational Transconductance Amplifiers. Electronics 2020, 9, 983. https://doi.org/10.3390/electronics9060983

- **Toledo, P.** Crovetti, H. Klimach and S. Bampi, "A 300mV-Supply, 2nW-Power, 80pF-Load CMOS Digital-Based OTA for IoT Interfaces," 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2019, pp. 170-173, doi: 10.1109/ICECS46596.2019.8965062.

- **P. Toledo**, O. Aiello and P. S. Crovetti, "A 300mV-Supply Standard-Cell-Based OTA with Digital PWM Offset Calibration," 2019 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), 2019, pp. 1-5, doi: 10.1109/NORCHIP.2019.8906958.

- Crovetti, P., Musolino, F., Aiello, O., **Toledo, P.** and Rubino, R. (2019), breaking the boundaries between analogue and digital. Electron. Lett., 55: 672-673. https://doi.org/10.1049/el.2019.1622

Published Papers about other topics but published during Ph.D's Degree period:

- T. Bradde, S. Grivet-Talocia, **P. Toledo** et al., "Fast Simulation of Analog Circuit Blocks Under Nonstationary Operating Conditions," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 11, no. 9, pp. 1355-1368, Sept. 2021, doi: 10.1109/TCPMT.2021.3099215.

- O. Aiello and **P. Toledo**, "Temperature Characterization of a Fully-synthesizable Rail-to-Rail Dynamic Voltage Comparator operating down to 0.15-V : (Invited paper)," 2021 19th IEEE International New Circuits and Systems Conference (NEWCAS), 2021, pp. 1-4, doi: 10.1109/NEWCAS50681.2021.9462749.

- O. Aiello, P. Crovetti, **P. Toledo** and M. Alioto, "Rail-to-Rail Dynamic Voltage Comparator Scalable Down to pW-Range Power and 0.15-V Supply," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 7, pp. 2675-2679, July 2021, doi: 10.1109/TCSII.2021.3059164.

- T. Bradde, **P. Toledo**, M. De Stefano, A. Zanco, S. Grivet-Talocia and P. Crovetti, "Enabling fast power integrity transient analysis through parameterized small-signal macromodels," 2019 International Symposium on Electromagnetic Compatibility - EMC EUROPE, 2019, pp. 759-764, doi: 10.1109/EMCEurope.2019.8871828.
- L. H. Rodovalho, **P. Toledo** and S. Bampi, "A 0.6 V Current Reference Based on the MOSFET Forward-Body-Biased ZTC Condition," 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2019, pp. 290-293, doi: 10.1109/ICECS46596.2019.8964641.
- **P. Toledo**, D. Cordova, H. Klimach, S. Bampi and P. S. Crovetti, "A 0.3–1.2 V Schottky-Based CMOS ZTC Voltage Reference," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 10, pp. 1663-1667, Oct. 2019, doi: 10.1109/TCSII.2019.2932281.

Prizes:

- 2021 Pre-Doctoral Grants from the IEEE Circuits and Systems Society
- Finalist of the Huawei Italy University Challenge 2021 in IC Design track
- 3rd Best Ph.D. Student of the Year, 2021, Electrical, Electronics and Communications Engineering Ph.D. Prize, Doctoral school of Politecnico di Torino
- Best Student Paper Award, 2019, IEEE International Conference on Electronics, Circuits and Systems (ICECS 2019)