Junction Temperature Estimation Via Plug-In System for the Design Validation of IGBT Industrial Power Converters

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Matteo Gregorio, *Student Member, IEEE,* Fausto Stella, *Member, IEEE,* Radu Bojoi, *Fellow, IEEE,* and Fabio Pagani, *Member, IEEE*

***Abstract*—In the design process of power electronics converters, the power semiconductors thermal modelling is one of the most critical tasks. An accurate estimation of the junction temperature allows the validation of the converter design and also the calibration of the thermal models during prototyping. Therefore, this paper presents a straightforward method to estimate the junction temperature directly on the target converter using a plug-in measurement system. The estimation is based on the IGBT on-state voltage measurement under high current with a dedicated sensing circuitry externally connected to the converter under test. This solution is specifically designed to fulfill the needs during the prototyping process and design validation since allows a fast and reliable monitoring in all working conditions of interest and the sensing circuitry does not affect the normal operation of the converter under test (CUT). The acquisition circuitry and the calibration procedure are described and tested on a 68 kVA IGBT industrial three-phase inverter. The experimental results obtained on the target inverter prove that the proposed design validation based on the implemented estimation of the junction temperature provides better results than the conventional design methods based on thermal models implemented in simulators.**

***Index Terms*—Power converter design, IGBT power modules, junction temperature estimation, thermal modelling.**

I. Introduction

NOWADAYS power electronics converters are used in a wide range of applications requiring high efficiency, power density and reliability. Being the thermal heat dissipation ability the most limiting factor [1], all these targets are possible only with a proper thermal management at both system and components levels [2], [3]. As reported in [4], the temperature is one of the major root causes of failure and semiconductors and capacitors are the most vulnerable parts showing failure mechanism correlated to their average working temperature and thermal swing [3]. Moreover, the continuous demand in cost reduction can only be obtained with a retrenchment of safety margins during the design process, affecting any longer negatively the power converter reliability. Consequently, many attempts have been made by power modules manufacturers to develop packaging techniques able to mitigate the failure mechanisms and to improve the thermal dissipation capacity [5]–[7]. On the other hand, power converters designers must optimize the overall system performance via optimization algorithms [8]. The converter design starts first with the evaluation of voltage and current stress of power devices, based on the converter topology and the worst-case operating condition. Afterwards, the power semiconductors losses and thermal model for the cooling system are evaluated to translate the operating conditions into a temperature profile [9], [10]. Therefore, a prerequisite to get junction temperature estimation is the knowledge of the loss model and the thermal model. The first can be obtained by the parameters provided by manufacturers in datasheet [11]. Nevertheless, often those parameters are representative of specific working conditions that not necessarily correspond to the actual one. Otherwise, they can be extracted by means of an experimental characterization as double pulse test (DPT) test [12], but accurate measuring of the power switches currents and voltages to evaluate the switching losses is difficult and requires a dedicated test rig that is usually implemented by the manufacturers of the power modules.

Similarly, thermal models of power modules are provided by the manufacturers in datasheet [13]. However, these thermal models are often inaccurate since they refer to a single switch in the module and do not take into account the thermal coupling between the devices inside the module. Furthermore, these parameters are usually conservative, leading to an overestimation of the junction temperature. Improved thermal models like the ones presented in [14]–[17] can be used to overcome the above limits. Conversely, these models rely either on numerical methods to solve thermal problems, as finite-element simulation (FEA), or to experimental characterization. In the former case, a comprehensive knowledge of the power module in terms of layout, material composition and dimensions, is essential. However, all these parameters are not always available. In the latter case, a dedicated test rig is mandatory to characterize the thermal impedance of each device at a time. In both procedures, the output is a matrix of impedance that correlates the losses with the junction temperature and its dimension depends on the number of devices.

In all these cases, the estimated junction temperature is affected by uncertainties that could limit the effectiveness of the models. Therefore, it is essential to validate the expected temperature during the prototype validation phase by directly measuring the semiconductors temperature. Hence, the aim of the paper is to propose a plug-in board and a test procedure for the junction temperature estimation of IGBT power modules employed in any industrial converters without integrated sensing circuitry. The estimation of the junction

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temperature is based on the on-state collector-emitter voltage detection at high collector currents using the plug-in board. Thereby, the junction temperature can be estimated during the converter operations and so the module thermal management and expected performance can be validated during prototyping [18].

The main advantages of the proposed technique compared to the state-of-the-art solutions currently available in literature [19]–[22] are:

- The proposed system is a plug-in solution that does not require any hardware modification of the CUT power layout.
- The proposed system for temperature estimation requires only one simple modification of the converter under test control firmware. In particular, the control firmware needs an additional state that is used to obtain the ON-state conduction voltage.
- The ON-state conduction voltage calibration is a simple and non-invasive procedure.
- Differently from other solutions, the proposed approach can use external sensing making the final results independent of the accuracy of the current sensors already installed on the power converter under test [23], [24].

This paper is an extension of the work presented in [25], and brings in added value by including:

- The proposed plug-in system for junction temperature estimation has been implemented on an industrial power converter, demonstrating its feasibility for the design validation of a real product.
- Extended experimental results for DC and AC operating conditions demonstrating the fast and reliable approach in the design validation process.
- A comparison of the estimated junction temperature with the predicted during the converter design phase by a classical method based on parameters provided in datasheets.

The paper is organized as follows: *Section II* presents a review of the junction temperature estimation methods and that one adopted in this paper, *Section III* describes the target converter employed as a case study and introduces the fundamental steps of the proposed method, namely calibration, data analysis and estimation. *Section IV* explains the calibration process, *Section V* defines how the results of the calibration process are manipulated to obtain a 2D look-up table employed for temperature estimation, while *Section VI* shows the experimental results. *Section VII* shows a comparison between the experimentally estimated junction temperatures with the results of the simulated thermal model based on the datasheet dataset. *Section IX* presents the conclusion of the paper.

II. Review of junction temperature measurement methods

As the most common way to measure a temperature within a power module is to use thermistors or thermocouples, the manufacturers usually integrate thermistors as NTC or PTC inside the power modules. However, this solution provides a measure that can be far from the real junction temperature of each switch due to the remoteness of the thermistor and therefore is more representative of the case temperature [26]. For this reason, the methods able to estimate directly the junction temperature are of great interest.

Several methods are well known in both literature and industry [27] such as optical methods, physical contact methods and electrical methods.

Optical methods [28] are based on sensors such as optical fibers and infra-red camera. The infra-red camera can provide a temperature map of the whole module and therefore can detect both the hot spot and the average temperature of each die, and the spatial resolution is high [29]. Furthermore, high current devices are distinguished by a substantial number of bond wire connections. In those components the image of the infrared camera is not directly usable due to the shading effect of the bonding wire that can affect the average temperature [30]. In contrast, the optical fibres can detect the temperature of a low spatial region and so in presence of a large surface die area they provide a punctual value that is no longer the average of the switch. However, in both solutions the dielectric gel inside the module has to be removed as the die must be seen by the optical sensor. Therefore, high voltage operation is not guaranteed anymore. For this reason, the optical methods fit well during the thermal model characterization but cannot be adopted for the prototype validation.

Physical contact methods [31] use sensors as thermocouples applied directly on the die surface. Despite their good precision, it is not trivial to guarantee the electrical insulation between the dies and the sensor while ensuring a good thermal coupling. Furthermore, their bandwidth is related to the size. To increase the bandwidth a low size chip is required leading to a punctual temperature estimation. As the introduction of the thermal sensor can strongly affect the reliability of the power device, this solution is usually avoided for industrial products.

Electrical methods take advantage of the component itself by exploiting the correlations among the junction temperature and the thermo-sensitive electrical parameters (TSEPs) [32], [33] as the ON-state voltage, the internal gate resistorR_{Gi} [34], the saturation voltage $V_{CE,sat}$ [35], and the threshold voltage V_{TH}. Thereby, the junction temperature estimation is simply performed using voltage and current probes, without intrusive modifications inside the module. However, the electrical methods have some drawbacks. As example, the estimated temperature represents the area average value inside the die [36] and therefore no information about the peak temperature can be extracted. Moreover, for high current devices consisting of paralleled dies, there is no chance to assess the temperature distribution among them. Depending on the adopted TSEPs, there are strong variations in terms of linearity, sensitivity, calibration process and easiness of implementation. Despite of their drawbacks, the electrical methods represent an attractive solution for industrial applications, where the optical and physical contact methods are often impracticable.

Among all the TSEPs, the ON-state voltage monitoring under high current working conditions is the most effective solution for the following reasons:

1) Temperature estimation is available at high current conditions when the thermal models need to be validated.

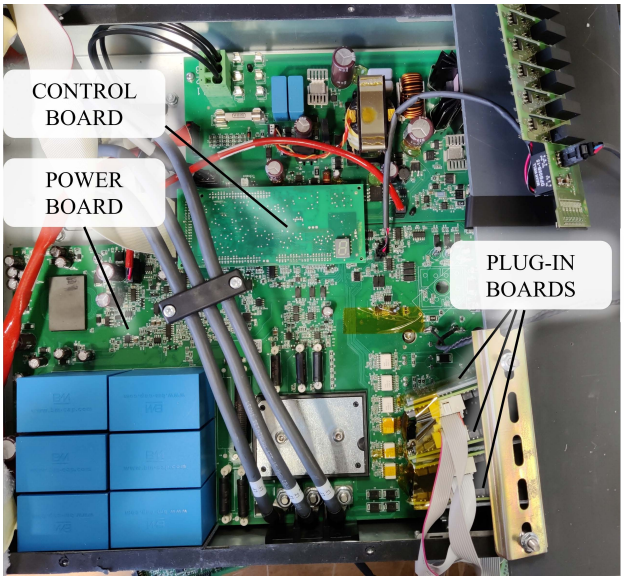

Fig. 1. Overview of the power converter with its final layout. The supplementary hardware includes the six plug-in boards implementing the ON-state voltage acquisition circuitry.

2) Acquisition of the ON-state voltage and current, thus directly measuring the semiconductors conduction losses.
3) The IGBT driver circuits are not altered.
4) The ON-state voltage measurement is the unique additional circuitry since the current measurement can be made with the already existing current sensor integrated in the converter.

In the literature, several solutions about the integration of the sensing circuitry in the gate driver of the converter are reported [19], [37], [38]. However, these options are not feasible for industrial products. The temperature estimation must be performed for any industrial converter with no need of dedicated gate drivers and other integrated sensing devices; therefore, the auxiliary circuitry can be an add-on component, externally plugged into the converter.

For all these reasons and to the best of the authors knowledge, the ON-state voltage is one of the solutions that best fits with the requirement of the junction temperature estimation during the converter design validation and therefore has been adopted for temperature estimation on an industrial power converter (currently in production) that is described in the next section.

III. Target Power Converter

In this paper, an industrial three-phase IGBT converter has been taken as target converter. The converter under study is shown in Fig. 1.

A plug-in board for each switch under test is connected directly to the main pin of the module under test (MUT) that is shown in Fig. 2, emphasizing the high-side (UH) and low-side (UL) IGBTs of inverter phase U, as well as the NTC. The plug-in board embeds the V_{CE} and V_{GE} voltage measurement circuit and therefore has to be located as close as possible to the MUT, in order to minimize the connecting cable thus reducing the measuring noise. The main features of the converter and the module under test are listed in Table. Ia and Table. Ib.

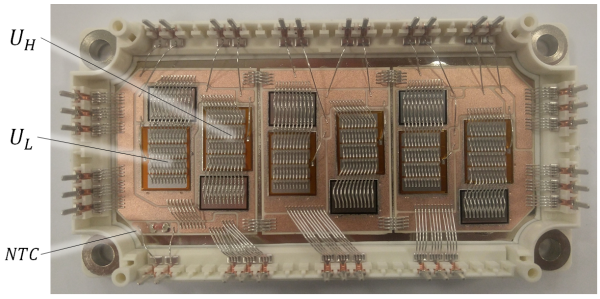

Fig. 2. Module under test (MUT).

TABLE I. Converter and module ratings at case temperature of 25°C

(a)

Converter		
S_{nom}	68	kVA
V_{dc}	400-700	V
f_{sw}	4	kHz

(b)

Module		
V_{CES}	1200	V
I_C	200	A
V_{GE}	$\pm$20	V
T_{Jop}	-40 to +150	$°C$
$V_{CE,sat}$@200A	1.70	V

In the following sections the plug-in board with the dedicated voltage measurement circuitry and the proposed procedure for the temperature estimation are described. As depicted in Fig. 3, the method consists of three different steps: calibration, data analysis and temperature estimation. It is worth noticing that the IGBT gate voltage is sampled to ensure the same driving voltage in both the calibration and the temperature estimation phase.

IV. Calibration Process

The aim of the calibration process is the extraction of the $V_{CE,i}$ ($I_{C,i}$, $T_{j,i}$) maps, where $V_{CE,i}$, $I_{C,i}$ and $T_{J,i}$ are respectively the ON-state voltage, the current and the junction temperature of the $i-$th IGBT from the module under test.

The calibration process is performed directly on the 3-phase power converter embedding the power module under test. The converter load is a dedicated three-phase inductor and the ON-state voltages V_{CE} and the gate-emitter voltages V_{GE} of the devices are measured with six external boards communicating with a MCU board, as shown in Fig. 4.

The calibration process consists of the ON-state voltage measurement during a sequence of three current ramps. The sequence is shown in Fig. 5, and for each current ramp two devices at a time are characterized, thereby the MUT can be identified with three ramps. By repeating this procedure at different heatsink temperatures the module can be fully characterized.

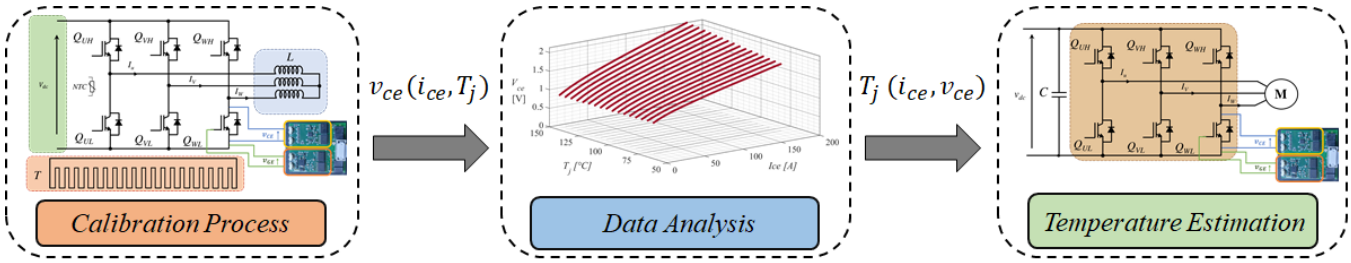

Fig. 3. Steps for the junction temperature estimation: calibration, data analysis and real-time estimation.

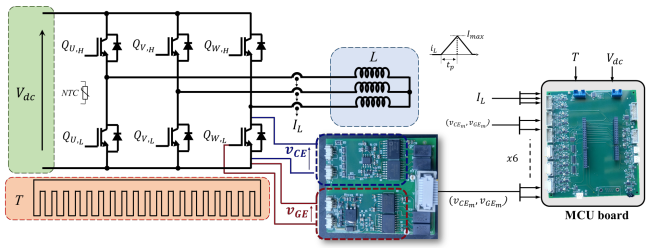

Fig. 4. Schematic of the proposed calibration setup. The pictures of the boards are respectively in the middle the plug-in board and on the right the external MCU-board for the V_{CE} and V_{GE} acquisitions.

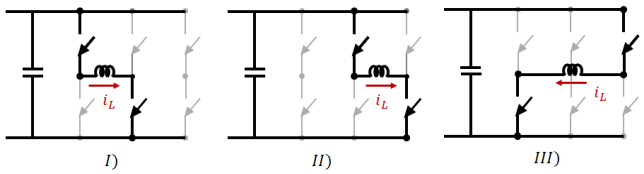

Fig. 5. Schematics of current ramps: pulse I) characterization of devices UH, VL; Ramp II) characterization of devices VH, WL; Ramp III) characterization of devices WH, UL.

The calibration process can be described in the following steps:

1) *Heating Phase:* The heatsink is heated up until the maximum temperature needed is reached.
2) *Current Ramp Phase:* A current ramp is set for each device of the MUT, so $V_{CE,i}$,$I_{C,i}$ can be measured.
3) *Cooling Phase:* the heatsink is cooled down to the following target temperature.

Steps 2 and 3 are repeated until the lowest target temperature is reached.

The process is summarized in Fig. 6, as depicted the ascending part of the current ramp allows the IGBTs characterization while the descending parts their relatives freewheeling diodes FWDs. Given the ramp time t_p, the peak current ramp value I_{max} depends on the input supply voltage V_{dc} and the inductance value L. The V_{dc} and L shall be properly selected according to specific criteria illustrated in the following section.

The main challenges of the current ramp phase are the on-state voltages and temperatures measurement. A further issue is introduced by the MUT internal layout since their parasitic resistances and inductances impose strict constraints during the current ramp phase. Therefore, the on-state voltages measurement, the temperatures measurement, the MUT internal layout effect and the data results of the calibration process are described in detail in the following parts of the paper.

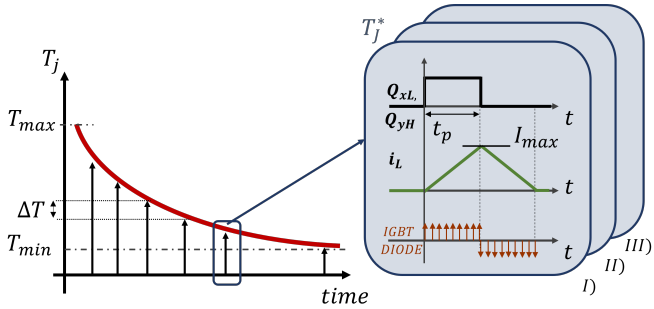

Fig. 6. Description of the calibration procedure. The MUT is heated up to the maximum temperature and then cooled down. Each time a target temperature is reached, a series of three current ramps (namely I, II and III) are imposed in order to calibrate the conduction voltage of the IGBTs and the FWDs.

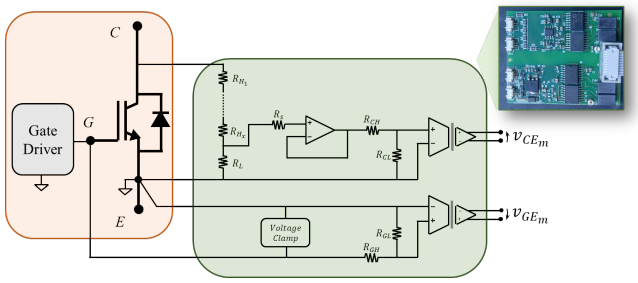

Fig. 7. ON-state acquisition circuitry, highlighted in red the power board of the converter under test, in green the external plug-in board.

A. ON-State Measurement

The external plug-in boards integrate the circuitry for the measurement of the gate emitter driving voltage and the ON-state voltage of each IGBT.

The ON-state voltage sensitivity of IGBTs is in the range of -1 to +4 mV/°C and depends strongly on the current value [39]. Due to the low voltage sensitivity, the most critical task is the design of the V_{CE} measurement circuitry. The system has to be able to measure properly very low voltages with a resolution of millivolts while protecting itself against the dc-link voltage during the device OFF-state. For these reasons, several solutions have been proposed in literature specifically for IGBTs or MOSFETs [20], [40]–[47]. According to the requirements of each application, the V_{CE} monitoring circuit should be selected considering the minimum resolution needed, the measuring range, the maximum sample rate and the bandwidth [24], [48].

The adopted measurement circuit consists of a two-stage topology, as shown in Fig. 7. The first input stage is a voltage divider followed by a unity-gain amplifier. The voltage divider is designed to attenuate the OFF-state voltage of the IGBT

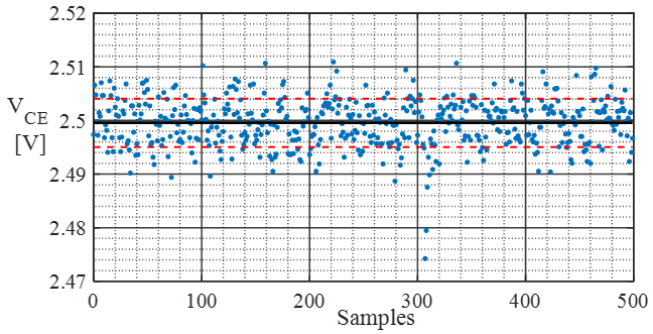

Fig. 8. Sampled voltage for IGBT VL with reference input voltage 2.5V, std=4.5mV.

(i.e the DC-link voltage) to a voltage range consistent to the measurement circuit supply (i.e $\pm 5V$). The unity-gain amplifier provides a low output impedance for the second stage of the measurement circuit. Besides, the resistor R_s protects the circuitry in case of a fault events as the DC-link overvoltage since the input side of the OPAMP is clamped to its supply voltage and the current is limited by the R_s. The second stage provides the insulation between the IGBT common-mode voltage and the control board potential. The signal provided by the first stage is subjected to a further attenuation by a voltage divider and then crosses the isolation barrier of an isolated amplifier.

The benefits of the adopted measurement circuit are: (1) the simplicity (few components are required), (2) the proper mitigation uncertainty due to the presence of the clamping circuitry during the ON-state period [19], [46], (3) negligible influence on the normal operation of the power module and (4) the measurement circuit does not require an active driving [40], [49]. Due to the high impedance of the input stage, the parasitics introduced by the plug-in boards can be considered negligible, especially for IGBTs that are devices characterized by a relatively slow switching behaviour. In the second stage, a voltage divider is used to lower the voltage of the first stage according to the requirements of the insulated operational amplifier. This solution permits to measure both the V_{CE} and the forward voltage V_D of the FWD.

The measuring circuit has the following ratings: measuring range ±3.7V, 16-bit resolution, 1.5MSamples/s, 15μs of maximum delay. The adopted measuring range of ±3.7V is covering the all possible situation as the ON-state voltage drop is 1.7V at 200A, as specified in Table. Ib. The delay is the time interval between the turn-on transition of the IGBT and the steady-state value of the corresponding digital output signal. This delay is introduced by the acquisition circuitry and is consistent with the industrial low switching frequency converters wherein the switching period can be several hundreds of microseconds.

The acquisition circuitry has been calibrated in terms of offset and gain by comparing the measured reference voltages with a precision multimeter. The result of a single acquisition is shown in Fig. 8, as can be noticed the maximum noise is in the range $\pm 10mV$ while the standard deviation for 500 samples is $4.5mV$. This noise is reflected in the estimated temperature as will be described in the experimental results section.

Recently, the increasing diffusion of wide-bandgap materials such as SiC and GaN have increased the concern about the ON-state voltage measurement for temperature estimation, conduction losses estimations and dynamic on-resistance assessment [40], [47]. Although the literature reports solutions with higher dynamic response and better accuracy [50] with respect to the proposed measurement system, these solutions are complex and require an additional number of components. Furthermore, the proposed measurement system does not require to be actively driven (e.g., open a switch to protect the measurement circuit when the voltage between the collector and emitter of the power device is high).

The gate voltage level strongly affects the device ON-state characteristics therefore the V_{GE} is also measured. To ensure a constant V_{GE} during all working conditions, a gate voltage clamp circuitry is integrated in the measuring board. Moreover, the clamping voltage is adjustable thus the MUT can be characterized under different V_{GE}.

B. Current Measurement

The junction temperature is estimated by exploiting the T_j (V_{CE},I_C) correlation hence the device current must be measured. Compared to the ON-state voltage acquisition, the device current can be measured by the phase output current sensors already available on the power converter under test [24]. However, to make the method independent of the accuracy from the sensors mounted on the converter under test, a set of three external closed-loop hall effect current sensors have been used. The current measurement circuit and the ON-state voltage measurement circuit are designed to have the same bandwidth of 50kHz to mitigate the mismatches among the current and voltage samples.

C. Junction Temperature Measurement

The accuracy of the junction temperature estimation is strongly dependent on the temperature measurement during the calibration process. Therefore, a homogeneous temperature distribution inside the MUT and a limited IGBT self-overheating during the current pulses must be both ensured.

The homogeneous temperature distribution is guaranteed by a slow heating phase of the heatsink. As a result the NTC inside the module is representative of all IGBTs [19]. Furthermore, three thermocouples are placed under the baseplate in correspondence of the three dies to track temperature during the whole calibration process.

During the current ramp only the conduction loss term contributes to the losses so it can be easily estimated. The maximum overheating depends on the peak current I_{max} and the ramp duration t_P. For a targeted I_{max}, having a shorter t_P leads to limited self-overheating since less energy must be dissipated. Consequently, the ramp period must be properly selected to limit the overheating below the required threshold.

The thermal model provided in the datasheet lacks accuracy due to the parametric dispersion between the devices, however, it can be used to provide an estimation of the IGBTs self-overheating. The worst-case condition corresponds to the maximum conduction losses, when the IGBTs are at the

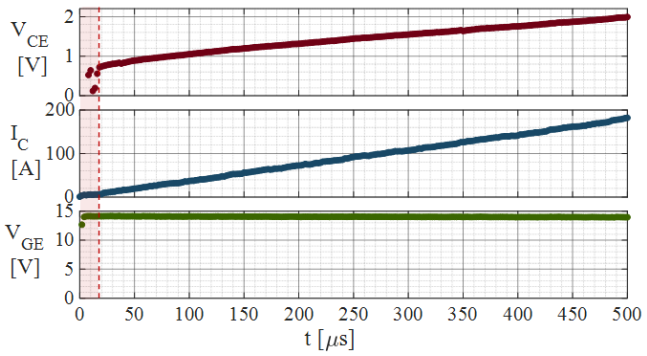

Fig. 9. Raw acquisition signals at $T_J = 115°C$: from the top the voltage V_{CE}, the current I_C and the voltage V_{GE} for device UL.

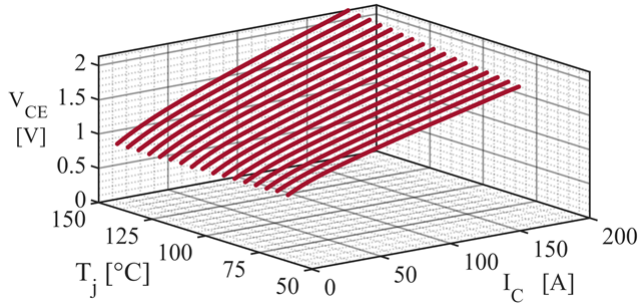

Fig. 10. The V_{CE} map for low side IGBT - UL.

maximum junction temperature. For instance, the maximum self-overheating of the MUT at $T_J = 150\ °C$ and characterized with pulses of $t_P = 500\mu s$ and $I_{max} = 200A$, is lower than $2°C$. In this paper, the maximum calculated self-overheating is within the acceptable threshold and therefore no compensations are required. If needed, the overheating can be partially compensated during the data analysis phase by combining the measured conduction losses with the thermal model provided in the datasheet.

D. Results of the Calibration Process

The results of a measurement for a single device are shown in Fig. 9. The variables are acquired with a timescale of 2µs. The first samples are not considered to eliminate the influence of the oscillation produced by the switching transients. Fig. 10 shows the result for a single device where the calibration has been performed from $150°C$ to $50°C$.

E. Module Layout

The internal module layout may affect the temperature estimation. The module lead resistance indicated in datasheets includes the bonding wires, the DBC copper and the terminal resistances for a single switch and has a non-negligible value that can affect the ON-state voltage measurement [23]. Similarly, the module stray inductance introduces an offset in the voltage measurement that is proportional to the $\frac{di}{dt}$. This limitation can be overcome if the sensing terminals are present (e.g. the Kelvin terminal) that can reduce the path shared by the sensing circuitry and the power traces.

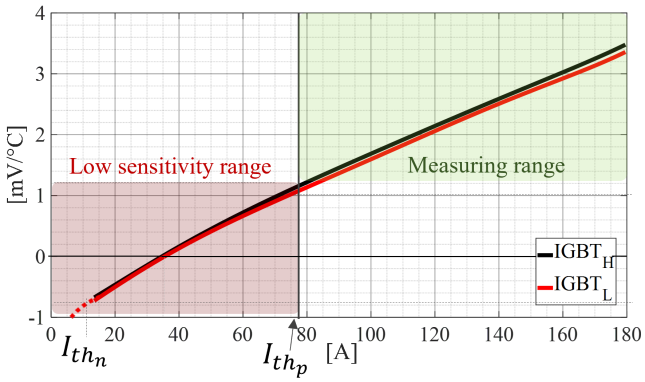

Fig. 11. Average sensitivity curve for phase U high-side and low-side IGBTs.

For the MUT shown in Fig. 2, the low-side switches have both collector and emitter signal terminals, so the effect of the lead resistance is sharply reduced, while the collector connection of the high-side switches is the power terminal of the DC-link upper rail. Therefore, the junction temperature is estimated for the low-side switches only.

In conclusion, the power module layout has a non-negligible effect on the junction temperature estimation process and it cannot be easily evaluated. The ramp period t_P should be selected as a trade-off between the self-overheating of the device and the offset in the voltage measurements.

V. Data Analysis

The $V_{CE}(I_C, T_J)$ maps derived by the calibration process must be elaborated to obtain the $T_J(V_{CE}, I_C)$ look-up tables that can be used for the temperature estimation in the real application. As a first step, for each set of current ramps the raw data collected during the calibration process $v_{CE}= f(t)$ and $i_C= f(t)$, (Fig. 9), are filtered. Thanks to the high sampling rate of the acquisition circuit, the influence of the measuring noise can be strongly reduced. The filtered curves $v_{CE}= f(i_C)$ are resampled to a current vector I_C common for all the calibrated temperatures, resulting in the uniform sampled look-up table $V_{CE}(I_C, T_J)$. Then, the sensitivity analysis of the ON-state voltage with respect the junction temperature is performed. As expected, the ON-state characteristic presents a specific inversion point [23] at which the temperature coefficient changes its sign. For current values below the inversion point, the conduction voltage decreases for increasing temperature while for current above this point the conduction voltage increases. This is reflected to the sensitivity curves for low side IGBT and high side IGBT that are shown in Fig. 11. It must be underlined here that the points for current values below $10A$ are not considered and therefore they are excluded, as highlighted in Fig. 9. Based on the sensitivity curve, two thresholds can be defined, respectively the current negative threshold $I_{th,N}$ and the current positive threshold $I_{th,P}$. The current range between $I_{th,N}$ and $I_{th,P}$ has very low sensitivity. As a result, the change in the ON-state voltage with respect to the junction temperature is too small and therefore cannot be accurately detected by the acquisition circuit. Otherwise, for current values higher than $I_{th,P}$, the sensitivity increases

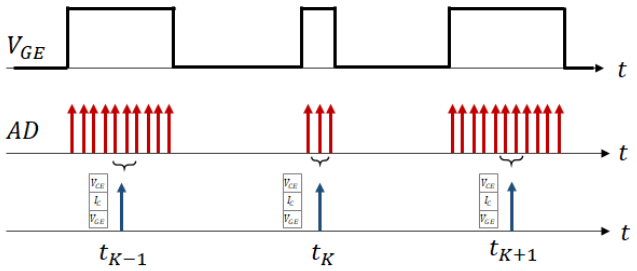

Fig. 12. Description of the acquisition process during the temperature estimation phase.

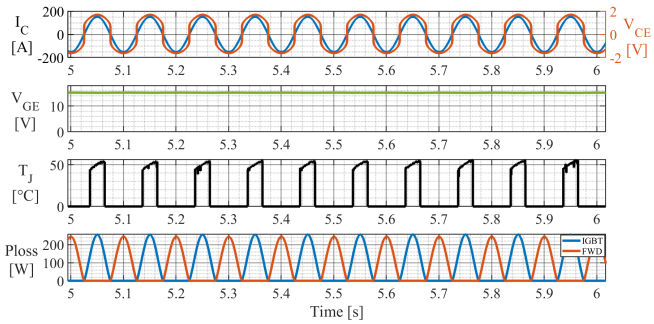

Fig. 13. Results of an acquisition process for device UL. From top to bottom: the ON-state voltage, the load current, the gate voltage, the estimated junction temperature and the instantaneous conduction losses for the IGBT and its antiparallel FWD. The gate emittore voltage is sample during both the IGBT and FWD conduction time.

and therefore the temperature can be correctly estimated. It is worth noticing that $I_{th,P}$ is correlated to the resolution of the ON-state measurements. Indeed, higher voltage resolution results in an increased $I_{th,P}$ allowing an extended temperature estimation range.

Finally, the reverse look-up table $T_J(V_{CE}, I_C)$ is extracted for each IGBT.

VI. Junction Temperature Estimation

The junction temperature estimation is carried out with the testing configuration shown in Fig. 1. The acquisition boards are placed nearby the power modules and connected directly to the main pin with the intent to minimize the length of the connecting cable. The module under test is controlled by the converter MCU (i.e., control board) while the plug-in boards and the external current sensors are connected to a dedicated acquisition board embedding an MCU for data sampling and storing. The acquisition board does not need to communicate with the control MCU of the converter under test.

The sampling process starts whenever each acquisition board detects a rising edge in the gate voltage and lasts until the falling edge, as depicted in Fig. 12. In this time interval, the V_{CE}, I_C and V_{GE} signals are acquired with an acquisition sampling time of $2\mu s$, and the junction temperature estimation is performed by using the middle samples that correspond to the positive and negative vertices of the PWM carrier. Thereby, the measuring circuit can reach its steady-state and none switching transient occurs during these samples.

As shown in Fig. 13, the outcomes of this process are signals sampled at the switching frequency. The positive voltage is the

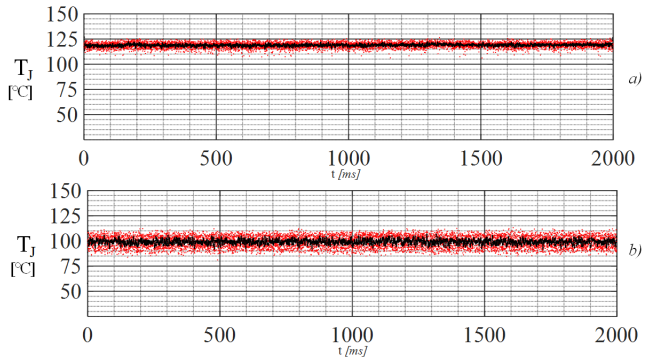

Fig. 14. Experimental results under DC load current condition. a) Estimated junction temperature at $130A$, instantaneous (red) and filtered at 200Hz (black). b) Estimated junction temperature at $85A$, instantaneous (red) and filtered at 200Hz (black).

ON-state voltage of the IGBT, while the negative corresponds to the forward voltage of the FWD. In both time intervals, the load current is sampled thus allowing the instantaneous conduction losses evaluation for both IGBT and FWD. The performance of the acquisition circuitry is evaluated by imposing a DC current and measuring the estimated junction temperature at high (a) and low (b) DC currents, Fig. 14. As expected, the estimation is affected by a noise that depends on the sampled current value according to the sensitivity curves of Fig. 11 and the maximum noise described in Fig. 8. The instantaneous junction temperature presents a noise limited within $\pm 10°C$ of range at $85A$ of output current while it shrinks to a value lower than $\pm 4°C$ when the current rises to $130A$.

The estimated junction temperature of a device for low frequency (1Hz) output current operating point is shown in Fig. 15(a). To test the worst-case operating condition, the cooling fans have been turned off while the DC-link voltage has been set at 700V. As expected, the temperature is available only in a limited interval of time when the output current is higher than the minimum threshold $I_{th,P}$ (i.e. 80A), thus the peak temperature can be estimated while no information about its minimum can be drawn. Although the maximum power losses in the IGBT is in correspondence of the peak current, the peak junction temperature is delayed with respect to the current and is due to the MUT thermal impedance. Fig. 15(b) shows the ON-state characteristic. The first quadrant exhibits a hysteresis phenomenon explainable by the self-heating of the IGBT, while the third quadrant shows the forward characteristic of the FWD. Accordingly, the system is able to measure properly the forward voltage of the FWDs and may be adopted for the estimation of the diode junction temperature.

The transient and the steady state models of the MUT can be evaluated during the prototyping phase. In Fig. 16 the junction temperature is estimated for an AC $(50Hz)$ current during a load cycle of period $1s$, imposing again the worst-case operating condition (cooling fans are OFF, DC-link voltage 700V). Thanks to the high sample rate (at the switching frequency) the system is able to estimate the temperature during both the fundamental frequency $(50Hz)$ and the load cycle $(1Hz)$.

Furthermore, the junction temperature has been estimated by

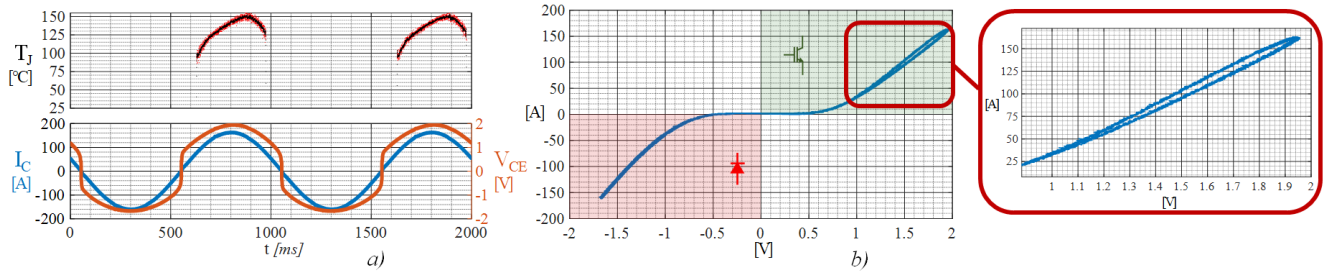

Fig. 15. Experimental results under sinusoidal load current condition of $160A_{pk}$ and $f = 1$Hz, DC-link voltage 700V, cooling fans are OFF

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a) Top: estimated junction temperature, instantaneous (red) and filtered at 200Hz (black). Bottom: V_{CE} and I_C. b) Forward characteristic of the IGBT and FWD.

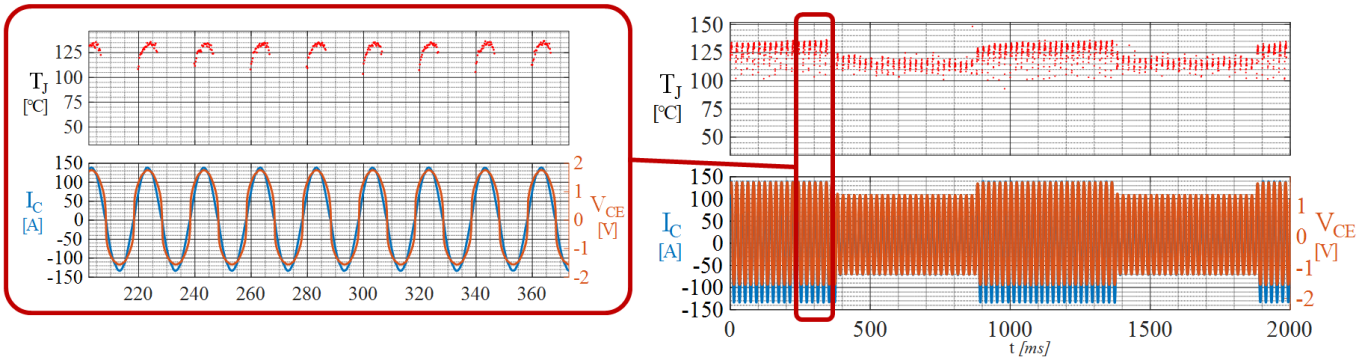

Fig. 16. AC cycle load current condition from $140A_{pk}$ to $70A_{pk}$, $f = 50$Hz, DC-link voltage 700V, cooling fans are OFF. Top: estimated junction temperature. Bottom: V_{CE} and I_C.

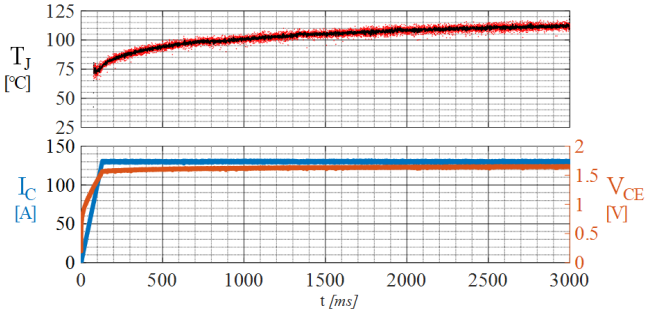

Fig. 17. Experimental results under DC load current condition of $130A$ and initial heatsink temperature 50°C, DC-link voltage 700V, cooling fans are ON. Top: estimated junction temperature, instantaneous (red) and filtered at 200Hz (black). Bottom: V_{CE} and I_C.

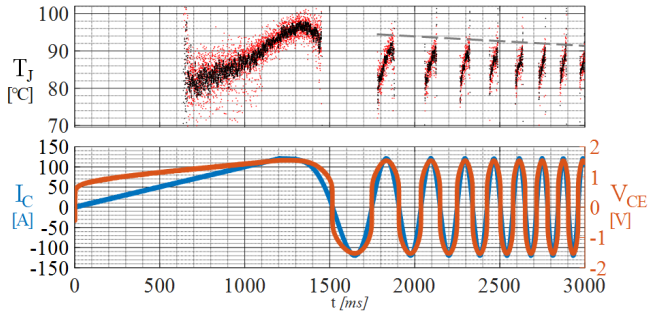

Fig. 18. I/f control with $130A_{pk}$. Top: the estimated IGBT junction temperature, the instantaneous (red) and filtered at 200Hz (black). Bottom: the V_{CE} and the I_C.

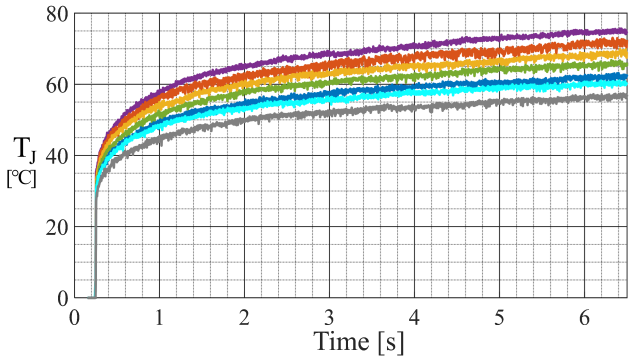

Fig. 19. Junction temperature for device UL at DC current 120A, f_{sw}=4kHz and initial heatsink temperature 25°C. From top to bottom the dc-link voltage: 700V, 650V, 600V, 550V, 500V, 450V, 400V.

implementing an I/f control (current/frequency control) using a constant peak output current of 130A and a frequency that increases linearly from 0 up to 50Hz. The results for this test are shown in Fig. 18. As expected, the maximum temperature and the cycle span exhibit a slight decrease with the raising of the frequency, due to the thermal impedance of the MUT.

The described method can be used to estimate the junction temperature by varying some design parameters as the dc-link voltage and the switching frequency. In the first case, the results are shown in Fig. 19 for a sweep of the dc-link voltage from 400V to 700V, maintaining a constant load current, initial heatsink temperature and fan speed. As expected, the junction temperature increases with the dc-link voltage. For the second

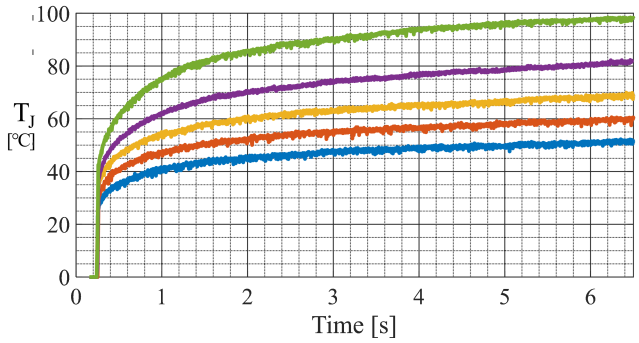

Fig. 20. Junction temperature for device UL at DC current 120A, V_{DC}=600V and initial heatsink temperature 25°C. From top to bottom the switching frequency: 8kHz, 6kHz, 4kHz, 3kHz, 2kHz.

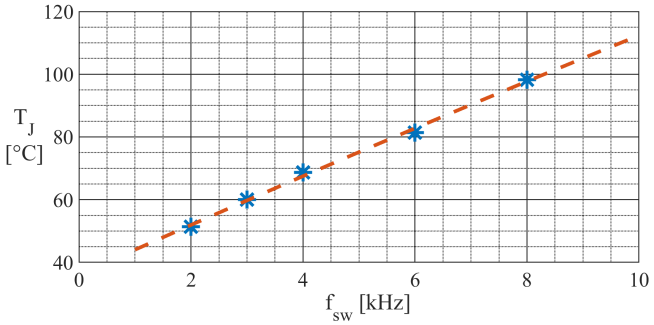

Fig. 21. Steady state junction temperature versus switching frequency for the device UL at current 120A, V_{DC}=600V.

case, for a step DC current, obtained for different switching frequencies, are shown in Fig. 20. In such a case, the test is performed with a purely inductive load hence a low modulation index M (i.e. $\sim$0.5) is required to maintain the fixed target current. With the hypothesis of a low current ripple respect to the reference target, it can be assumed that the conduction losses and the switching current do not change in this analysis. Consequently, the junction temperature increases linearly with the switching frequency. This assumption has been validated experimentally and the results are shown in Fig. 21. Indeed, the points indicating the estimated junction temperature at steady state condition fits well with the linear interpolation.

VII. Electro-thermal Model Validation

The data from the temperature estimator can be used to validate the electro-thermal model of the converter. During the design phase of the converter, the designer must verify the safe operations of all the electrical components with a special focus on power semiconductors being among the most stressed parts of the converter. This operation is usually performed via analytical models or by using dedicated simulation software such as PLECS.

A thermo-electrical model of the converter, shown in Fig. 22, has been developed in the PLECS simulation environment. The power semiconductors and the heatsink have been thermally modelled using the data provided in the datasheets being the only data available during the design phase of the converter. As example two different operating conditions are here reported and the data obtained from PLECS are compared with the one

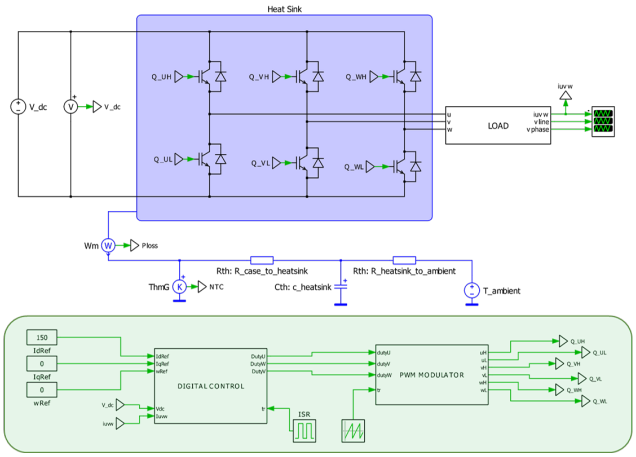

Fig. 22. PLECS model of the converter under test. The blue box represents the thermal model of the heatsink while the green box is the inverter digital control.

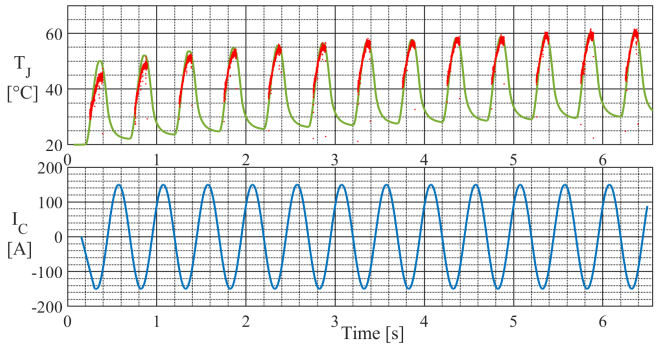

Fig. 23. Estimated (red) and simulated (green) junction temperature at a phase current of $150A_{pk}$-$2Hz$.

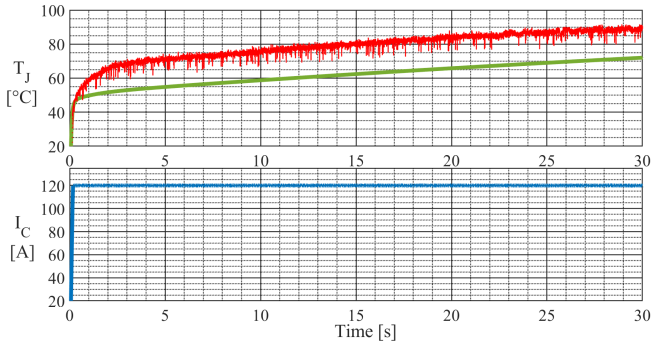

Fig. 24. Estimated (red) and simulated (green) junction temperature at a phase current of $120A$ - DC.

obtained from the temperature estimator using the proposed plug-in system. The plot shown in Fig. 23 compares the junction temperature of IGBT UL obtained from the PLECS model with the one obtained from the temperature estimator when the inverter outputs three phase currents having 150A (peak) and 2 Hz to an inductive load. The two temperature waveforms shown in Fig. 23 present a good matching in terms of peak value. In this case, the thermal model provides a very good representation of the real behaviour of the converter. Fig. 24 shows a comparison between the measured and the simulated IGBT UL junction temperatures, when the converter is working at DC and outputs 120A DC for phase U. As can be noted in

Fig. 24, the PLECS model tends to underestimate the junction temperature and provides a wrong dynamic and 'steady state' temperature estimate with an error of about 20°C. This error can be explained by the different heating of the dies inside the power module due to spatial effects as the thermo-coupling among near dies and asymmetries of the cooling system that for certain operating conditions may differ for the simplified models provided in datasheets. All these effects cannot be properly modelled without a complex thermal matrix. Therefore, this result clearly demonstrates the importance of having an experimental method able to validate the converter design on the real industrial prototype as the simulation models may produce wrong results due to simplified thermal modelling.

VIII. Conclusion

The paper proposes a plug-in acquisition board and a procedure for the junction temperature estimation of IGBT power modules employed in a target industrial power converters. Due to the acquisition noise and low sensitivity, the estimated junction temperature is available only at high current conditions and provides insight about the average temperature of the dies. Nevertheless, these limits do not affect the value of the proposed methodology since the thermal module management needs to be validated at the worst-case operating conditions. The easiness of implementation and plug-in boards make this solution suitable in industrial applications to validate the junction temperature during the prototype validation phase and therefore confirm the performance expected from the design phase. The complete process is described from the calibration step, the data analysis, and the estimation phase. The results are provided with a three-phase industrial converter under given transient and steady-state conditions. A comparison between the temperature estimated with the proposed plug-in system and the one obtained by simulation using thermal model (based on datasheet) has been provided. The results of this comparison demonstrates that significant estimation errors can be expected for particular operating conditions where the models provided by manufacturers are not sufficient to represent the behaviour of the physical system. Therefore, the proposed solution implemented on industrial power converter represents the best converter design validation method.

Furthermore, with a low additional work, it would be possible to put into communication the measurement board with the converter MCU (e.g. SPI communication) thus enabling to provide real-time temperature estimation to the control firmware. This solution can be used to protect the power devices during the preliminary debug phases of the converter.

The temperature estimation method can be carried out for any converter topology. Although the results are shown for an IGBT-based converter this solution can be extended to other semiconductors technologies such as silicon carbide (SiC).

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