Investigation on the Susceptibility to EMI of Second-Order Modulators

Investigation on the Susceptibility to EMI of Second-Order $\Delta\Sigma$ Modulators

Markeljan Fishta
dept. of Electronics and Telecommunications
Politecnico di Torino
Turin, Italy
markeljan.fishta@polito.it

Franco Fiori
dept. of Electronics and Telecommunications
Politecnico di Torino
Turin, Italy
franco.fiori@polito.it

***Abstract*—This paper analyzes the effects of radio frequency interference on second order $\Delta\Sigma$ modulators based on continuous-time (CT) and on discrete-time (DT) architectures. Specifically, Modulators used for the acquisition of sensor signals are targeted, which can operate with moderate clock rates due to the relatively small bandwidth of the signal to be acquired. A continuous wave interference with frequency above that of the modulator clock signal is superimposed onto the nominal input one with the purpose of evaluating the degradation of their performance, and more specifically their capability to demodulate out of band interference.**

***Index Terms*—**

I. Introduction

Integrated Circuits targeted for safety critical electronic modules such as those used in automotive, aerospace or military applications, must comply with tight EMC specifications such as those dealing with the electromagnetic emission tests [1] [2] or the electromagnetic susceptibility tests [3] [4], before being deployed to the market. The compliance to EM emission specs deals mostly with switching circuits such as core logic blocks, IOs and DC-DC converters and on the way the switching noise is propagated off chip. Therefore, the design of such circuits should be carried out to keep the switching noise spectrum within a given mask. On vice versa, EM susceptibility specs are usually regarded as design constraints for the front-end circuits, which are directly affected by the interference injected into the IC pins. Specifically, analog cells like those used in sensor signal conditioning circuits have shown to be highly susceptible to radio frequency interference because they demodulate the out-of-band interference [5] [6]. As a consequence, investigations of the last decades in this field have been mostly aimed to design analog circuits immune to EMI, meaning circuits that do not demodulate the interference. Furthermore, given that amplifiers and filters are usually based on high gain amplifiers, the focus has been on them for a long time [7]. However, analog signals can be conditioned and acquired effectively with oversampling analog to digital (AD) converters based on $\Sigma\Delta$ modulators. In such circuits, the conditioning amplifier is not needed since they show a small input range. Such converters are largely used in the acquisition of sensors signals, and in the signal conditioning chains or radio receivers. The latter are usually based on continuous time (CT) architectures due to the lower power consumption and the higher speed they can achieve with respect to their discrete time (DT) counterparts. The operation of such circuits can be impaired by disturbances superimposed onto the input signal as discussed in [8]. This work focuses on interferers located between the superior edge of the signal bandwidth and the clock frequency of the modulator, assuming that the interferer might be an adjacent channel, close to the desired one. In practice, [8] focuses on the effect of interferers below the modulator clock frequency.

DT modulators are largely used for the acquisition of sensor signals, since they work with moderate clock frequencies. This means that they can easily be subjected to EMI, which resides out of band, meaning over the clock frequency of the modulator. While EMI below the clock frequency of the modulator having a large amplitude can corrupt the baseband signal through the circuit nonlinearities or by driving the modulator outside the stable range, EMI higher than the clock frequency can be folded back into the signal passband because of aliasing [9]. This paper presents a study, through simulation, on the effect of EMI, and a comparison between two modulators - CT and DT - having the same noise shaping transfer function. In II the design of the modulators and the simulation setup is presented. Simulation results are shown and analyzed in III. Finally, conclusions are drawn in IV.

II. Second order $\Delta\Sigma$ converter

The block diagram of a generic second-order discrete-time $\Delta\Sigma$ modulator (DT-MOD2) is shown in Fig. 1. In particular, a Cascaded Integrator FeedBack (CIFB) topology is considered. Its operation can be described as follows: the difference between the sampled input and output signals is processed by the loop filter through a double integration operation. The processed signal is then discretized by the low-resolution quantizer inside the loop. Sampling is performed at a much larger frequency than the input signal bandwidth, according to the relation

$$f_{\mathrm{S}} = 2 \cdot OSR \cdot f_{\mathrm{B}} \tag{1}$$

This work was partially supported by the Power Electronics Innovation Center (PEIC), Politecnico di Torino, Italy. (Corresponding author: Franco Fiori).

where f_S is the sampling frequency, OSR is the oversampling ratio and f_B is the input signal bandwidth. The analog input signal can be recovered by filtering and downsampling the bit stream $v_\mathrm{D}[n]$. A continuous-time modulator (CT-MOD2) has a similar structure, as can be seen in Fig. 2. The main difference is the location at which there is the separation between the CT and DT domains. In the DT-MOD2 the sampling occurs at the input and the loop operates in the DT domain while in the CT-MOD2 the loop operates in the CT domain and sampling occurs at the quantizer. Nevertheless, both architectures provide a second-order noise transfer function (NTF) for the noise added by the quantization. The selection of the NTF order, OSR and number of quantization levels is a trade-off between bandwidth and system complexity, as a specific Signal to Quantisation Noise Ratio (SQNR) is targeted. The modulators considered in this work were designed aiming at a low-bandwidth, high-resolution sensor acquisition application. The target SQNR was

$$SQNR = 95\,\mathrm{dB} \tag{2}$$

and, for the sake of simplicity, two-level quantisation was assumed. These requirements lead to a second order NTF and OSR = 128. The following DT NTF was synthesized by means of the Schreier's toolbox [10]

$$NTF_\mathrm{D}(z) = \frac{(z-1)^2}{z^2 - 1.64z + 0.69} \tag{3}$$

and the loop coefficients were found by comparison with the NTF computed on the block diagram. The NTF for the CT-MOD2 was computed by applying the Impulse-Invariant Transformation (IIT) [11] to the loop function, yielding

$$NTF_\mathrm{C}(s) = \frac{s^2}{s^2 + 0.33 f_\mathrm{S} s + 0.006 f_\mathrm{S}^2} \tag{4}$$

where a NRZ pulse shape has been assumend for the feedback DAC. After finding the loop coefficients, dynamic range scaling was performed in order to make sure that the integrator states are not clipped due to the limited output range [12]. Finally, the input coefficient b_1 was scaled in order for the desired input range to be achieved. Changing b_1 does not affect the NTF since this coefficient is outside of the loop. On the other hand, the Signal Transfer Function (STF) is modified as its magnitude at low frequency is

$$STF_\mathrm{DC} = \frac{b_1}{a_1}. \tag{5}$$

This allows one to compute

$$b_1 = a_1 \frac{V_\mathrm{DD}}{FS} \tag{6}$$

where V_DD is the supply voltage and FS is the full swing of the input signal. The simplified circuit implementation of the CT and DT modulators are shown in Fig. 4 and in Fig. 3, respectively. The loop coefficients are mapped into RC time constants in the CT implementation and into capacitor ratios in the DT implementation. The equivalence between the two schematics was verified by simulation of the impulse response

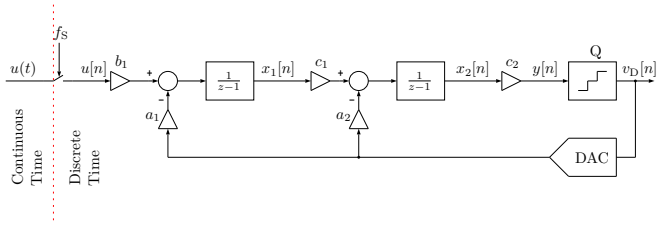

Fig. 1. CIFB architecture block diagram, second order discrete-time implementation. Signals are represented in the discrete time domain. Sampling occurs at the input. The vertical dashed line indicates where the separation between the continuous time and discrete time domains occurs.

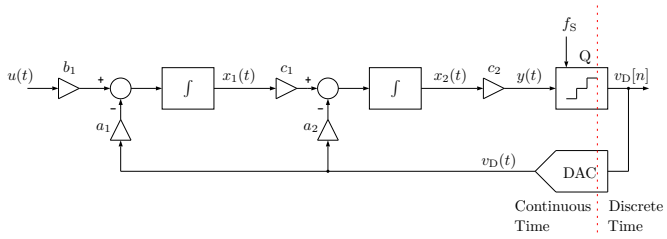

Fig. 2. CIFB architecture block diagram, second order continuous-time implementation. Signals are represented in the time domain. Sampling occurs inside the loop, at the Q block. The vertical dashed line indicates where the separation between the continuous time and discrete time domains occurs.

of the loop filters. In this simulation the input signal was set to zero, the loop was opened and a unit pulse was fed back to both loop filters. The output of such simulation is shown in Fig. 5, where the expected impulse response is plotted as well. It can be seen that, at the sampling instants, v_x2 has the same value in both cases, indicating that the two circuits implement the same NTF.

III. Analysis of the EMI effects

The two $\Delta\Sigma$ modulators, as presented so far, were designed with reference to a $0.35\,\mu\mathrm{m}$ low-voltage CMOS technology process, with power supply of $3.3\,\mathrm{V}$. OA specifications were set such that the performance of the modulators was not impaired, as gain-bandwidth product (f_U) limitation is responsible for the linear settling of the integrators and slew-rate (SR) limitation can result in harmonic distortion at the output of the modulator. Since the current design uses a moderate clock frequency of $f_\mathrm{S} = 4\,\mathrm{MHz}$, a constraint of $f_\mathrm{U} > 5 f_\mathrm{S}$ was chosen [11]. An upper bound on the SR limitation instead can be computed for the CT implementation using the loop filter time constants and the reference voltage which yields a worst-case value of $SR < 8.53\,\mathrm{V/\mu s}$. For the DT implementation a suggested constraint from [11] is $SR > 1.1 \cdot \Delta \cdot f_\mathrm{S}$, where Δ is the difference between the levels of the quantizer, which yields $SR < 14.52\,\mathrm{V/\mu s}$. Time domain simulations were used as well to check that the output of the integrators settled in less than half a clock period, before the sampling instant. The same OA, whose specifications are summarized in Table I, was used for both the CT and SC implementations. The output D flip-flop was implemented by means of a standard

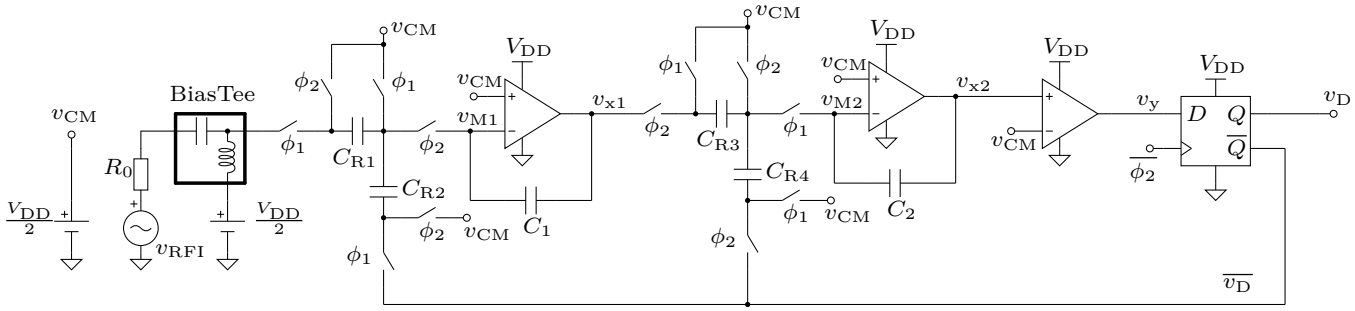

Fig. 3. Circuit implementation of the Switched-Capacitor modulator. The D-type Flip Flop performs both the sampling of the quantizer output signal and it provides the feedback pulses to the loop filter. Timing of the control signals for the switches was set such that the effects of charge injection and clock feedthrough were minimized.

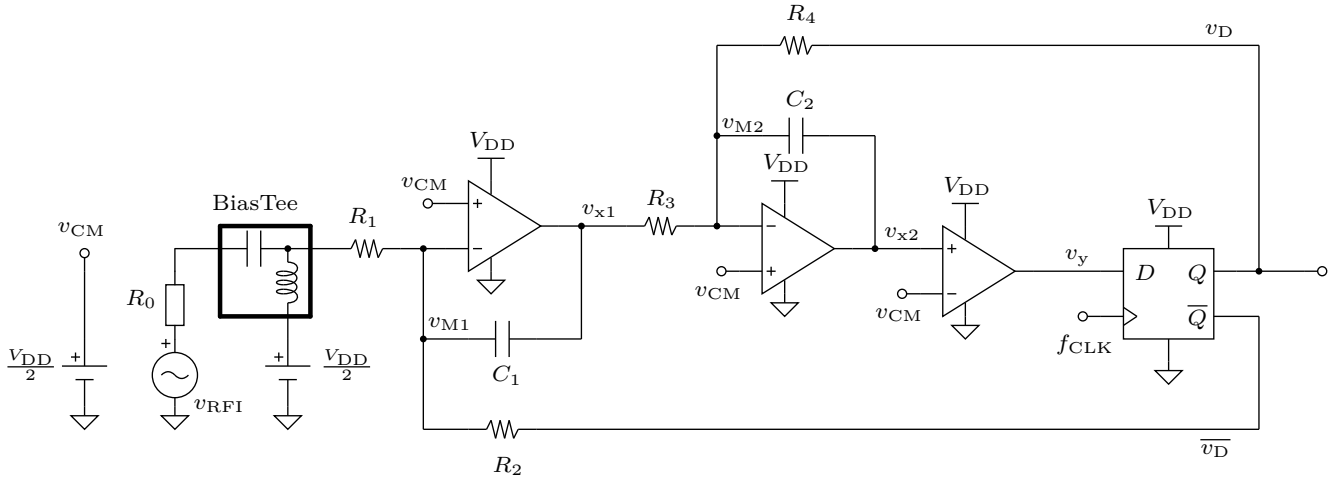

Fig. 4. Circuit implementation of the Continuous-Time modulator. The D-type Flip Flop performs both the sampling of the quantizer output signal and it provides the feedback pulses to the loop filter.

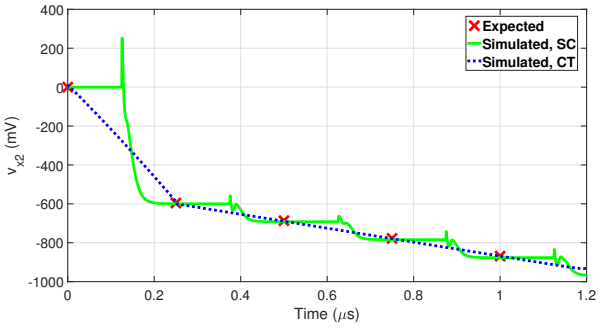

Fig. 5. Impulse response comparison for the two modulator architectures and the synthesized impulse response. The voltage represented is the output of the second integrator, following a pulse applied to the loop filter while the input is at zero.

cell in the chosen CMOS process. The analysis of the EMI effects on both modulators was performed through time-domain simulations, using SPECTRE, a Spice-like simulator. The simulation setup was built as shown in Fig. 4 and Fig. 3

Supply voltage	3.3 V
A_{d0}	84 dB
f_U	31 MHz
PM	69 deg
SR	17 V/µs

TABLE I
OA SPECIFICATIONS.

for the CT and SC modulators, respectively. The analysis of the EMI effects on both modulators was performed through time-domain simulations, using SPECTRE, a Spice-like circuit simulator. The simulation setup was built as shown in Fig. 4 and Fig. 3 for the CT and DT modulators, respectively. The nominal input signal was set at zero and a CW signal with variable amplitude and frequency was superimposed. Amplitudes of $V_{\mathrm{pk,inj}} = 200\,\mathrm{mV}$ and $V_{\mathrm{pk,inj}} = 1\,\mathrm{V}$ were used for the disturbance signal, in order to analyse the effect of disturbances both inside and outside the input range of the modulators. The frequency was swept across the range $(20\,\mathrm{MHz}, 960\,\mathrm{MHz})$ for the purpose of covering a range of frequencies widely used for radio communications. The

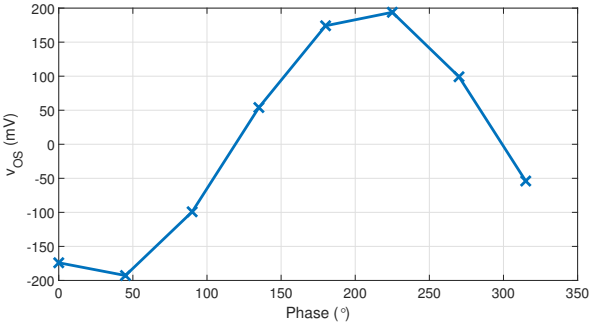

Fig. 6. Input-referred offset, DT-MOD2, phase sweep at 20 MHz.

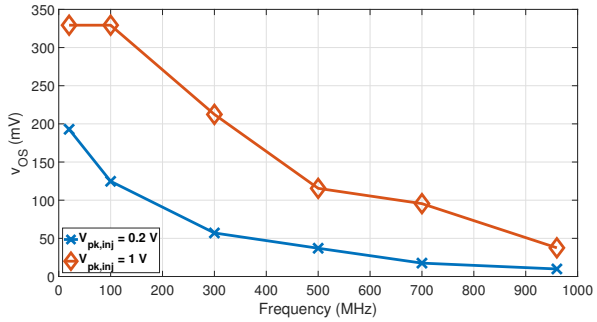

Fig. 7. Input referred offset, DT-MOD2. Worst case delay was set for the input signal at the different frequencies.

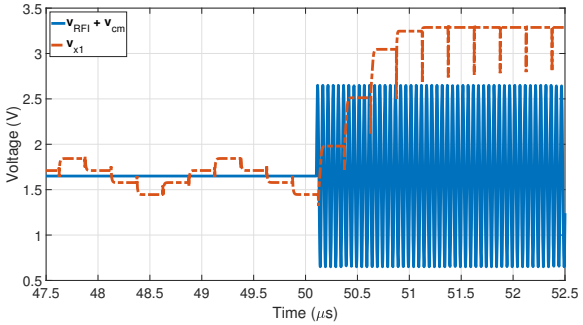

Fig. 8. Saturation of the integrators shown for the case with $V_{\mathrm{pk,inj}} = 1\,\mathrm{V}$ and $f_{\mathrm{inj}} = 100\,\mathrm{MHz}$.

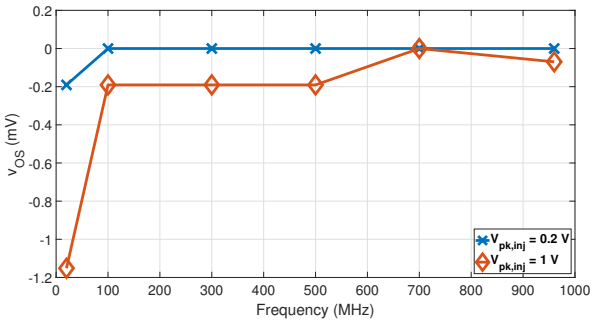

Fig. 9. Input-referred offset, CT-MOD2.

criterion for evaluating the susceptibility of the two circuits to EMI, as commonly done in previous works [7], is the input-referred offset voltage, computed as

$$v_{\mathrm{OS}} = \frac{\langle v_{\mathrm{D}} \rangle}{STF_{\mathrm{DC}}} \tag{7}$$

where $\langle v_{\mathrm{D}} \rangle$ is the average of the output voltage during the observation time.

A. DT-MOD2

Simulations were performed on the DT-MOD2 in order to evaluate the worst-case EMI-induced offset. For this purpose, the phase of the disturbance with respect to the sampling signal edge was swept. The resulting offset voltage is shown in Fig. 6. As to be expected, the input referred offset varies with the phase of the disturbance. The reason is that the test frequencies are an integer multiple of the modulator clock frequency, hence the disturbance is sampled always at the same point inside the period. This means that the undersampled signal cannot be distinguished from a DC signal and its magnitude depends on the phase relation between the disturbance and the sampling signals. After finding the worst case for the phase of the disturbance, simulations were performed at varying frequency and amplitude. Input-referred offset in the various cases is shown in Fig. 7. The offset voltage shown has been normalized by removing the observed offset in the case without injection.

B. CT-MOD2

As in the previous case, simulations were performed at varying phase for the disturbance signal. In this case, a noticeably lower offset variation was noticed with respect to the case of the DT-MOD2. Simulations were then performed at varying amplitude and frequency of the disturbance signal and the results are presented in Fig. 9. The most important difference with respect to the DT case is the significantly lower input-referred offset voltage. In order to observe weather the interference gives rise to other effects, besides offset voltage, simulations were performed with a sinusoidal signal applied to the modulator and the disturbance signal superimposed to it. The input signal had a frequency $f = 4.01\,\mathrm{kHz}$ and amplitude $V_{\mathrm{pk}} = 200\,\mathrm{mV}$, while the disturbance signal had variable frequency and amplitude. A number $N = 16384$ of clock cycles was simulated and the N-Point Fast Fourier Transform (FFT) of the output signal was computed. Results are plotted in Fig. 10. Simulations were performed injecting at the output as well, according to the setup shown in Fig. 14. A worst-case analysis was performed by applying a CW signal such that the amplitude of the superimposed disturbance on the output signal is $200\,\mathrm{mV}$ and $1\,\mathrm{V}$. The non inverted output of the D Flip Flop was chosen for the injection, since the disturbance in this case would only be filtered by one stage before being quantised, hence maximizing its effect. Results of these simulations are shown in Fig. 15.

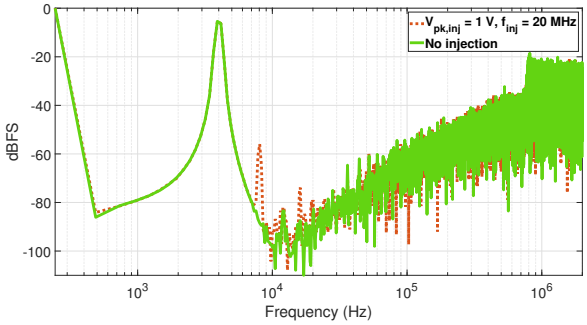

Fig. 10. Spectrum of the output voltage for the CT circuit. Comparison between the case with no injection and the case with $V_{\mathrm{pk,inj}} = 1\,\mathrm{V}$, $f_{\mathrm{inj}} = 20\,\mathrm{MHz}$.

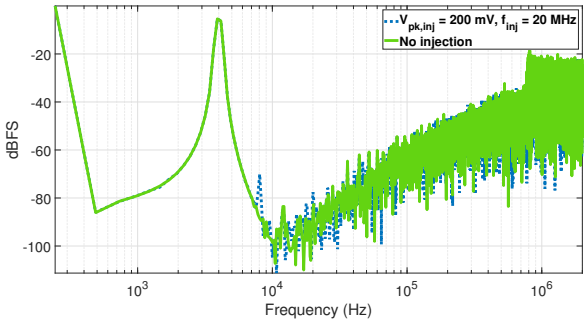

Fig. 11. Spectrum of the output voltage for the CT circuit. Comparison between the case with no injection and the case with $V_{\mathrm{pk,inj}} = 200\,\mathrm{mV}$, $f_{\mathrm{inj}} = 20\,\mathrm{MHz}$.

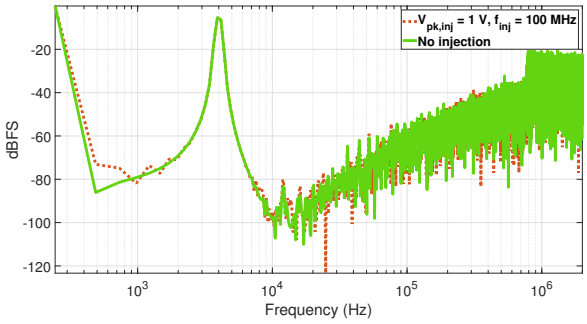

Fig. 12. Spectrum of the output voltage for the CT circuit. Comparison between the case with no injection and the case with $V_{\mathrm{pk,inj}} = 1\,\mathrm{V}$, $f_{\mathrm{inj}} = 100\,\mathrm{MHz}$.

C. Results Discussion

It can be seen from Fig. 7 that at $200\,\mathrm{mV}$ injection amplitude the input-referred offset at the lower frequencies is approximately equal to $200\,\mathrm{mV}$, since the disturbance voltage is being sampled always at its peak. At the higher frequencies the observed offset voltage decreases, partly because of the low-pass filtering introduced by the switch resistance and the sampling capacitor, partly because of the inaccuracy in fixing the signal delay as its period becomes increasingly smaller. On the other hand, at $1\,\mathrm{V}$ injection amplitude, the input-referred

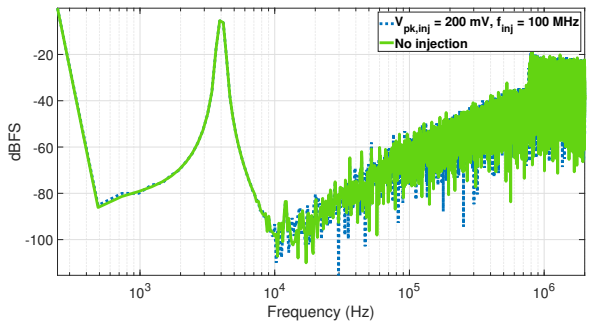

Fig. 13. Spectrum of the output voltage for the CT circuit. Comparison between the case with no injection and the case with $V_{\mathrm{pk,inj}} = 200\,\mathrm{mV}$, $f_{\mathrm{inj}} = 100\,\mathrm{MHz}$.

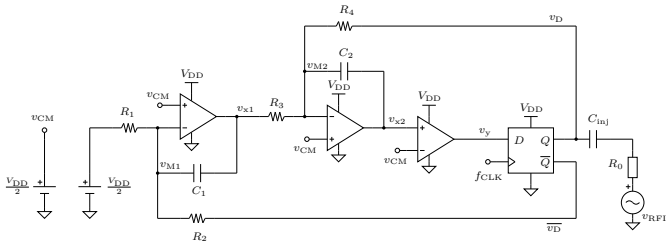

Fig. 14. Simulation setup for output injection.

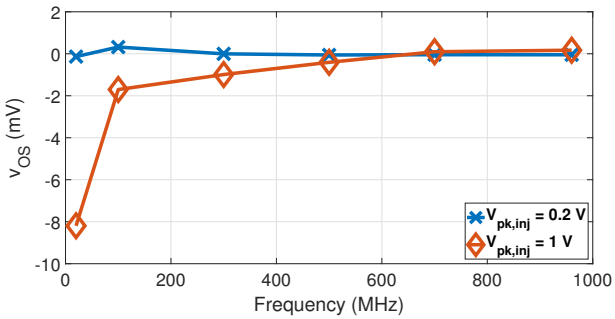

Fig. 15. Input-referred offsetin the CTMOD2 as a result of disturbance injection at the output.

offset is smaller than $1\,\mathrm{V}$. This is due to the fact that the input range of the modulator was set to

$$FS = \frac{V_{\mathrm{DD}}}{5} \tag{8}$$

hence the sampled disturbance is outside the input range. This can be seen by observing the internal signals of the circuit, presented in Fig. 8, where it is shown that the first integrator is driven into saturation. Concerning the CT-MOD2, it was observed that the magnitude of the residual offset decreases with increasing frequency and it is larger for larger disturbance amplitudes. A possible explanation could be related to the filtering of the disturbance before being sampled. Since the applied disturbances are out of band of the OA, the integration operation performed by the modulator is not effective at the frequencies of the disturbances. Hence, the disturbance is not

averaged out by being integrated by the loop filter. Instead, it is low-pass filtered by the passive components around the first integrator i.e., the input resistor R_1 and the equivalent capacitance loading the OA inverting input. The residual offset voltage could then be related to a non zero-area residual disturbance overlapped to the error voltage of the first OA, which propagates towards the output. Spectral analysis showed that the RFI can give rise to even-order distortion. Simulation showed a $30\,\mathrm{dB}$ increase in HD2 and a $10\,\mathrm{dB}$ increase in HD4 at $20\,\mathrm{MHz}$ and $1\,\mathrm{V}$ amplitude injection.

The amount of distortion decreased as the amplitude of the disturbance was reduced, and was barely noticeable as the frequency increased at $100\,\mathrm{MHz}$. It is not clear at present which is the relation between the RFI disturbance injected and the increased even-order distortion at the output of the modulator. It could be related to the fact that the input signal has some frequency components that are close to the f_U of the OAs and still below the corner frequency of the passive network which performs low-pass filtering on the higher frequency disturbances, however there are few published studies that elaborate on the relationship between integrator gain-bandwidth product and harmonic distortion so the root cause of the observed distortion is still to be understood. Injection simulations at the output of the modulator showed a slightly increased offset voltage with respect to the ones performed at the input, with a similar behavior as a function of amplitude and frequency of the disturbance. The main reason is that the injection at the output was performed at a point such that the disturbance is filtered by only one stage of the loop filter, hence maximizing its effect.

IV. Conclusion

In this paper, the effects of EMI on two second-order $\Delta\Sigma$ modulators were analyzed by time-domain simulations. Simulations showed that, for CT-MODs, the interference applied at the input is largely suppressed by the low-pass filtering action of the input passive network around the first integrator since, at the injection frequencies, the OA is not operating as an integrator. Since the sampling action is performed inside the loop, at the quantizer, the interference has a very small effect on the quantized voltage, which translates in a small input-referred offset voltage when high frequency disturbances are added at the input. On the other hand, it resulted from spectral analysis that even-order harmonic distortion increases noticeably under injection conditions, especially at the lower frequencies where the filtering action of the passive network is not as effective. DT-MODs, on the other hand, sample the disturbance at the input, so for disturbances at frequencies being integer multiples of the clock frequency, the sampled input voltage cannot be distinguished from a DC voltage. The worst case is when the input voltage is sampled at its maximum/minimum, which can result in the modulator saturating because of the maximum stable input range, as was observed in the simulations with $1\,\mathrm{V}$ amplitude disturbance.

References

[1] IEC 61967, "Integrated Circuits-Measurement of Electromagnetic Emission, 150 kHz to 1 GHz," Ed. 1. 0, February 2006.

[2] F. Fiori, F. Musolino, "Measurement of integrated circuit conducted emissions by using a transverse electromagnetic mode (TEM) cell," in Trans. on Electromagnetic Compatibility, vol. 43, no. 4, 622-628, Aug. 2001.

[3] IEC 62132-4, "Integrated Circuits-Measurement of Electromagnetic Immunity, 150 kHz to 1 GHz," Ed. 1. 0, February 2006.

[4] H. Pues, D. Pissoort, "Design of IEC 62132-4 Compliant DPI Test Boards that Work up to 2 GHz", International Symposium on Electromagnetic Compatibility - EMC Europe, pp. 1-4, Sept. 2012, Rome, Italy.

[5] Jean-Michel Redouté, Michiel Steyaert, "EMC of Analog Integrated Circuits", Springer, 2010.

[6] F. Fiori, F. Crovetti, "Investigation on RFI effects in bandgap voltage references," in Microelectronics Journal, vol. 35, no. 6, 557-561, Aug. 2004.

[7] F. Fiori, "Investigation on the Effectiveness of the Dynamic Offset Cancellation to Improve the Immunity of DDAs to EMI", International Symposium on Electromagnetic Compatibility - EMC Europe, pp. 1-5, Sept. 2020, Rome, Italy.

[8] K. Philips, P. Nuijten, R. Roovers, A. Roermund, F. Chavero, M. Pallares, and A. Torralba, "A Continuous-Time Sigma-Delta ADC with Increased Immunity to Interferers," in IEEE Journal of Solid-State Circuits, vol. 39, no. 12, 2170-2178, Dec. 2004.

[9] D. Musumeci, F. Fiori, "Susceptibility of a Sigma-Delta Converter to EMI", International Zurich Symposium on Electromagnetic Compatibility, pp. 365-368, Jan. 2009, Zurich, Switzerland.

[10] Richard Schreier, "Delta Sigma Toolbox", Matlab, [Online] https://it.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox

[11] J. Cherry, W. Snelgrove, "Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion," Springer, 2002.

[12] Shanthi Pavan, Richard Schreier, and Gabor Temes, "Understanding Delta-Sigma Data Converters," John Wiley, 2017.