Optimal Tuning of AGDs Parameters and a Technique for Testing the Correct Mounting of Heatsinks on Power Transistors

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November 2021

Nowadays, energy conversion is one of the most popular topics addressed both in research and industrial environment. The reason for that is, in the last decades the energy consumption related to carbon fossil combustion has caused several negative effects on the environment, such as the global warming and the increase of the pollution level, leading the humanity to spend time and resources for increasing the utilization of energy sources with a low impact on the ambient, like the photovoltaic and the wind generated ones. Nevertheless such forms of energy are "*green*", they need to be converted and delivered in order to be exploited in the best way. Such subject has brought the *Power Converters* and all the related topics, and components which make up the power module to become a burning issue of the last years. When speaking about the conversion of the energy, the designer has to deal with several issues, among which the efficiency and thermal management of the system, which are two of the most critical aspects of the design flow, both mainly related to the most important components of a power converter, the *power switches*. These components are continuously under investigation, in order to improve their performance in terms of voltage and current handling, switching speed and power losses, leading the Silicon device to approach very close their theoretical limits. For such a reason, new semiconductor materials, the Wind Band-Gap (WBG), have been investigated to develop even more performant power switches, with the aim of replacing their Silicon counterpart. Such devices, with their faster switching transients and smaller parasitic capacitances, can excite high frequency resonant circuits occurring in oscillations, overvoltages and/or overcurrents that could destroy the power transistor and increase the level of the Electromagnetic Interference (EMI). Traditional approaches to solve such an issues consist of using snubber circuits and/or to reduce the strength of the driver increasing the gate resistance. Nevertheless such solutions remove the oscillations, reducing the overvoltages and the overcurrents, they can reduce excessively the switching speed of the transient, increasing the switching losses and so

the temperature of the switches, which need of even larger heatsinks to dissipate the produced heat and making ineffective the use of WBG devices. A consolidate solution to fix such issues consists of using Active Gate Driver (AGD) to turn-on and to turn-off the power switches. Such solution allows the designer to control the switching waveforms during the transitions, by modulating the strength of the driver and providing the user the capability to find the best trade-off between the power losses and the switching speed. Notwithstanding the effectiveness of the AGD techniques, it worth highlighting that in literature any method to derive the gate driving profile is provided, and the driving waveforms is often obtained by means of trial and error approach.

The aim of the first part of this thesis is to fill such gap, by providing a mathematical model to obtain the optimal switching waveforms, i.e, the non oscillating and less dissipative ones is proposed, and then an algorithm to obtain the optimal gate current profile by means of simulation is proposed. The optimal switching waveforms, along with the parameters resulting from the proposed algorithm, are a step forward with respect to the trial-and-error or local optimization methods that can be found in literature. Indeed, the proposed approach provides the target output waveforms, thus knowing in advance the best trade-off between power dissipation and switching speed. The method discussed in this work is then applied on a prototype, resulting in the optimal switching waveforms expected from the proposed analysis.

In the second part of this thesis, the focus moves on the thermal management of power transistors, more precisely on the capability of a power MOSFET, on which is mounted an heatsink, to dissipate the heat. In particular, two end of manufactury test strategies to check the correct assembling of an heatsink on the power switch are proposed. Such techniques are based on the linear relationship existing between the drain source on resistance ($R_{ds,on}$) and the junction temperature T_j, so they do not requires any temperature measurements, once the calibration procedure is performed. The former technique can be applied to transistors which gate can be reached with an Automatic Test Equipment (ATE) controlling the duration of the on phase of the device, the latter can be applied on power transistors mounted in hard switching power converter, while they are normally working. The proposed technique are both experimental assessed considering several commercial heatsinks and different induced thermal faults, which simulate the incorrect behavior of the heatsink. The experimental validation has allowed for the identification the thermal faults in more than 90% of the analyzed cases.