Doherty Power Amplifiers for Ka-Band Satellite Downlink

Doherty Power Amplifiers for Ka Band Satellite Downlink (invited)

Anna Piacibello[#*1], Paolo Colantonio[†2], Rocco Giofrè[†3], Vittorio Camarchia[#4]
[#]Department of Electronics and Telecommunications, Politecnico di Torino, Torino, Italy
[*]Microwave Engineering Center for Space Applications (MECSA), Roma, Italy
[†]Department of Electronic Engineering, Universitá di Roma Tor Vergata, Roma, Italy
{[1]anna.piacibello, [4]vittorio.camarchia}@polito.it, [2]paolo.colantonio@uniroma2.it, [3]giofr@ing.uniroma2.it

***Abstract*—This paper describes the design, realization and tests of different Doherty power amplifiers (DPAs) specifically conceived for Ka-band satellite downlink applications, i.e., 17.3 – 20.3 GHz. In particular, different design strategies have been explored by accounting for the possibility to combine power on-chip at either device or PA level, also exploring the parallel (current summing) and "series" (voltage summing) interconnection of elementary devices. As a result, three DPAs have been implemented on a commercial GaN HEMT process with 100 nm gate length grown on Silicon substrate. Pros and cons of these different solutions will be highlighted by presenting the main design steps and the preliminary experimental results.**

***Index Terms*—Doherty, GaN, high efficiency, linearity, power amplifiers, satellite.**

I. Introduction

The Power Amplifier (PA) is one of the bottleneck elements in determining the performance of wireless transmitters, both for space and ground applications, in terms of energy efficiency and linearity.

Satellite transmitters are moving towards increasingly high carrier frequencies and spectrally efficient modulating signals, to achieve data rates as high as possible in an ever more crowded frequency spectrum. Therefore, the PA is expected to operate as efficiently as possible not only at peak output power levels, but also at a certain amount of output power back-off (OBO), depending on the Peak-to-Average Power Ratio (PAPR) of the adopted signal.

Simultaneously, the availability of Gallium Nitride High Electron Mobility Transistor (GaN HEMT) technologies is pushing the replacement of Travelling Wave Tube Amplifiers (TWTAs) by Solid State PAs. However, despite the high power density of GaN, to achieve watt-level output power at MMIC level, several transistors have to be combined.

Corporate PAs have naturally been the first explored architecture for such applications, and have proved to provide the required power levels with interesting saturated efficiency levels up to Ka-band, at least. Recently, the Doherty PA (DPA) architecture is being explored as a possible valid alternative to corporate PAs for space applications at microwave and mm-wave frequencies, to improve the average efficiency when modulated signals are considered, while still targeting a sufficient linearity.

This paper presents an overview of the research activities carried out in the framework of the GANDALF project, supported by the European Space Agency (ESA), which aim is to investigate the possibility to develop high performing MMIC GaN DPAs for Ka-band satellite downlink applications.

II. Project aims and requirements

The GANDALF project aims at assessing the feasibility of DPAs, targeting at least 36 dBm of output power (P_{out}) and 35 % of power added efficiency (PAE) at 15 dB of Noise-to-Power Ratio (NPR) in the 17.3 – 20.3 GHz band. The desired small signal gain is of 30 dB, with input and output return loss lower than -15 dB. Further requirements are that all active devices should maintain a junction temperature lower than 160 °C in all operating conditions, with the chip base plate temperature ranging from -10 °C to +75 °C, and that the DPAs must be insensitive to load variations, which may occur during non standard operative conditions. The linearity assessment itself is not trivial, as it is based on the system level figure of merit NPR, that is still being investigated from the theoretical point of view, especially when concerning nonlinear dynamic systems such as wideband PAs [1]. The NPR characterization consists in evaluating the ratio between nonlinear distortion noise and signal power spectral density at the output of the PA, when the PA is excited by additive white Gaussian Noise (AWGN) with a central notch. In the classical NPR characterization, the AWGN distribution imposes a PAPR of 8 dB, which may differ from the one of the application. On the other hand, this ensures that different NPR measurements are comparable, without the need of specifying the IQ data of the adopted signal.

The main requirements are compared in Table I with the performance achieved by some previously published PAs targeting a similar frequency range. The targeted performance was above state of the art at the time the project was started, and similar P_{out}, PAE and bandwidth requirements have not yet been achieved simultaneously even today, especially under the stringent thermal and linearity constraints of satellite applications.

III. Selected technology

The selected technology is the D01GH process by OMMIC, a GaN HEMT tehcnology with 100 nm gate length grown on a 100 μm thick Silicon substrate. The maximum operating drain supply voltage supported is 15 V, which limits the use

TABLE I
COMPARISON BETWEEN SPECS AND SOA KA-BAND PAS

Freq. (GHz)	Pout (dBm)	PAE (%)	Gain (dB)	Der. Y/N	Ref
20–21	33	27	27.5	N	[2]
18–20	34.5	18	22	N	[3]
20.2–21.2	29	18	19	N	[4]
17.3–20.3	43	22	31	Y	[5]
17–20.2	39.5	28	24	Y	[6]
17.3-20.3	**36**	**35**	**30**	**Y**	**Target**

* For [2], data at 15 dB NPR. For [3], [4] an estimate for similar linearity

of the technology for space applications only up to 11.25 V, according to reliability (i.e., de-rating) rules. This yields a power density around 2 W/mm. Since 5 W of output power is desired at 15 dB NPR, and being the NPR an *a posteriori* verification, a rough *a priori* estimation is needed to guide the design, at least in terms of choice of active periphery and width of high efficiency region. In order to reach the desired power target with a sufficient amount of back-off to allow for the required linearity (≈2-3 dB), the DPAs have been designed for 38-39 dBm of output power and 6 dB of OBO from efficiency peak. This requires an overall active periphery between 3 mm and 4 mm for the power stage.

IV. PA ARCHITECTURES

To achieve the required power level on a single-chip DPA, assuming a symmetrical DPA configuration with the same periphery on Main and Auxiliary branches, an active periphery of the order of 1.5–2 mm is required for each branch. This is not compatible with a single device (max. size for which the foundry non-linear model has been validated is $8\times100\,\mu$m), thus a combination of at least two devices for each branch becomes mandatory.

Consequently, by using the $8\times100\,\mu$m device as building block, different possibilities to combine power on-chip have been explored (Fig. 1), at device level or at PA level, as detailed in [7]. In particular, the DPA named MMIC1 exploits the parallel combination of two transistors in Main and Auxiliary branches, whereas in the DPA named MMIC2 the same output power is achieved by combining two mini-DPA cells. Indeed, in MMIC2 the final stage of Main and Auxiliary branches of each mini-DPA is implemented with only one $8\times100\,\mu$m device. Then, the two mini-DPAs are combined directly on-chip.

While at PA level the parallel combination is the only possibility, at device level two possible strategies exist for power combination, i.e., in parallel (current summing) or in series (voltage summing) [8]. The parallel combination is potentially easier to be designed, although it may be affected by some degree of asymmetry between the loading conditions of the two transistors, but it lowers the optimum load impedance, thus increasing the transformation ratio to 50 Ω. The series combination is quite complex to be designed, especially at operating frequencies close to the process cut-off frequency, posing layout, matching and stability challenges [9], but it has the advantage of increasing the optimum load impedance thus bringing it closer to 50 Ω. On these bases, an advanced DPA architecture, named MMIC3, has been developed relying upon the series device combination (stacking). It is more complex in terms of number of different bias lines, including two different drain supply voltage levels, but it allows to achieve a gain that is comparable to MMIC1 and MMIC2 without the need of the pre-driver stage in front of the DPA itself. In both cases, the architectures based on device-level combination (MMIC1 and MMIC3) result more compact, with a chip area of $5\times4\,\text{mm}^2$.

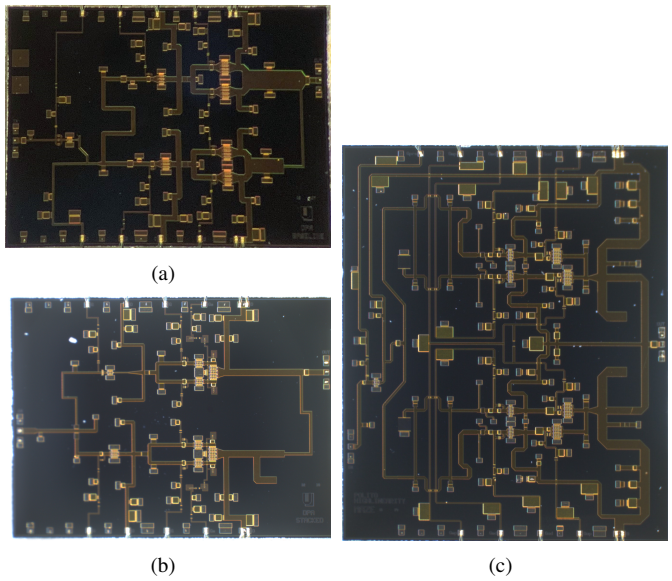

Fig. 1. Microscope photographs of (a) MMIC1, (c) MMIC2 and (b) MMIC3.

The combination at DPA level generally assures a better control of the load modulation since it has no issue related to the different loading conditions of transistors in the same branch. On the other side, it is in general more area consuming, and poses a challenge in terms of routing of the DC bias lines to the internal active devices, which in general need to be biased at a different voltage than the external ones, unlike in a corporate PA. The presence of driver stages inside the DPA architecture has a two-fold impact on this aspect, with opposite implications. On the one side, a higher number of DC bias lines are necessary; on the other side, drivers can be used to "distribute" the class C of the Auxiliary branch, shaping the required current profile while adopting the same bias voltage for several stages, thus reducing the number of independent DC bias lines. There are two possibilities to split and combine the power between the cells, i.e., adopting isolated couplers or non-isolating structures. The latter may be advantageous in terms of losses, especially at the output, where they have a strong impact on efficiency, but are riskier in terms of stability and also make the overall PA performance more strongly reliant on the accuracy of the nonlinear model in predicting the device impedance, especially at the input. The developed MMIC2 is based on non-isolating splitting and combining

structures and aims at maintaining as many degrees of freedom as possible in terms of separate gate bias controls, which is expected to be beneficial during the characterization, to adjust the Auxiliary turn-on and the overall linearity. The resulting chip is more dense and area consuming than the others, with a chip area of $5\times6\,\mathrm{mm}^2$, but it should allow to maintain the expected performance over a wider bandwidth.

V. Experimental Results

The on-wafer screening of the designed DPAs has been carried out at the nominal bias point. Fig. 2 (a)–(c) shows the measurement scattering parameters of the working chips. Notably, the small-signal gain is around 30 dB for MMIC1 and MMIC2 whereas MMIC3 achieves a slightly lower value. Input and output matching of all chips are in between -7 dB and -15 dB in the overall bandwidth. Among the working chips, one for each version has been integrated on a copper carrier for the subsequent nonlinear characterization. Fig. 3 shows a picture of the assembled DPAs whereas Fig. 2(d) reports the measured power sweeps of the most advanced architecture (i.e., MMIC3) at 17.3 GHz and 20 GHz. Notably, this DPA achieves a saturated output power and maximum PAE close to 38 dBm and 35%, respectively. The characterization of MMIC1 and MMIC3 is in progress.

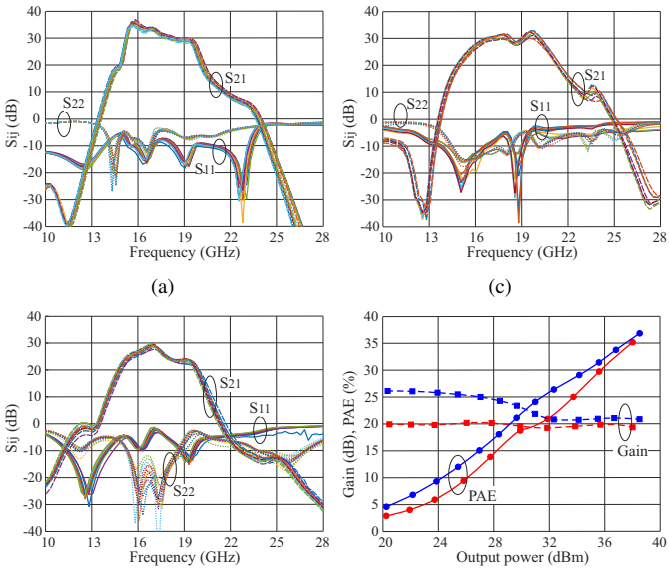

Fig. 2. Measured scattering parameters of (a) MMIC1, (c) MMIC2 and (b) MMIC3 in the respective nominal bias conditions, and measured power sweeps of MMIC3 (d) at 17.3 GHz (blue) and 20 GHz (red) .

VI. Conclusion

This paper discussed three design strategies for the realization of a MMIC DPA for the satellite Ka-band downlink application. Advantages and limitations of the on-chip power combination have been discussed analysing the chips manufactured in the framework of the project GANDALF. The experimental characterization of the designed MMICs confirmed the feasibility of the approaches to reach the target output power and gain on the whole band of the proposed solutions. From the efficiency point of view, differences have been experienced, and the most innovative configuration based on stacking devices demonstrated very promising results.

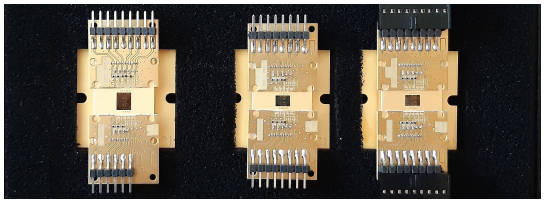

Fig. 3. Photograph of the chips mounted on *ad hoc* test fixtures.

Acknowledgment

The work reported in this paper has been performed under the European Space Agency contract No. 4000123873/18/NL/HK for the development of Single-chip Ka-band Doherty Amplifier. The views presented in the paper represent solely the opinion of the authors and should be considered as R&D results not necessarily impacting the present and future ESA missions.

References

[1] R. Figueiredo, N. B. Carvalho, A. Piacibello, and V. Camarchia, "Nonlinear Dynamic RF System Characterization: Envelope Intermodulation Distortion Profiles—A Noise Power Ratio-Based Approach," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 9, pp. 4256–4271, 2021.

[2] V. Valenta, I. Davies, N. Ayllon, S. Seyfarth, and P. Angeletti, "High-gain GaN Doherty power amplifier for Ka-band satellite communications," in *IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, Jan. 2018, pp. 29–31.

[3] C. Friesicke, P. Feuerschutz, R. Quay, O. Ambacher, and A. F. Jacob, "A 40 dBm AlGaN/GaN HEMT power amplifier MMIC for SatCom applications at K-band," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, May 2016, pp. 1–4.

[4] O. Cengiz, O. Sen, and E. Ozbay, "High power K-band GaN on SiC CPW monolithic power amplifier," in *2014 9th European Microwave Integrated Circuit Conference*, Oct 2014, pp. 548–551.

[5] S. Din, A. M. Morishita, N. Yamamoto, C. Brown, M. Wojtowicz, and M. Siddiqui, "High-power K-band GaN PA MMICs and module for NPR and PAE," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 2017, pp. 1838–1841.

[6] R. Giofrè, P. Colantonio, F. Costanzo, F. Vitobello, M. Lopez, and L. Cabria, "A 17.3–20.2-GHz GaN-Si MMIC Balanced HPA for Very High Throughput Satellites," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 3, pp. 296–299, 2021.

[7] A. Piacibello, R. Giofré, R. Quaglia, and V. Camarchia, "34 dBm GaN Doherty Power Amplifier for Ka-band satellite downlink," in *2020 15th European Microwave Integrated Circuits Conference (EuMIC)*, 2021, pp. 25–28.

[8] F. Costanzo, A. Piacibello, M. Pirola, P. Colantonio, V. Camarchia, and R. Giofrè, "A Novel Stacked Cell Layout for High-Frequency Power Applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 597–599, 2021.

[9] A. Piacibello, F. Costanzo, R. Giofré, R. Quaglia, P. Colantonio, M. Pirola, and V. Camarchia, "Evaluation of a stacked-fet cell for high-frequency applications (invited paper)," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 34, no. 5, p. e2881, 2021. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/jnm.2881