A Ka-band 33 dBm Stacked Power Amplifier Cell in 100 nm GaN-on-Si Technology

A Ka-band 33 dBm Stacked Power Amplifier Cell in 100 nm GaN-on-Si Technology

Chiara Ramella[1], Marco Pirola[1], Paolo Colantonio[2]
[1]*Dept. Electronics Telecommunications, Politecnico di Torino*, Torino, Italy
[2]*Dept. Electronic Engineering, Univ. Roma Tor Vergata*, Roma, Italy
chiara.ramella@polito.it, paolo.colantonio@uniroma2.it

***Abstract*—This work presents a self-biased 2-stacked power amplifier cell that shows, in simulations, an output power in excess of 33 dBm and gain and power added efficiency (PAE) above 6 dB and 27 %, respectively, over a 33.5 GHz to 39.5 GHz bandwidth. The cell has been developed on a commercial 100 nm GaN-on-Si process, applying space derating rules at center frequency, where the output power is almost 33.8 dBm, the associated gain is higher than 7 dB and PAE is above 35 %.**

***Index Terms*—stacked PA, MMIC, GaN-on-Si, mm-wave PA**

I. Introduction

Monolithic microwave integrated circuits (MMIC) power amplifiers working in Ka-band are key enabling components for a number of scientific and commercial applications, such as wireless communications, automotive radars and satellite radio. Above 30 GHz, achieving high power density at the power amplifier (PA) chip level is a very challenging task, even resorting to gallium nitride (GaN) technology, which can provide several watts per millimeter [1]. Indeed, at high frequency, the periphery of each single device employed should be kept small to limit the effect of parasitic reactances and finger-to-finger phase misalignments, which both result in poor power gain, and thus a considerable number of devices must be adopted in the final stage.

When many devices are required, the common solution of paralleling them to increase the output current presents several drawbacks in terms of chip size and cost, power gain and reduced optimum output impedance and complexity of the output combiner, with consequent higher losses and limited bandwidths. The stacked power amplifier, first introduced in [2], exploits series combination of N devices to achieve high output power. With proper biasing and loading, uniform voltage distributions can be obtained across the stacked transistors and the total output voltage is raised by N times, while keeping the output current the same of that of a single device. This technique allows to bias the system with voltages exceeding the breakdown voltage of the single device and thus is usually adopted in intrinsically low-breakdown technologies, such as CMOS [3]and GaAs [4]. However, it also brings other advantages that can be profitably exploited in GaN technology [5]: reduced chip area, higher gain (ideally almost 3 dB by stacking 2 transistors) and increased optimum load impedance, which, in turn, means easier output matching and lower losses.

At very high frequency, the phase de-tuning among stages introduced by device parasitics can become detrimental for output power, gain and efficiency. Thus, the design of the stacked cell layout and of the interstage matching networks becomes crucial. Moreover, the number of stacked transistors should be limited (two or three) even for high-cut-off-frequency technologies, since the gain boost provided from any additional stage may be overwhelmed by the losses introduced by its parasitics and the elements added to compensate for them.

As first proposed in [6], a stacked cell can be regarded as a 3-terminal "macro-device" which can then be replicated in cascade configuration or combined in any way, from classical paralleling to advanced architectures like, e.g., the Doherty power amplifier [7]. To limit the complexity of bias routing when combining more cells, a self-bias approach should be pursued, to avoid additional lines for the CG stages.

This works presents a self-biased 2-stacked power amplifier cell designed on 100 nm GaN-on-Si technology. According to simulation results, the cell is capable of providing more than 33 dBm (2 W) on a 6 GHz bandwidth around 36.5 GHz (16 % fractional bandwidth) with an associated gain above 6.7 dB on the whole range, and with a maximum of 7.1 dB at center frequency. Considering that gain of the device alone at center frequency is around 4.5 dB only, the advantage of the stacked architecture is significant. The cell has been designed to be compliant with space derating constraints [8] at center frequency, in terms of supply voltage and maximum device junction temperature. Note that the latter is particularly critical given the relatively low thermal performance of the Si substrate of the selected technology with respect to widely adopted SiC one [9].

II. Theory of operation

A stacked power amplifier consist of a number N of identical devices (device size and bias condition) that are DC and AC connected in series. Therefore, ideally, the drain voltages of each transistors add up, while their drain current is the same, as shown in Fig. 1 reporting the basic stacked PA circuit for the simplest case of $N = 2$.

The first stage is in common-source (CS) configuration, while the other $(N - 1)$ stages are in pseudo-common-gate (CG) configuration, i.e., at the operating frequency f_0, they are not grounded but connected to a finite impedance fixed by means of a gate capacitance C_{g}. The maximum number of

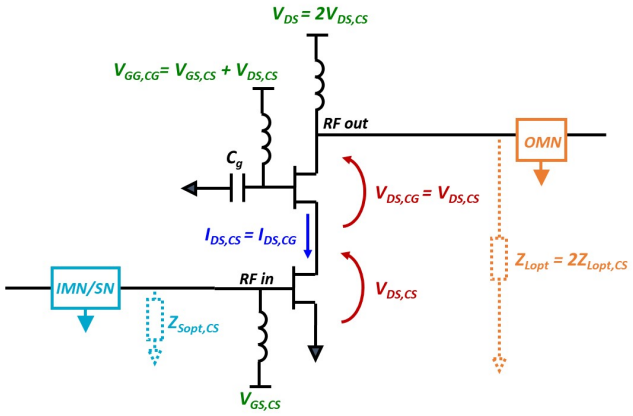

Fig. 1. Schematic diagram of a 2-stacked cell. The drain bias voltage is 2 times that of the CS stage alone, the drain-source current is the same for both devices, thus the gate-source voltages must be the same. The input impedance of the stacked cell is approximately the same of the CS stage alone, and thus the input matching (IMN) and stabilization (SN) networks are the same. The optimum output termination of the cell, instead, is 2 times higher that of the CS alone, which relaxes the design of the output matching network (OMN).

devices that can be stacked at a specific operating frequency is limited by the technology cut-off frequency f_{T} as [10]

$$N_{\max} = \left\lfloor \frac{1}{\ln(1 + f_0/f_{\mathrm{T}})} \right\rfloor \tag{1}$$

The stacked power amplifier architecture has been extensively analyzed from sub-RF to millimetre-wave frequencies [2], [11], [12], however, for the sake of clarity, the main concepts are briefly recalled in this Section, applied to the present case of a 2-stacked structure.

The gate capacitance C_{g} on the CG stage (see Fig. 1) represents a key element of the stacked PA, distinguishing it from a cascode. It forms a capacitive voltage divider with the input capacitance (C_{gs}), thus allowing for some gate voltage swing also at this terminal. This implies that part of the output signal of the CS is drawn toward the gate of the GC (*gate leakage*), which practically slightly reduces the gain of a stacked PA with respect to a cascode PA with the same devices. On the other hand, this approach reduces the draingate and drainsource swings under large-signal conditions, allowing reliable transistor operation under large voltage swings. Most important, the gate capacitance modifies the input impedance $Z_{\mathrm{in,CG}}$ that the CG stage presents to the CS drain and thus allows tuning the matching between the two stages. In particular, for frequencies that are much lower compared to the device cut-off, it allows for optimum power matching. In fact, assuming $f_0 \ll f_{\mathrm{T}}$, the output and feedback parasitic capacitances are assumed to be negligible, the devices can be considered unilateral, the voltage swings of both devices are in phase and the optimum load impedance of the CS device is purely real ($Z_{\mathrm{Lopt,CS}} = R_{\mathrm{Lopt,CS}}$) while that of the CG is simply $Z_{\mathrm{Lopt,CG}} = 2R_{\mathrm{Lopt,CS}}$. The real part of the input

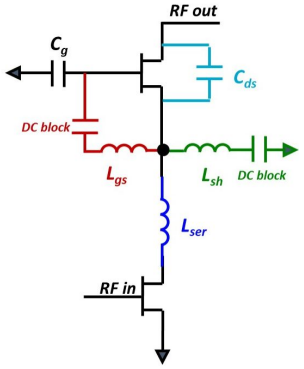

Fig. 2. Inter-stage matching networks: (blue) series inductance, (red) gate-source inductance, (green) shunt inductance, (cyan) feedback capacitance.

impedance of the CG stage is

$$\Re\{Z_{\mathrm{in,CG}}\} = \frac{1 + \frac{C_{\mathrm{gs}}}{C_{\mathrm{g}}}}{g_{\mathrm{m}}} \tag{2}$$

where g_{m} is the transconductance of the device. Thus, if $R_{\mathrm{opt,CS}} > 1/g_{\mathrm{m}}$, it is possible to find a value for C_{g} that matches the CS stage as

$$C_{\mathrm{g}} = \frac{C_{\mathrm{gs}}}{g_{\mathrm{m}} R_{\mathrm{Lopt,CS}} - 1} \tag{3}$$

At high frequencies the reactive parasitic of the devices start playing a crucial role. Due to their effect, in fact,

- the devices are no more unilateral (input impedance depends on drain loading condition)
- the input impedance of the devices becomes increasingly reactive and thus cannot be approximated by its real part only
- the optimum load impedance of the devices becomes inductive to compensate for the output capacitance
- the voltage waveforms across each drain-source terminal are no more in phase (*waveform de-phasing*)

Moreover, the lines that physically connect the stages introduce large phase rotations which can either compensate or worsen waveform de-phasing due to active device parasitics.

Therefore, an inter-stage matching network (ISMN) is needed to recover proper matching and operation of the stacked devices. Different approaches have been proposed so far, as shown in Fig. 2: (1) the series inductance [2], which can be practically implemented through inductive microstrip interconnection lines among the stages; (2) the feedback (drain-source) capacitance [11], which can compensate or reduce gate leakage; (3) the shunt inductance [13], which has the advantage of allowing for separately tuning the real and imaginary part of $Z_{\mathrm{in,CG}}$; and (4) the gate-source inductance [12], which, instead of minimizing the gate leakage, profitably exploits it to achieve matching, as shown in Fig. 3.

The inter-stage matching network, clearly introduces a power loss, due to both ohmic losses in the passive components and to non-ideal matching and consequent drain-source voltage phase misalignment (mismatch losses). The

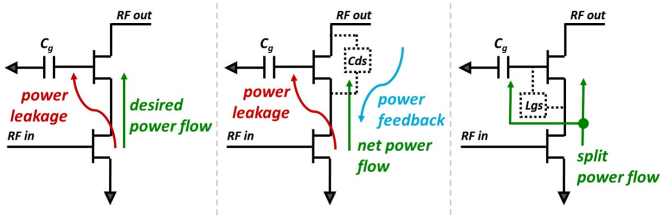

Fig. 3. The gate leakage issue in stacked PAs: (left) principle and possible solutions through (mid) feedback capacitance and (right) gate-source inductance.

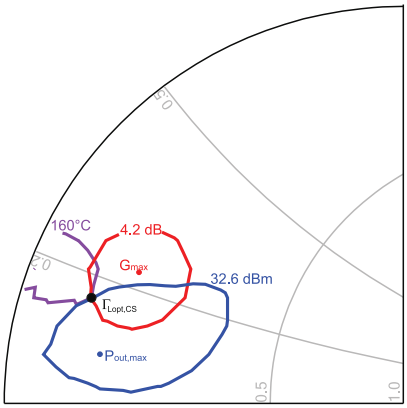

Fig. 4. CS device 1 dB compression load-pull contours at 36 GHz: (blue) output power, (red) power gain and (purple) junction temperature. The optimum load $\Gamma_{\mathrm{Lopt,CS}}$ (big black dot) is at the intersection among 160 °C limit and highest possible power and gain.

total ISMN loss is known as *stacking efficiency* and is the most crucial parameter of a stacked PA working at high frequency, as it can completely overwhelm all the advantages of the stacked architecture. Therefore, during design, the proper architecture and layout of the stacked cell must be carefully evaluated and all ISMN elements must be simulated electromagnetically (EM) [14].

III. MMIC Design

The stacked cell has been designed to be used as a basic element for the development of more complex PA structures in Ka-band. The selected center frequency is 36 GHz and the minimum target output power is 1.5 W, a value that should allow to comfortably reach 10 W by combining 8 cells in parallel. As a further constraints, the cell has been conceived to comply with space derating rules in narrow-band operation.

The selected technology is the OMMIC 100 nm gate-length GaN-on-Si process D01GH, which is able to provide more than 2.5 W/mm output power density at the target frequency around 36 GHz [1]. The cell is based on the 8×75 μm device, so that the total periphery of the 2-stacked structure will be 1.2 mm.

As a first design step, the analysis of the 8×75 μm device in CS configuration, was performed. Accounting for space derating, the drain voltage was set to 11.25 V, while the gate voltage was set to -1.75 V obtaining deep class-AB operation with $I_{\mathrm{D,q}}$ below 15 mA (2.5 % of $I_{\mathrm{D,max}}$). A such low quiescent bias current is selected in order to minimize power consumption in absence of input signal, which is crucial for pulsed-signal applications, especially in space environment where heat dissipation is cumbersome. The device is unconditionally stable above 23 GHz and was made unconditionally stable at all frequencies trough an ideal-component stabilization network composed of a parallel RC in series with the gate and a series inductance on the gate bias line. Load-pull simulations at 36 GHz have been carried out, posing particular attention to the junction temperature of the device, which should be below 200 °C for device reliability and below 160 °C for space applications. Harmonic control was deliberately neglected, since, given the complexity of the stacked architecture itself, adding also harmonic matching would result unfeasible. The device, however, proved to be quite insensitive to all harmonic terminations, except for the case of a second harmonic phase very close to 180°, which should be avoided. The results are shown in Fig. 4 [9]: the maximum output power attainable is above 34 dBm, however, due to the relatively poor thermal properties of the Si substrate, the associated dissipated power would yield a junction temperature above the maximum limit of 160 °C. The optimum load $\Gamma_{\mathrm{Lopt,CS}}$ should be thus selected as the best compromise among output power, junction temperature and gain i.e. at the intersection among the 160 °C contour and the highest-value contours of output power (32.6 dBm) and gain (4 dB).

Given the high operating frequency, a layout-aware, EM-based design of the cell is mandatory, since coupling effects among adjacent lines and components, not predicted by circuit-level simulations, can be detrimental for stacking efficiency [14]. The layout of the active device, shown in Fig. 5 (left), could have been modified targeting the most compact cell. However, to avoid possible model inaccuracies, the original device layout has been maintained. Moreover, since the device model includes 2 symmetric source terminals, all elements have been designed so as to keep the whole cell symmetrical along its central horizontal axis, as shown Fig. 5 (right). Finally, the cell includes a self-bias network that makes it an actually 3-terminal macro-device.

A 2-stacked cell requires three different bias voltages: the total drain voltage $V_{\mathrm{DS}} = 2V_{\mathrm{DS,CS}} = 22.5$ V, the CS gate voltage $V_{\mathrm{GS,CS}} = -1.75$ V and the CG gate voltage $V_{\mathrm{G,CG}}$ which must ensure $V_{\mathrm{GS,CG}} = V_{\mathrm{GS,CS}}$ and thus must be set to $V_{\mathrm{G,CG}} = V_{\mathrm{GS,CS}} + V_{\mathrm{DS,CS}} = 9.5$ V. The simplest choice for the cell biasing is to add a separate bias line for $V_{\mathrm{G,CG}}$, typically including a series resistor to improve stability [12]. This approach gives the opportunity to optimize the voltage value in measurement so as to compensate for device non-idealities, and is typically preferred in single-cell stacked PA implementation. However, when many stacked cells need to be combined, the routing of this additional line may become critical. To overcome this issue, a self-bias network is adopted. In the self-bias approach, the gate-source voltage of the CG stage is derived from a higher DC voltage of the circuit, the

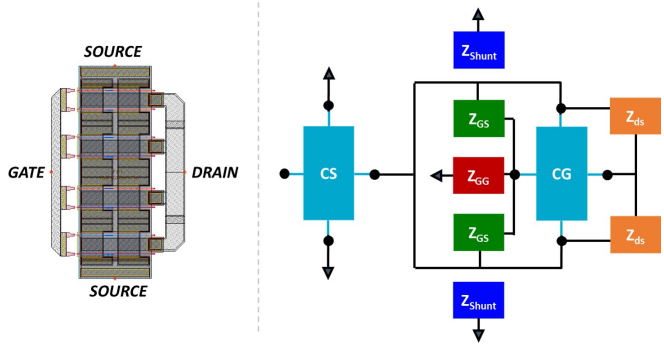

Fig. 5. Layout consideration: (left) device layout with 2 symmetric source terminals and (right) block diagram of a symmetric stacked cell including all possible ISMN elements. The CS drain current is split into two symmetrical paths going to the two source terminals of the CG stage, the gate capacitance, with any other possible element in parallel to it, is kept at the center of the structure, while any gate-source, drain-source or source-ground (shunt) element is split into two parallel blocks connected symmetrically to the 2 CG source terminals.

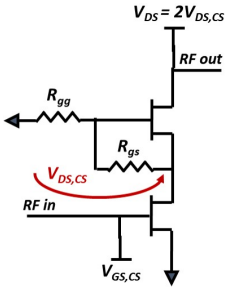

Fig. 6. Stacked cell in DC conditions.

CS drain voltage in this design, by means of a resistive voltage divider.

Fig. 6 reports the schematic of the stacked cell in DC operating conditions, where only the self-bias resistors $R_{\rm gg}$ and $R_{\rm gs}$ are present. The gate-source voltage of the CG stage is derived as

$$|V_{\rm GS,CG}| = V_{\rm DS,CS}\frac{R_{\rm gs}}{R_{\rm gs}+R_{\rm gg}} \tag{4}$$

The value of both resistors must be high enough in order not to affect RF performance. Moreover, they must guarantee that the DC current that flows through $R_{\rm gs}$ is sufficiently small compared to the total quiescent current $I_{\rm D,q}$. On the other hand, they must be physically implementable with MMIC technology, which limits their maximum value to few kilo-ohms.

Al possible ISMN configurations of Fig. 2 have been tested: both the series inductance alone and the feedback capacitance approaches proved to be unfeasible as they actually move the impedance levels away from the optimum value. Shunt inductance matching worked pretty well at circuit-level, but, once EM simulated showed a gate leakage far higher than expected, due to an unavoidable EM coupling between the gate capacitance and the interconnection lines from the CS drain to the CG source terminals [14].

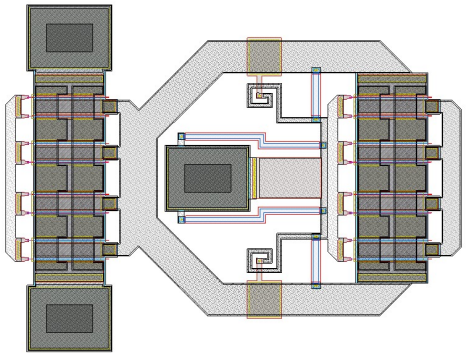

Fig. 7. Stacked cell layout.

Therefore, the gate-source inductance approach (see Fig. 3) was selected, deliberately coupling the CG gate with its source terminals to achieve the desired matching. The gate-source inductance approach, makes the values of $C_{\rm g}$, $L_{\rm gs}$ interdependent and thus requiring a careful EM-based optimization.

Fig. 7 reports the final layout of the EM optimized stacked cell. A single gate capacitance is adopted, while both self-bias resistors are split into 2 parallel ones (3.3 kΩ and 18 kΩ for $R_{\rm gs}$ and $R_{\rm gg}$, respectively). Two parallel spiral inductances are used for $L_{\rm gs}$ while the necessary DC-block gate-source capacitance has been integrated in the drain-source interconnection lines.

IV. Simulated Stacked Cell Performance

In this Section the large-signal CW simulation results of the stacked cell are reported. The cell is loaded at the CG drain with a lumped impedance of value $2Z_{\rm Lopt,CS}$, while at the CS gate the same stabilization network adopted for the analysis of the CS device alone is adopted.

Fig. 8 and Fig. 9 report the cell performance in the 33.5 GHz to 39.5 GHz range: in this bandwidth the output power is always above 33 dBm (2 W), with an associated gain above 6 dB and power added efficiency (PAE) above 27 %. The junction temperature in bandwidth is below the maximum value for terrestrial applications, that is 200 °C. The operating bandwidth is 6 GHz, that is more than 16 % fractional bandwidth and it is limited at low frequency by gain, which drops below 6 dB, and at high frequency by the CS junction temperature which would exceed the maximum limit for long-term reliable operation.

Fig. 10 and Fig. 11 report the cell performance at 36 GHz: output power around 33.8 dBm (2.4 W) is achieved, which is well above the minimum target value of 1.5 W. In this condition, the associated gain is in excess of 7 dB, PAE is above 35 %, and the junction temperature of both CG devices stays below the 160 °C limit compliant with space derating.

V. Conclusions

A 2-stacked power amplifier cell in 100 nm GaN-on-Si technology working in Ka-band has been presented, which

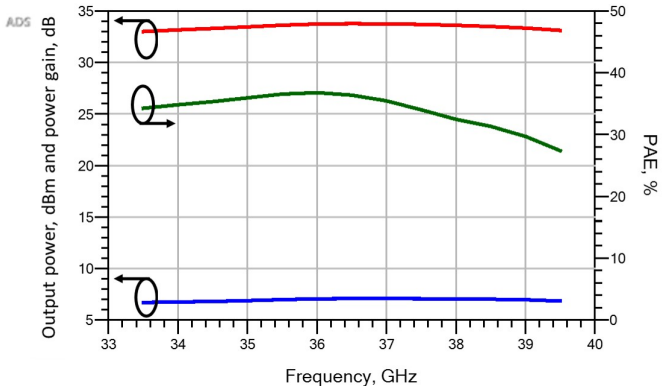

Fig. 8. Frequency behavior of the stacked cell at nominal output power: (red) output power, (blue) power gain and (green) PAE.

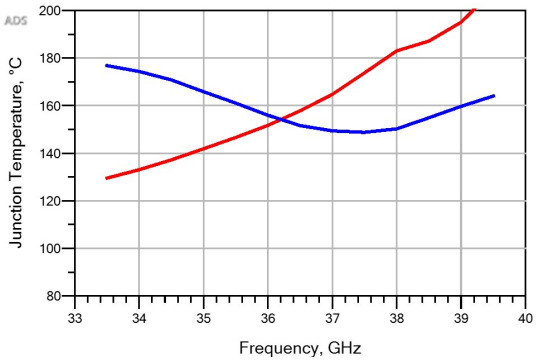

Fig. 9. Frequency behavior of the stacked cell at nominal output power: junction temperature of the (red) CS and (blue) CG stage.

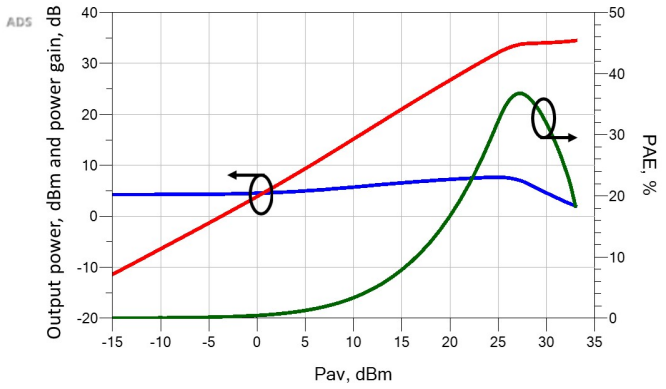

Fig. 10. Power sweep results at 36 GHz: (red) output power, (blue) power gain and (green) PAE.

is intended to be used as unit cell for developing high-frequency and high-power PA around 36 GHz. Despite the thermal limitations posed by the Si substrate, simulations show that the cell can deliver more than 33 dBm in a 6 GHz bandwidth around 36.5 GHz, with associated gain and PAE in excess of 7 dB and 27 %, respectively. At center frequency, the output power is almost 33.8 dBm, with associated gain and PAE of 7 dB and 35 %, respectively. Moreover, in narrow-band

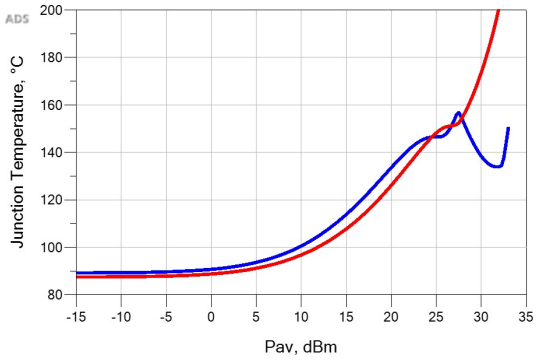

Fig. 11. Power sweep results at 36 GHz: junction temperature of the (red) CS and (blue) CG stage.

conditions around 36 GHz, the maximum junction temperature of the devices is kept below 160 °C, thus, at this frequency, the cell can also be effectively exploited for space applications.

References

[1] J. Moron, R. Leblanc, F. Lecourt, and P. Frijlink, "12W, 30% PAE, 40 GHz power amplifier MMIC using a commercially available GaN/Si process," in *2018 IEEE MTT-S Int. Microw. Symp.*, June 2018, pp. 1457–1460.

[2] M. Shifrin, Y. Ayasli, and P. Katzin, "A new power amplifier topology with series biasing and power combining of transistors," in *1992 IEEE Microw. Millimeter-Wave Monolithic Circuits Symp.*, June 1992, pp. 39–41.

[3] H. Wu, Q. Cheng, X. Li, and H. Fu, "Analysis and Design of an Ultrabroadband Stacked Power Amplifier in CMOS Technology," *IEEE Trans. Circuits Syst. II*, vol. 63, no. 1, pp. 49–53, Jan 2016.

[4] C. Ramella *et al.*, "Characterization-oriented design of a compact GaAs MMIC 3-stacked power cell," in *2016 Int. Conf. Microw. Radar Wireless Comm. (MIKON)*, May 2016, pp. 1–4.

[5] B. A. Ezzeddine, H. A. Hung, E. Viveiros, and H. Huang, "High-power GaN MMIC PA Over 40-4000MHz," in *2013 IEEE MTT-S Int. Microw. Symp.*, June 2013, pp. 1–4.

[6] A. K. Ezzeddine and H. C. Huang, "The high voltage/high power FET (HiVP)," in *2003 IEEE Radio Freq. Integr. Circuits Symp.*, June 2003, pp. 215–218.

[7] F. Costanzo *et al.*, "A Ka-band Doherty Power Amplifier using an innovative Stacked-FET Cell," in *2019 Conf. Ph.D Research Microelectron. Electron.*, July 2019, pp. 165–168.

[8] F. Scappaviva *et al.*, "10 Watt High Efficiency GaAs MMIC Power Amplifier for Space Applications," in *2008 Eu. Microw. Integr. Circuit Conf.*, Oct 2008, pp. 562–565.

[9] C. Ramella *et al.*, "Thermal-aware GaN/Si MMIC design for space applications," in *2019 IEEE Int. Conf. Microw. Antennas Comm. Electronic Systems (COMCAS)*, 2019, pp. 1–6.

[10] A. Piacibello *et al.*, "A Ku-band Compact MMIC PA based on Stacked GaAs pHEMT cells," in *2018 Int. Workshop Integr. Nonlin. Microw. Millimetre-wave Circuits (INMMIC)*, July 2018, pp. 1–3.

[11] A. K. Ezzeddine, H. C. Huang, and J. L. Singer, "UHiFET - a new high-frequency High-Voltage device," in *2011 IEEE MTT-S Int. Microw. Symp.*, June 2011, pp. 1–1.

[12] Y. Kim and Y. Kwon, "Analysis and Design of Millimeter-Wave Power Amplifier Using Stacked-FET Structure," *IEEE Trans. Microw. Theory Tech.*, vol. 63, no. 2, pp. 691–702, Feb 2015.

[13] T. Fersch *et al.*, "Stacked GaAs pHEMTs: Design of a K-band power amplifier and experimental characterization of mismatch effects," in *2015 IEEE MTT-S Int. Microw. Symp.*, May 2015, pp. 1–4.

[14] C. Ramella, A. Piacibello, V. Camarchia, and M. Pirola, "Electromagnetic Crosstalk Effects in a Millimeter-wave MMIC Stacked Cell," in *2020 Int. Workshop Integr. Nonlin. Microw. Millimetre-wave Circuits (INMMIC)*, 2020, to appear.