Ultralow-Power Digital Control and Signal Conditioning in GaAs MMIC Core Chip for X-Band AESA Systems

Ultra-Low-Power Digital Control and Signal Conditioning in GaAs MMIC Core-Chip for X-band AESA Systems

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***Abstract*—This work presents the design and characterization of an ultra-low-power core-chip for electronically scanned arrays at X-band, implemented in 0.25/0.5 μm E/D-mode GaAs pHEMT technology. In particular, design details are given about the two core functional blocks embedded in the MMIC: a 12-bit phase and amplitude control circuit and a 18-bit serial-to-parallel interface. The serial-to-parallel interface was designed resorting to a custom symmetric device model, expressly conceived for the time domain simulations required for digital circuits. Thanks to the adoption of a differential structure with resistive pull-ups, it achieves a state-of-the-art power consumption of 2.2 mW/bit and nearly 87% yield. The analog circuit includes a 6-bit phase shifter and a 6-bit attenuator. To mitigate risks, two different phase shifter architectures have been developed and are compared in this work, discussing advantages and drawbacks of the different solutions. Since the two designs share the same target specifications, a truly fair comparison can be made not only in terms of performance, but also concerning robustness and repeatability, thus providing useful guidelines for the selection of the most appropriate strategy. In particular, it is shown that one architecture outperforms the other by about 2 dB and 1.5° in terms of insertion loss and RMS phase error, respectively.**

***Index Terms*—GaAs, MMIC, mixed analog digital integrated circuits**

I. Introduction

ACTIVE electronically scanned array (AESA) systems represented a technological breakthrough with respect to passive phased array systems in terms of improved performance, reconfigurability and wide-band capabilities, but also in terms of improved reliability, ease of installation and reduced cost and weight, finding application in mobile communication (5G), space communication and defense systems [1]–[3].

AESA systems include a huge number of independent radiating elements, each one equipped with its own transmit/receive module (TRM), which must therefore be extremely compact and have low weight, low cost and high repeatability. This can be accomplished by reducing the number of microwave monolithic integrated circuit (MMICs) in the TRM and hence by increasing their capabilities to perform different functions. Nowadays the trend is to implement the TRM with only two MMICs: the single-chip front-end (SCFE) and the core-chip (CC), or multi-function chip (MFC).

The SCFE, directly connected to the radiating element, accomplishes the main function of signal amplification in both transmit (TX) and receive (RX) mode, thus embedding an high-power amplifier (HPA), a low-noise amplifier (LNA) and the necessary switching functions for TX/RX signal duplexing. To simultaneously provide high power density and low-noise feature, GaN is at present the most widely adopted technology for the SCFE [4]–[8].

Electronic beam steering and shaping require phase and amplitude control of the RF signal. This signal conditioning function is carried out by the CC/MFC, which therefore requires a programmable phase shifter and attenuator, together with the necessary switches to properly route the RF signals, but also digital controls for all these analog blocks [9]. In fact, since a huge number of control lines is required within a CC/MFC, including a digital serial-to-parallel interface sensibly alleviates control signal routing [10]–[15]. Since such CC/MCF are typically implemented in GaAs technology, the design of digital functionalities is not as straightforward as in Si-based chips, and current consumption may become an issue. In fact, the main challenges in developing compact and efficient CC/MFCs are combining a high level of integration with high yield and repeatability and achieving low DC power consumption.

A core-chip operating in the 7.6 GHz-9.1 GHz range has been designed and implemented in a commercial 0.25 μm E/D-mode GaAs pHEMT MMIC technology. The core functionalities of the CC are the 12-bit phase and amplitude control circuit (PAC) and the 18-bit serial-to-parallel interface (S2P), whose first demonstrators were introduced in [16]. In this paper, additional design details are given for both circuits, and CC-level experimental results are presented for the first time. In order to mitigate design risks, two different PS architectures have been developed using standard PDK models provided by the foundry and included in two different CC versions. This allowed for an experimental comparative evaluation in terms of RF performance, sensitivity to process

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TABLE I
MAIN FEATURES OF THE WIN'S PD25-00 PROCESS.

Parameter	E-mode FET	D-mode FET
Trans-conductance	$>$ 730 mS/mm	$>$ 350 mS/mm
Maximum current	$>$ 450 mA/mm	$>$ 360 mA/mm
Breakdown voltage	$>$ 8 V	$>$ 13 V
Threshold voltage	0.15 V to 0.45 V	-1.3 V to -0.7 V
Cut-off frequency	$>$ 60 GHz	$>$ 26 GHz
Gate leakage current	$<$ 1.5 µA/mm	
Turn-on resistance	$<$ 2.6 Ω.mm	$<$ 1.25 Ω.mm
Passives (C and R)	600 pF/mm^2; 120 Ω/□; 50 Ω/□	

variations or model inaccuracy and reliability/yield, of the two PS versions. According to the results obtained, the circuit topologies that minimize the component count (both active and passive) are more robust against process variations and lead to better RMS performance, well in line with state-of-the art results. Concerning the design of the digital circuits, an ad-hoc symmetric Angelov model has been developed to allow for fast and accurate transient simulations. The S2P was optimized for low-power consumption and compactness, achieving state-of-the-art result in terms of consumption per bit (2.2 mW/bit), together with a remarkable yield above 86%.

II. TECHNOLOGY

MMIC technology is preferable in compact AESA systems due to the smaller footprint of the circuit and superior integration level with respect to MEMS or diode counterparts, despite it suffers from higher insertion losses and thus requires external amplification. Recently, Gallium Nitride solutions have been proposed [17], however the maturity level and production costs of this technology are still unsuitable for large-scale applications. Silicon based MMICs offer excellent integration level and technological maturity. However, they suffer from poor RF performance in terms of noise and losses with respect to Gallium Arsenide counterparts.

While GaAs is able to provide better performance and lower RF losses than Silicon, it shows lower flexibility in implementing digital/switching functionalities. For logic circuits, a process featuring both enhancement and depletion (E/D) transistors is preferable [11]. Among other commercial foundries, WIN semiconductor offers a reliable and relatively low-cost E/D-mode GaAs pHEMT process [18]. In particular, the PD25-00 process was selected for the present design, as best trade-off between technological maturity and RF performance at X-band frequencies. This process combines low-noise 0.25 µm gate-length E-mode transistors with high-linearity 0.5 µm gate-length D-mode ones and it has been expressly conceived for monolithic RF control circuits adopting D-mode switches and E-mode digital architectures. The main process features are summarized in Table I. D-mode FETs are optimized for switching applications, from cold-FET analysis (V_{DS} = 0 V) a 0.9 Ω.mm ON-state resistance at V_{GS} = 0.4 V and a 0.25 pF/mm OFF-state capacitance at V_{GS} = -3.3 V have been extracted, while a switching time around 100 ns is reported in [19].

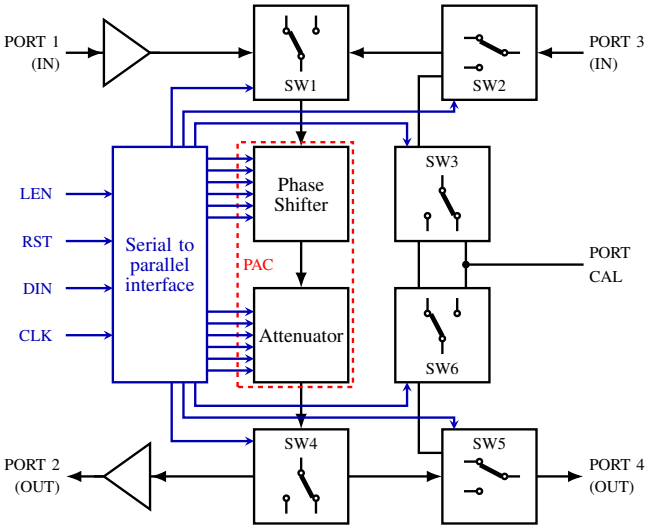


Fig. 1. Block diagram of the core-chip.

III. CHIP ARCHITECTURE

The core-chip architecture is reported in Fig. 1: the PAC is composed of a 6-bit attenuator and a 6-bit phase shifter, for a total of 2^{12} = 4096 possible PAC states. Moreover, 6 switches are required to set the chip operative mode (TX/RX/CALIBRATION/ISOLATION), thus rising the number of CC states to 2^{18}. The routing of a large number of control lines increases the complexity of the antenna digital control architecture at system level and may become practically unfeasible within a large-scale AESA systems. For this reason, the CC includes a 18-bit serial to parallel interface that reduces the number of the control signals to only four, three of which are shared among all the CCs in a synchronous array. Moreover, simplifying the control signal interface helps in reducing the CC area, with consequent benefits on MMIC yield and reliability. Finally, the CC includes TX and RX driver amplifiers to boost gain, noise and linearity of the Transmit-Receive Module (TRM). The most challenging targets of the CC design are: 1) low power consumption; 2) low bias voltage; 3) high yield and reliability and 4) low noise margin.

In the following sections, design details about the S2P and PAC circuits are discussed. These blocks represents the fundamental functionalities of the CC: the former is the enabling element for high integration level, while accuracy and flatness in bandwidth of the PAC performance, especially of the phase shifters, are key elements for a CC/MFC [2].

IV. SERIAL-TO-PARALLEL INTERFACE

The required external control signals are the input data (DIN), the clock signal (CLK), the latch enable signal (LEN) and the latch reset signal (RST). The design specifications for the S2P are summarized in Table II, the most stringent being current consumption: below 4 mA and 20 mA for the positive and negative supply voltage, respectively.

A. Device Model

Microwave transistor models included in the foundries' design kits (PDKs) are typically optimized for harmonic balance

TABLE II
DESIGN REQUIREMENTS FOR THE S2P.

Parameter	Value	Parameter	Value
HI-level IN	[2.3 to 3.6] V	HI-level OUT	[(0 to 0.4] V
LO-level IN	[0 to 0.5] V	LO-level OUT	[-2.4 to -3.3] V
Frequency	$\leq$ 50 MHz	Slew-rate	$>$ 0.2 V/ns
CLK active	rising edge	LEN active	falling edge
DC current	$<$ 4 mA; $<$ 20 mA	Leakage current	$<$ 250 µA

simulations. In fact, RF circuits typically operate in periodic or quasi-periodic conditions and thus are designed and optimized in the frequency domain. However, the design of a digital circuit requires time-domain simulations, where such models show in many cases convergence or even stability issues. This was the case for the selected technology: the PDK transistor models, available only for RF CADs, proved to be unsuitable for the S2P design, leading to extremely slow simulations even with few transistors and huge convergence issues when the number of transistor increased above 10. Moreover, even if the logic devices are symmetrical, i.e., feature interchangeable drain and source terminals, the PDK model is not, since in RF circuits the role of each terminal is defined *a priori*. On the contrary, in digital switching applications, the role of these two terminals is determined by the circuit instantaneous operating condition.

To overcome these issues, a simplified ad-hoc model was extracted based on the symmetrical Angelov/Chalmers non-linear model included in Keysight ADS environment [20], [21]. The key transitor's features for transient simulation of the CC digital part are the output current-voltage dynamic, the clamping effect due to the (symmetrical) input diodes and the loading effect among interconnected devices due to the intrinsic device reactances. The digital operating frequency is very low compared to the cut-off of the selected technology, thus devices can be modeled with a nonlinear static model, adopting time- and power-invariant reactances hence relieving convergence and stability issues, and speeding up simulations. The model parameters have been extracted by fitting the DC characteristics (drain current) and DC-10 GHz S-parameters in both cold-FET (parasitics, diodes) and hot-FET (intrinsic reactances) bias conditions simulated with the PDK model. The logic devices included in the original PDK are the 1×5 µm and the 1×10 µm E-mode and D-mode transistors. E-mode devices of both sizes have been exploited in the S2P, thus, for improved accuracy, two independently optimized parameter sets have been extracted for the two possible gate widths. The extracted model allowed for the fast transient simulations required for the S2P design. The final analysis of the complete S2P, counting more than 500 transistors, requires a time-domain simulation up to at least 1 µs for loading a full 18-bit sequence at the 25 MHz nominal operating frequency. Thanks to the ad-hoc model, such simulations can be completed in less than a minute.

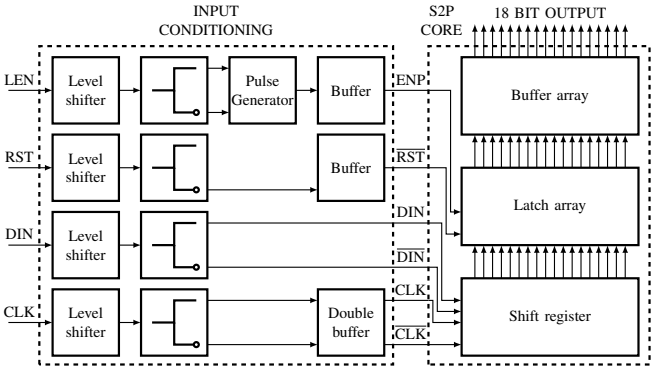


Fig. 2. Block diagram of the S2P.

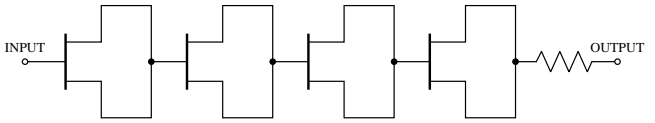


Fig. 3. Level shifter: the 4 FETs behave as diodes providing roughly 0.8 V drop each. The input dynamic is 0 V to 3.3 V. Considering also the loading effect of the splitter/inverter circuit the final internal dynamic of the S2P is -3.3 V to -2.4 V.

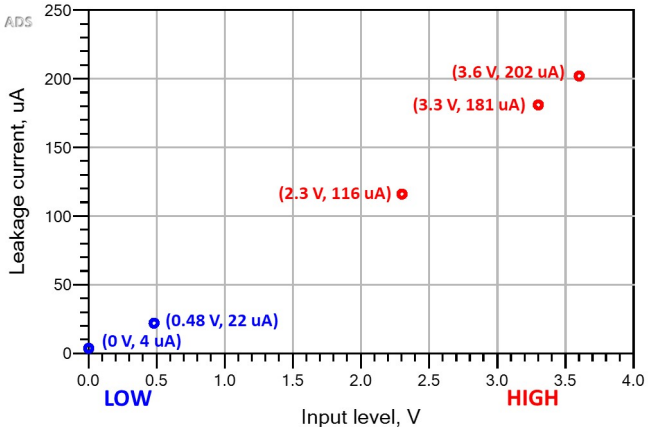


Fig. 4. Simulated S2P input leakage current (same for all inputs).

B. Design

As depicted in Fig. 2, the S2P is composed of two sub-blocks, namely the input conditioning section and the S2P core, where the actual serial-to-parallel conversion takes place. The latter is composed by a fully modular structure developed on three cascaded levels [13], [22]: 1) a synchronous shift register driven by the clock signal, 2) a latch array that maintains or flushes to the output the register's bits according to the enable input signal and 3) an output buffer to provide the required voltage levels (see Table II) and driving currents for the analog modules. Transferring such modularity at layout level, it is straightforward to increase or reduce the number of bits, which becomes just a matter of chip area occupation. In fact, for clock frequencies below a few hundred of megahertz, the transmission line delay on the control inputs, in the order of tens of picoseconds, does not compromise the synchronous behavior of the digital state machine.

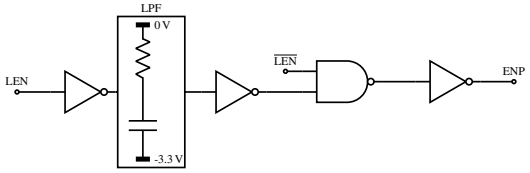


Fig. 5. Latch pulse generator.

1) Input conditioning: The block diagram of the input conditioning section is included in Fig. 2. As indicated in Table II, the S2P inputs must be compatible with LVTTL/CMOS logic, with nominal LO/HI values of 0 V and 3.3 V, respectively. These levels are translated into an internal logic swing for the S2P between -3.3 V (LO) and -2.4 V (HI) by means of the circuit shown in Fig. 3. To limit current sinking form the inputs and decrease sensitivity to voltage variations, four cascaded E-mode FETs, connected to behave as diodes, have been exploited. The internal voltage dynamic has been selected as best trade-off between noise margins, to avoid spurious multiple-bit shifting, and input current. The designed circuit achieves proper operation of the S2P for all input levels within the tolerances indicated in Table II and with input leakage currents within 200 μA, as shown in Fig. 4.

Differential logic circuits, as those used in the S2P, require non-overlapping complementary signals. Therefore a dedicated spiltter/inverter circuit is inserted in cascade with the level shifters of all inputs. Indeed, the latch reset mechanism does not need complementary driving. However, to maintain block symmetry and uniform delay across inputs the same circuit is adopted also to obtain the $\overline{\text{RST}}$ signal.

The latch circuit is designed so as to flush the stored bit to its outputs when the enabling signal (ENP) is HI. The desired operation is to have a transition-controlled bit transfers, therefore a HI-to-LO transition in the external latch enable signal (LEN) must be converted into a HI state for the internal ENP signal. However, keeping the ENP signal HI for too long time may cause instability and multiple spurious changes of the output word. To prevent this issue, the external LEN transition is converted into a very short ENP pulse that is high for only about 10 ns. This is accomplished by means of a mixed analog/digital monostable circuit, shown in Fig. 5, that exploits the time constant of an RC low-pass filter to create a pulse with fixed width.

Finally, since clock, enable and reset input signals must simultaneously drive 18 cells, common-source buffer amplifiers are inserted in cascade to all these inputs to boost their current supply capacity.

2) S2P core: A more detailed schematic of the S2P core circuit is given in Fig. 6. As power consumption and latency in a S2P architecture are mainly determined by the storage elements [23], the main challenge of the S2P design is to develop a compact, fast and low-power basic storage cell, namely a level-controlled latch (LL), based on which all high-level logical functions (e.g. flip-flops) can be implemented. Achieving cell compactness is difficult in GaAs technology since, contrarily to Si technology, it offers only few metallization levels (two in the present case). As a result, a careful

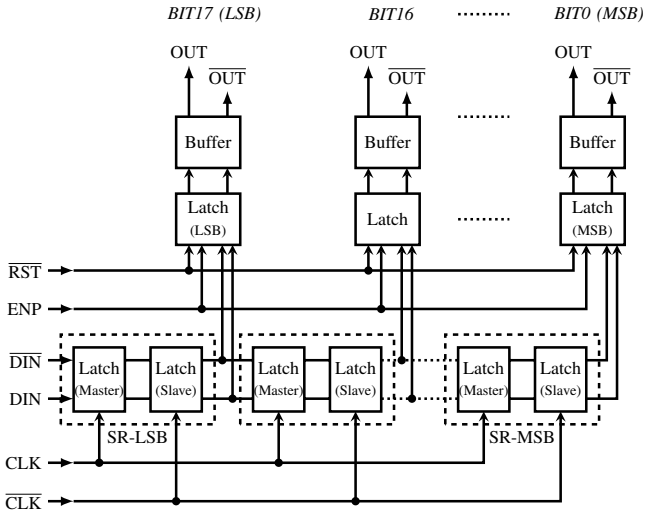


Fig. 6. Detailed block diagram of the S2P core section.

layout optimization must be pursued [22].

As achieving a high yield is a key goal of the S2P design, circuit simplicity and minimized transistor count must be pursued. E/D technology allows for several logic families to be implemented, such as source follower buffered FET (EDSF,EDSFD,SFED) and super-buffered FET (EDSB) logics [24]. Despite showing relatively wide noise margins, all these logics require a large number of transistors, which negatively impacts on the yield and implies high current consumption and large area occupation. Therefore, in this design NOT and NAND logic gates are implemented with E-mode transistors in common-source configuration, as in Direct Coupled FET logic (DCFL), but with resistive pull-ups replacing D-mode FETs [16]. Moreover, as shown in Fig. 7, a differential architecture, inspired by CMOS Cascade Voltage Switch Logic (CVSL) differential latches [25] has been preferred. The differential structure provides fast transitions and good noise margins without needing buffer FETs, hence reducing the transistor count. Resistive pull-ups ensure higher yield with respect to active pull-ups, thanks to the lower spread of MMIC passives with respect to active device's parameters. Moreover, resistive pull-ups allow for reducing power consumption, a main requirement of this design. Their value, however should be optimized, trading off between commutation speed and current consumption, as shown in Fig. 8. The selected value, around 50 kΩ, allows for less than 2 ns commutation speed and around 40 μA current consumption per gate.

Despite the simplicity of the adopted NOT and NAND blocks, good noise margins are obtained together with a compact layout of the latch cell (roughly 100 μm×110 μm). Nonetheless, to further improve spurious transition rejection, and to ensure at the same time a more accurate synchronization, a transition-controlled master-slave D-flip-flop cell (FF) was exploited to implement the shift register, obtained by cascading two complementary driven latch cells as shown in Fig. 10.

Finally, an array of output buffers (OB), based on the shifting/inverting circuit shown in Fig. 9, is adopted to set

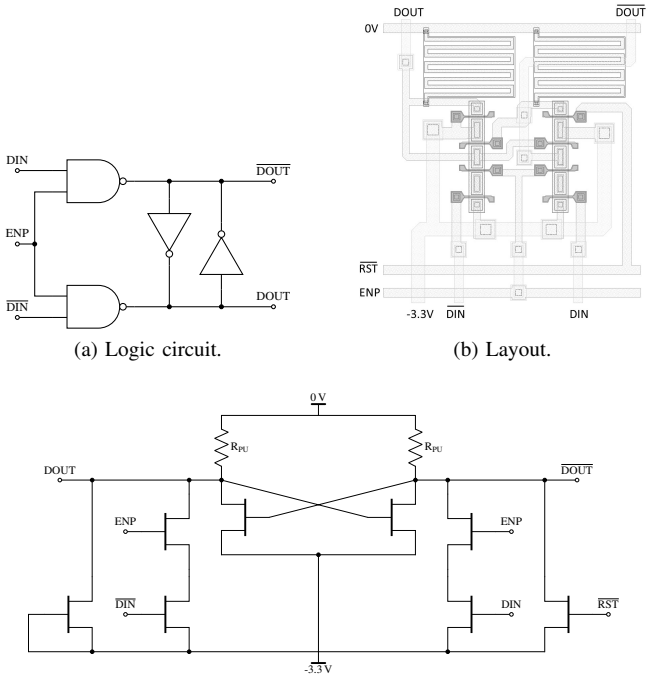


Fig. 7. Latch circuit.

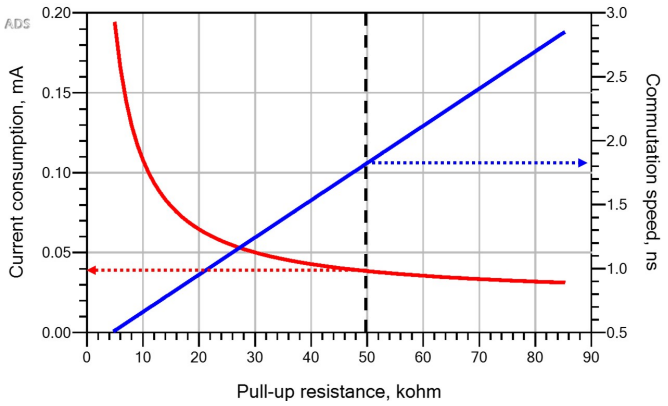


Fig. 8. Simulated current consumption and commutation speed (delay between state transition at input and at output) of a single NOT gate as a function of the pull-up resistor value. The gate is loaded with another NOT gate to simulate the actual operative loading condition.

the output HI/LO levels to the desired values (0.4 V/-3.3 V) and to increase the output current. In the same figure, the circuit adopted to obtain the 0.4 V reference from the available supplies is also reported. The complete layout of the S2P converter is shown in Fig. 10 and it is obtained by replicating 18 times the basic FF+LL+OB structure reported in the inset. As can be noticed, the flip-flop layout was individually optimized to occupy the same area of the latch cell in the horizontal direction. The total 18-bit S2P size is 2.5 mm×0.5 mm, that means 0.07 mm^2/bit, and includes roughly 500 transistors. This results outperform those reported by the authors in [13], where the area occupied by the 13-bit S2P was 2.7 mm×0.8 mm (0.17 mm^2/bit) and the transistor count was nearly double.

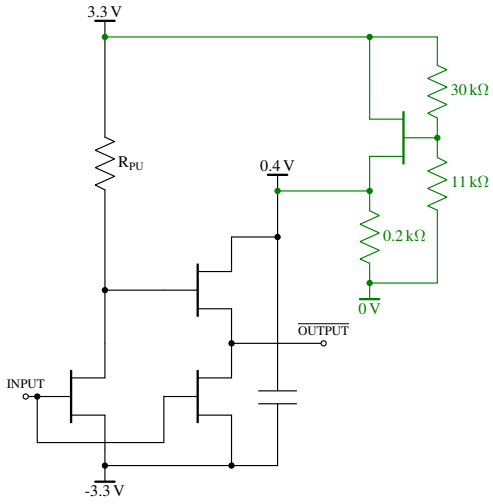


Fig. 9. Basic structure adopted in the output buffers (black circuit, half of a buffer cell): level-shifting/inverting stage. The input dynamic is from -3.3 V to -2.4 V, while the output dynamics goes from -3.3 V to 0.4 V. The 0.4 V reference is generated with the circuit reported in green. In this circuit the HEMT periphery is 4×10 µm and was obtained by paralleling four 1×10 µm transistors.

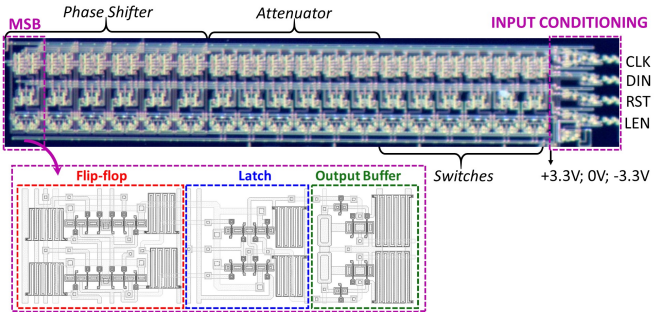


Fig. 10. Microscope picture of the S2P and layout of a single bit (FF+LL+OB). The occupied chip area is less than 0.12 mm×0.4 mm for the single bit and less than 2.5 mm×0.5 mm for the whole S2P.

C. Simulation and Measurement Results

Fig. 11 shows the S2P simulation results at the nominal clock frequency of 25 MHz, demonstrating proper signal waveforms and correct S2P behavior as well. The maximum operating frequency is limited to 50 MHz by the pulse width of the latch enable signal ENP. The latter, which must be lower than half clock cycle, was set to nearly 10 ns in the present design to enhance S2P robustness to process variations at 25 MHz.

Thanks to the differential architecture with optimized pull-up resistors (in the range 20 kΩ−100 kΩ), the simulated current consumption is below 12 mA, of which roughly 2 mA are drawn by the input conditioning section. Measurement results on the implemented MMIC are in very good agreement with simulation predictions. Fig. 12 reports the measured DC currents of all the CC samples of the foundry run. Over 330 samples, 286 worked properly, that corresponds to nearly 87% yield for the CC digital part. This remarkable result was achieved thanks to both the high repeatability of the selected technology and the adopted yield-oriented design strategy. On

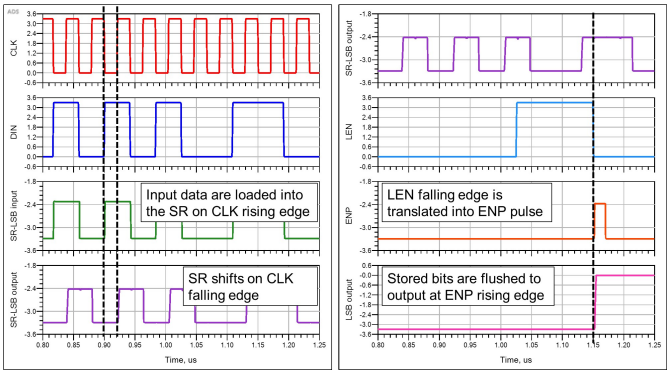


Fig. 11. Simulated behavior of the S2P.

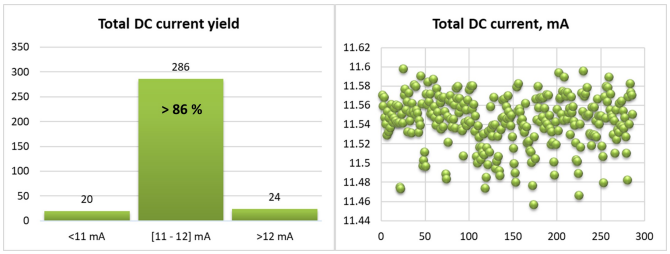


Fig. 12. Measured S2P DC current consumption on 330 CC samples.

TABLE III
COMPARISON OF THE S2P PERFORMANCE WITH THE LITERATURE.

Ref.	Technology µm	Number of bits	Clock freq. MHz	DC power mW/bit
[10]	0.2µm GaAs	16	20	4.4
[26]	0.5µm GaAs	12	N.A.	11
[13]	0.18µm GaAs	13	40	17
[27]	0.5µm GaAs	24	N.A.	11
[14]	0.5µm GaAs	27	10	2.6
[15]	0.5µm GaAs	12	N.A.	6.7
[28]	0.25µm GaAs	4	N.A.	10.6
T.W.	0.25µm GaAs	18	25	2.2

the working samples the average current consumption was 11.55 mA, 10 mA from the negative supply and 1.55 mA from the positive one. The total S2P power consumption therefore results below 40 mW, which means about 2.2 mW/bit, a state-of-the-art result for GaAs serial-to-parallel interfaces, as shown in Table III.

V. PHASE AND AMPLITUDE CONTROL CIRCUIT

In analog beamforming networks a phase shifter and attenuator cascade is introduced to implement the active antenna's desired beam shaping and pointing [2]. The requirements for these two blocks are reported in Table IV, while design details are given in the following Sections.

A. Phase Shifter

As specified in Table IV, a 6-bit phase shifter (PS) is adopted in the designed CC. There are many design possibilities to implement a PS [29]. Among voltage-controlled switchable

TABLE IV
DESIGN REQUIREMENTS FOR THE PAC.

Parameter	Value
Operating frequency	7.6 GHz to 9.1 GHz
DC control voltages	-3.3 V (LO) and +0.4 V (HI)
I/O return loss	≥10 dB
Phase values (0° to 360°)	180°; 90°; 45°; 22.5°; 11.25°; 5.625°
Attenuations (0 dB to 31.5 dB)	16 dB; 8 dB; 4 dB; 2 dB; 1 dB; 0.5 dB

TABLE V
ADOPTED CELL TOPOLOGIES IN THE TWO PS VERSIONS.

Version	180°	90°	45°	22.5°	11.2°	5.6°
A	HP/LP (T/Π)	HP/LP (T/Π)	RF	AP	AP	SDL
B	HP/LP (T/T)	HP/LP (T/T)	HP/LP (T/T)	HP/LP (T/T)	AP	AP

PS, in particular the switched filter, the switched delay line and the loaded line approaches are the most commonly adopted [2]. To mitigate development risks and assess the benefits and drawbacks of the various circuit solutions, two different PS versions have been developed.

For the cells with higher phase shift values (180° and 90°) a switching topology between a high-pass (HP) path and a low-pass (LP) path is implemented. Path selection is realized through a pair of single-pole double-throw (SPDT) switches with series and shunt FETs. The latter are inserted to increase isolation and improve matching at the expense of SPDT insertion loss. A simplified schematic of this type of cell is shown in Fig. 13. The theoretical values of the ideal lumped inductive and capacitive elements appearing in the T- and Π-type networks are found by applying a set of equations available in [30] or [29]. The elements values are function of the impedance to be shown at the RF ports, namely Z_0, the desired phase shift, and the operating frequency. Fig. 14 provides the ideal lumped element values considering $Z_0 = 50\,\Omega$ at 8.4 GHz (mid-band frequency), for both T and Π configurations. Some design considerations can be inferred analyzing these plots: for the 180° cell there is no difference in the ideal lumped element values of the two topologies, and therefore the designer has freedom of choice between implementing a T and Π network. Similar considerations hold also at 90° where the difference between the two topologies is small. On the contrary, for the 45° and 22.5° cells there is a large difference between the T and Π topologies. The inductor and capacitor values on the HP path in the Π topology become, respectively, very large and very small, often unpractical to synthesize, thus making the Π network unfeasible. Therefore, for the mid-value cells the T topology is preferable in both the HP and LP sections. For the intermediate PS cells other possible solutions, based on simpler networks than a HP/LP cell, have been also explored: the reconfigurable filter and the all-pass network reported in Fig. 15a and Fig. 15b. For the lower value cells (11.2° and 5.6°) the ideal lumped element values in Fig. 14 become either too large (HP section) or too small (LP section), thus the HP/LP solution was discarded. Instead, both

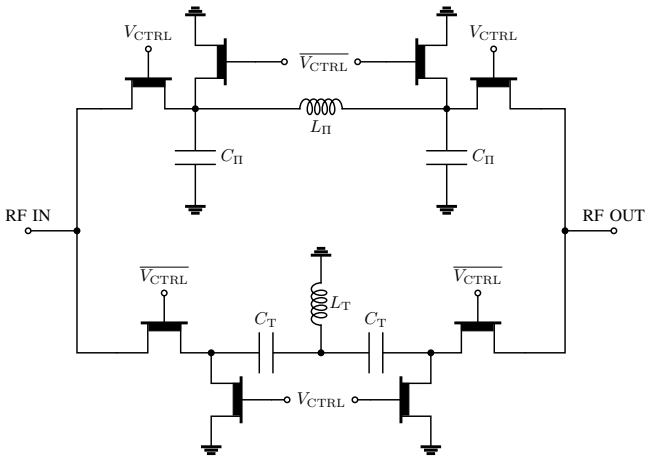


Fig. 13. Simplified schematic of a HP/LP phase shifter cell with mixed T/Π topology.

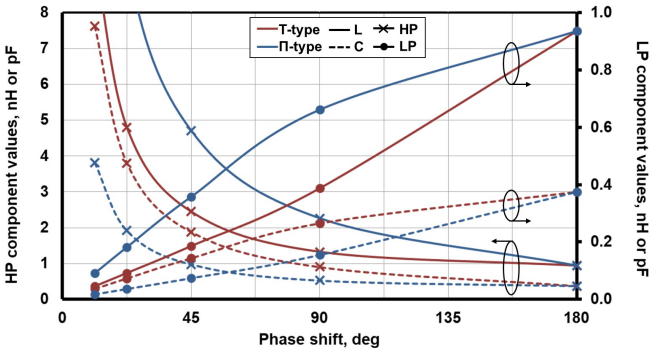
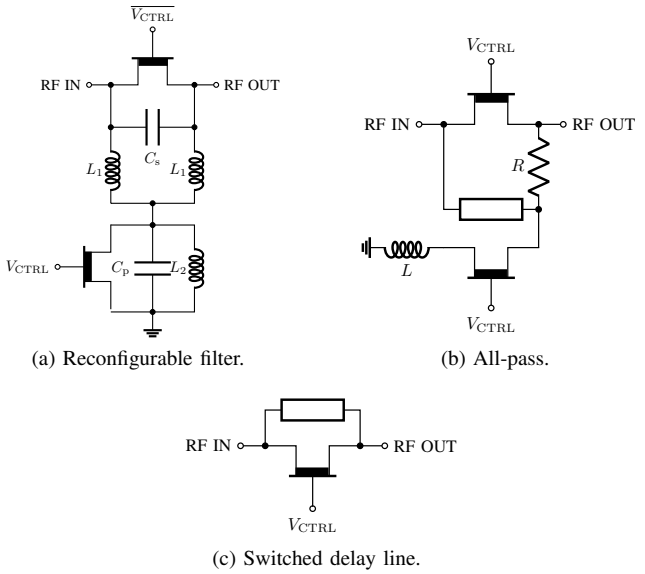


Fig. 14. Ideal inductors (solid) and capacitors (dashed) values of the HP (crosses) and LP (circles) networks considering a 50 Ω termination at 8.4 GHz, for the T (red) and Π (blue) topologies.



(a) Reconfigurable filter. (b) All-pass.

(c) Switched delay line.

Fig. 15. Simplified schematics of the different adopted PS cell topologies.

the all-pass and the switched delay line (Fig. 15c) topologies have been implemented. The detailed design equations for the three solutions shown in Fig. 15 are reported in [31]–[33]. As in the HP/LP case, the reactive elements values are function of termination impedance, operating frequency and desired phase shift.

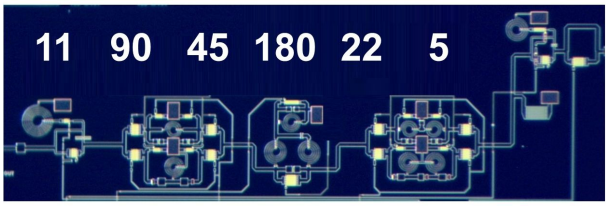
Table V reports the architecture of the two phase shifter versions indicating the solution implemented on each single phase shifting cell. Note that all-pass (AP) and switched delay line (SDL) cells require one control voltage only, while the high-pass/low-pass (HP/LP) and reconfigurable filter (RF) cells need two complementary driving voltages, thus the PS of version B needs one more control line than PS version A. In general, the design guideline followed for version A consists in implementing, where feasible, the more compact and simpler (from a circuital perspective) phase shifting cell. For the higher value cells, the mixed T and Π topology, for the HP and LP path, respectively, is preferred in order to minimize the number of inductors required by the circuit (same configuration of Fig. 13). Instead, for the lowest phase shifting cell the switched delay line is adopted which does not require any lumped element. Version B, instead, is designed implementing the same T topology for the 4 higher phase shifting HP/LP cells and the all-pass topology for the two lower phase shifting cells. Version B is designed minimizing the number of cell topologies appearing in the phase shifter. Finally, circular and rectangular spiral inductors are compared in the two versions. For the same inductance value, the former occupy a larger area than the latter, but their electrical model is expected to be more accurate since the discontinuities are evenly distributed along the geometrical structure [34]. Circular spiral inductors are exploited in version A, where the larger area is not an issue thanks to the minimized number of inductors and cell complexity. Contrarily, version B exploits rectangular inductors to gain compactness and thus the final layout size of the entire PS is $3.6\,\text{mm} \times 1.6\,\text{mm}$ for both versions. Note that the actual height of the cells is within 0.7 mm, however, due to CC layout constraints, the cells could not be deployed all on a same row.

To maintain a fair assessment, the same EM analysis set-up in Keysight Momentum is adopted for the two versions, adopting the EM stack-up provided by the foundry. Table VI reports the FET geometries employed in the two designs for each phase shifting cell. Version A employs smaller series transistors in the higher phase shifting cells and larger series transistor in the lower phase cells. Consequently, the SPDTs in the 180° and 90° cells feature worse insertion loss than the same cells of version B, while the simpler topology adopted in version A for the other cells is expected to give lower insertion losses with respect to version B counterparts. Finally, a 2.5 kΩ resistor is applied to the gate terminal of every transistor. This value is a trade-off between fast switching requirement and adequate isolation of the gate terminal from the control voltage source. Accounting for 0.2 pF gate-source capacitance in the largest FET, the switching speed is in the order of 1 ns in both PS versions.

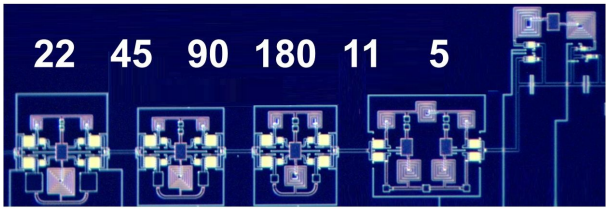
The two PS versions, shown in Fig. 16, have been tested to verify their compliance with the requirements, evaluated in terms of RMS phase error over the operating bandwidth. Fig. 17 shows the measured phase shift versus frequency for the two PS versions. Version A exhibits a more constant

TABLE VI
PHASE SHIFTERS' FET PERIPHERIES (NUMBER OF FINGERS MULTIPLIED BY UNIT GATE WIDTH EXPRESSED IN MICRONS).

Version/config.		180°	90°	45°	22.5°	11.2°	5.6°
A	SERIES	8×30	8×30	8×50	6×25	6×20	6×50
	SHUNT	2×30	2×30	2×75	2×55	2×20	none
B	SERIES	6×50	8×50	8×50	8×50	4×25	2×20
	SHUNT	none	4×20	4×20	4×20	4×25	2×20



(a) Version A.

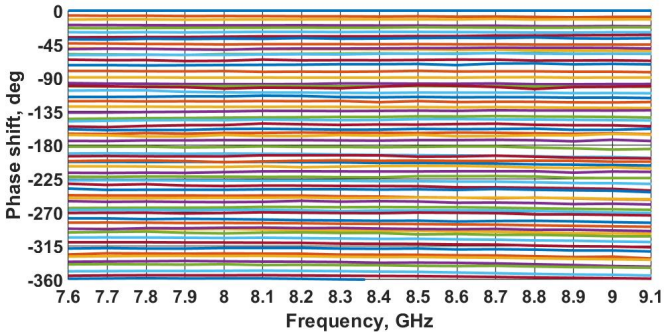


(b) Version B.

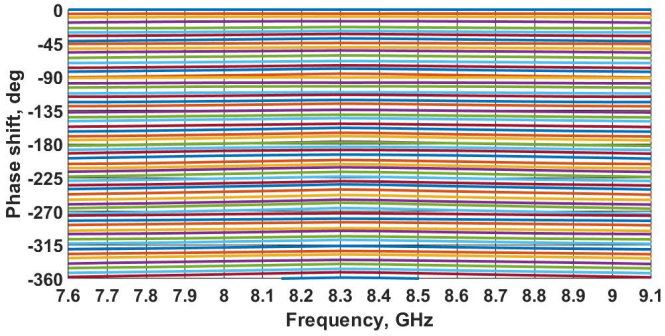
Fig. 16. Microscope picture of the 2 phase shifters (numbers indicate the phase shift in degree of the various PS cells).

TABLE VII
INDIVIDUAL PHASE ERRORS AVERAGED OVER THE ENTIRE OPERATING BANDWIDTH FOR THE TWO PS VERSIONS.

Version	180°	90°	45°	22.5°	11.2°	5.6°
A	−2°	1°	−1°	0°	−1°	0°
B	−2°	−2°	−3°	−3°	−1°	0°



(a) PS version A.



(b) PS version B.

Fig. 17. Measured CC phase shift. Attenuator state is 0 (no attenuation).

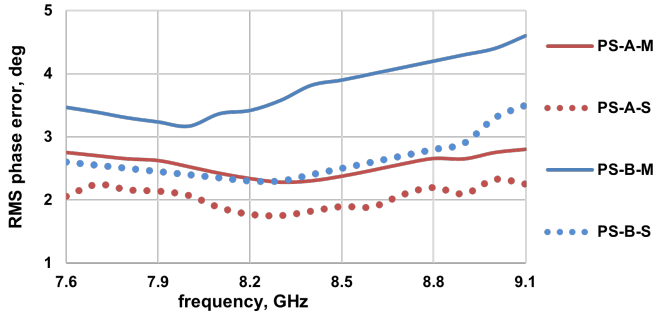


Fig. 18. Measured (-M, solid line) and simulated (-S, dotted line) PS RMS phase error.

behavior over frequency while version B shows an "inverted-U" shape phase shift. In both cases there is an excessive phase shift that can be noted by the lowest PS line, slightly above -360°. The effect is limited in version A and more evident on version B. Table VII reports the individual phase errors of each cell averaged over the entire operating bandwidth. Apparently, the cell topologies proposed in version A are more robust to electrical model and electromagnetic stack-up uncertainties than those proposed in version B, especially for the intermediate phase shifting cells, namely 90°, 45°, and 22.5°, where the topology of versions A and B is totally different. Considering the cells' topologies, the following hypothesis are inferred: in the HP/LP cells, the better results of version A are explained by the use of a single inductor in each path, while in the 22.5° cell version A uses a simpler all-pass network. Moreover, the ideal lumped element values of the HP/LP cell of version B are very small in the LP section and very large in the HP path. Consequently, the components are close to the technology's upper and lower feasibility limit and more sensitive to process variations. For the 11.2° and 5.6° cells there is little difference since the topologies are similar in the two versions and both of fairly simple structure. Finally, from Fig. 14 no difference is expected in the 180° cell, but minor deviations related to the synthesis of the Π topology for the LP network and the use of circular inductors in version A. Fig. 18 shows the measured and simulated RMS phase error at fixed attenuation versus frequency confirming the better behavior of version A over version B. There is some discrepancy between measurements and simulations mainly due to the limited accuracy of inductor EM simulations. The discrepancy is more evident in PS-B, for the reasons previously discussed.

Test structures of both PS versions have been characterized to evaluate the insertion loss. As shown in Fig. 19, version A exhibits better insertion loss mainly due to the simpler elementary topology for the 45° and 22.5° cells. In both cases, there is a slight difference between measured and simulated results, quantified in less than 0.1 dB/cell. The reason is an

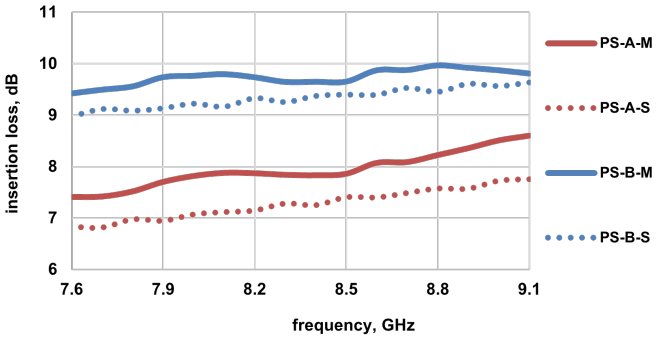
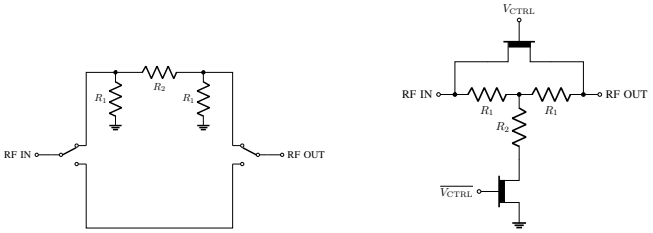
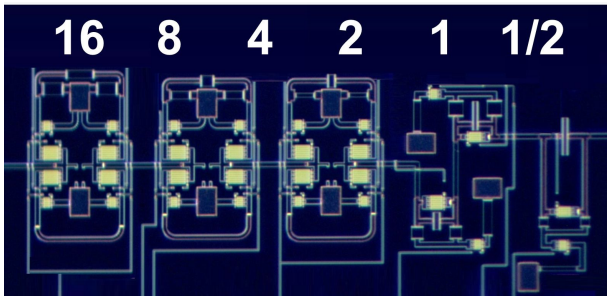


Fig. 19. Measured (-M, solid lines) and simulated (-S, dotted lines) insertion loss of PS test structures.



(a) Π topology. (b) Bridged-T topology.



(c) Microscope picture of the attenuator (numbers indicate the attenuation in dB of the various cells).

Fig. 20. Simplified schematics and layout of the attenuator.

under-estimation of the ON FET's parasitic resistance. The discrepancy between measurement and simulation is more evident on PS-A having smaller FET geometries on the series branch. Insertion loss could be further reduced by increasing the periphery of the FETs appearing in the series branch of the SPDTs, depicted in Fig. 13. However a careful trade-off between SPDT insertion loss and isolation should be performed before completing this task so that the leakage through the isolated branch is kept under control. Another way to reduce PS insertion loss is to increase the FET ON-state voltage therefore reducing the parasitic ON-state resistance of the FET. This technique would however have an impact on the S2P circuit design since it would be forced to produce a higher HI-level OUT value than the one indicated in Table II. The measured results for PS-A compare well with other reported experiments, as shown in the Table. IX.

B. Attenuator

As specified in Table IV, a 6-bit attenuator is adopted in the designed CC. In this case there are fewer design possibilities and the design risks with respect to the phase shifter are much more limited. Consequently, only one attenuator version is designed. For the higher value cells (16 dB, 8 dB, and 4 dB) a switching topology between a resistive attenuator (ATT) cell and a reference (REF) path is implemented. The resistive attenuator cell is realized with a Π topology since the series resistor values are larger than those of the equivalent T topology, and consequently less sensitive to process variations. Path selection is realized through a pair of SPDTs with series and shunt FETs. The lower value attenuation cells (2 dB, 1 dB, and 0.5 dB) are synthesized with a bridged-T topology that features smaller layout area, lower insertion loss and feasible resistor values for the considered attenuation level with respect to the switched attenuator solution [35]. Table VIII reports the FET geometries employed in each attenuator cell. The attenuator layout is shown in Fig. 20, size is 3.6 mm×1.6 mm.

Fig. 21 shows the measured attenuation versus attenuator state in the operating bandwidth. The attenuation level is practically ideal, as confirmed by state 64 that reaches, on average, 31.5 dB. The line has the expected constant 0.5 dB/step gradient. Finally, Fig. 22 shows, on the right axis, the measured

TABLE VIII
ATTENUATOR'S FET PERIPHERIES (NUMBER OF FINGERS MULTIPLIED BY UNIT GATE WIDTH EXPRESSED IN MICRONS).

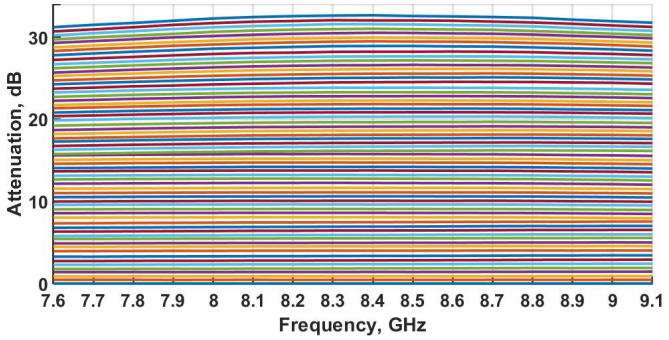
Config.	16 dB	8 dB	4 dB	2 dB	1 dB	0.5 dB
SERIES	8×50	8×50	8×50	6×40	4×40	4×40
SHUNT	4×20	4×20	4×20	4×20	4×20	4×20

and simulated RMS amplitude error at fixed phase shift versus frequency. The in band typical performance is 0.2 dB. The same Fig. 22 reports the attenuator test cell measured and simulated insertion loss on the left axis. Also in this case there is an under-estimation of the insertion loss for the reason discussed in the previous paragraph.

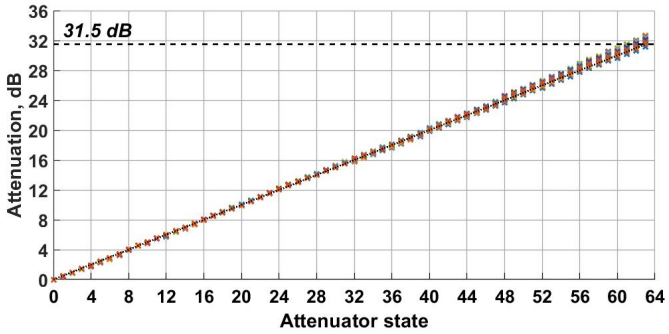
C. RF characterization

Fig. 23 depicts the measured constellation ($2^{12} = 4096$ points) at center frequency of the core-chip with PS version A. Note that angles in Fig. 23a are given in a positive (clockwise) notation while in Fig. 17 they are given as negative values (counter-clockwise). The parasitic phase shift of the attenuator is limited to ±6°. At lower attenuation levels (states 0 to 24) this value is less than ±3°. The constellation maintains the correct phase states thanks to the quasi-ideal behavior of the attenuator circuit. The phase states remain clearly separated especially at lower attenuation levels. At 0°, 45°, 180° and 225° there is a superposition of two consecutive phase states due to the phase shift of the 180° and 45° cells, slightly higher than expected. This effect, however, can be easily corrected in the design since it is a constant bias with respect to the ideal phase shift value.

Measured return loss (RL) is shown in Fig. 24 for the PAC containing PS-B. S_{11} is associated to the PS input port connected to SW1 while S_{22} to the ATT output port connected to SW4. SW1 and SW4 are indicated in Fig. 1. S_{22} is more



(a) Attenuation versus frequency.



(b) Attenuation versus attenuator state in the operating bandwidth (16 frequencies, 100 MHz spacing).

Fig. 21. Measured CC attenuation. PS state is 0 (0° shift).

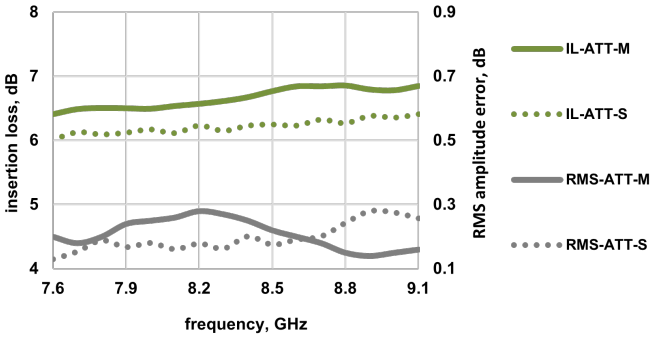
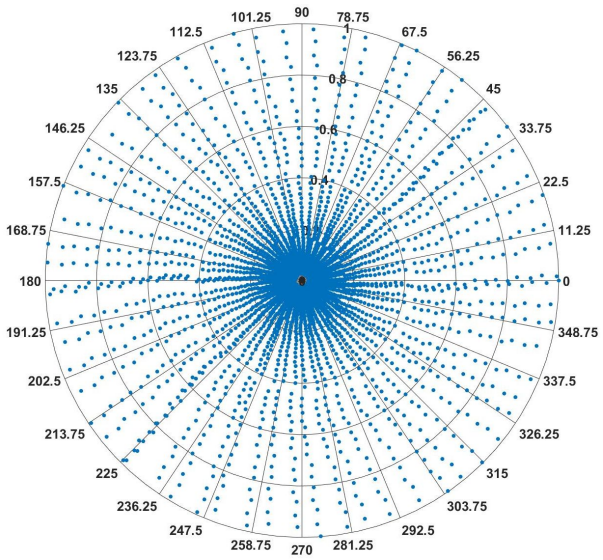
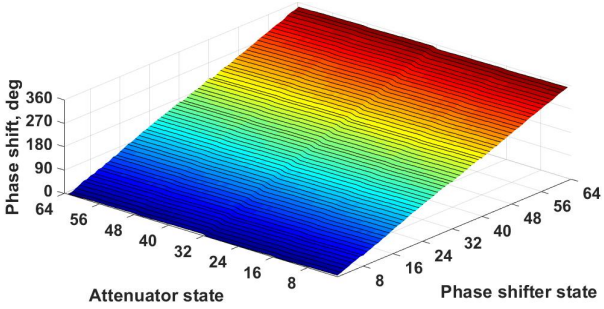


Fig. 22. Left axis: Insertion loss of ATT test structure and right axis: RMS amplitude error at fixed phase shift. Measured (-M, solid line) and simulated (-S, dotted line).



(a) Attenuation-phase shift polar plot normalized with respect to state 0 (no attenuation, no phase shift).



(b) Phase shift versus attenuator and PS state.

Fig. 23. Measured CC constellation at 8.4 GHz. PS version A.

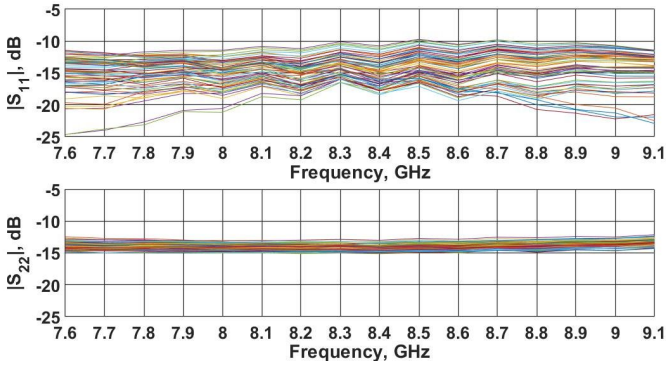


Fig. 24. Measured return loss. Top: PS input port, bottom: ATT output port.

constant in frequency due to the resistive nature of the attenuator as opposed to the PS showing a larger variation, typical of reactive cells. For both ports, RL is better than 10 dB, while the typical value is 13 dB on both ports. The version having PS-A is also tested for impedance matching. The RL is between 10 and 21 dB also for version containing PS-A. Characterization of the test structures confirm that the RL is better than 10 dB also at the intermediate ports, not accessible at PAC circuit level. Table IX compares the measured average RMS phase error at CC-level, i.e. including also the cross-talk effect, with previously published results. Both CC versions compare well with the literature, especially considering that better RMS values can be obtained by correcting the average (bias) errors of the cells reported in Table VII. Note that [27] specifies that the RMS phase error is calculated versus the 64 phase states only. Consequently, this figure of merit degrades if the effect of the 64 attenuation states is included in the analysis.

Finally, Fig. 25 shows the statistical analysis of the CC phase setting at 8.4 GHz. In particular, the results concerning the 90° PS cell of PS version B are reported, which are statistically significant as this cell has the most complex HP/LP topology, with many transistors, less favorable passive values and rectangular inductors. The analysis is carried out over the 130 properly working CC samples (nearly 79% yield). The

TABLE IX
COMPARISON OF THE RF PERFORMANCE WITH THE LITERATURE.

Ref.	Technology	Frequency range, GHz	Number of bits PS / ATT	RMS phase error, deg	RMS amplitude error, dB	Insertion Loss PS+ATT, dB	Return Loss, dB
[32]	0.5µm GaAs	$1.4-2.4$	6/0	4	0.4	4	>10
[36]	0.13µm CMOS	$7.9-9.6$	4/0	6	0.5	N/R	N/R
[37]	0.13µm CMOS	$8.5-10.5$	6/5	4.3	0.5	$12+N/R$	>11
[27]	0.5µm GaAs	$8.5-10.5$	6/6	2.5	1	$10+6$	>12
[38]	0.13µm SiGe	$9-11$	5/0	3.8	1.2	15	>15
[17]	0.25µm GaN	$8-12$	5/0	6.4	0.4	9	>10
[39]	65nm CMOS	$8-10.5$	6/6	4	1	$16+10$	>12
[28]	0.25µm GaAs	$11-13$	4/0	4	0.5	N/R	>10
[40]	0.25µm GaAs	$12-18$	4/5	5.1	0.7	$3+5$	>7
[41]	0.25µm GaN	$9-11$	6/6	4	0.8	$13+N/R$	>10
PS-A	0.25µm GaAs	$7.6-9.1$	6/6	$4^{\dagger}$	$0.6^{\diamond}$	$7.5+6.5$	>11
PS-B	0.25µm GaAs	$7.6-9.1$	6/6	$5.5^{\dagger}$	$0.6^{\diamond}$	$9.5+6.5$	>10

considering also † the attenuator's effect quantified in $1.5°$ RMS and $^{\diamond}$ the phase shifter's effect quantified in 0.4 dB RMS. N/R Not Reported

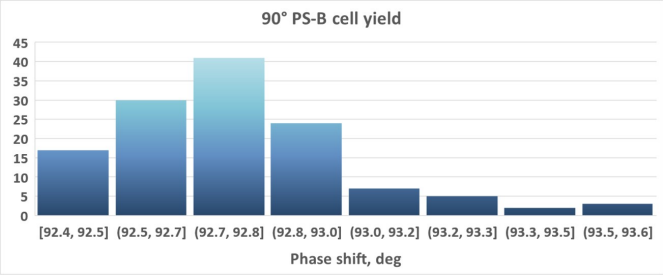


Fig. 25. Measured phase shift for the 90° cell of PS (HP/LP, version B) on 130 CC samples: mean value and standard deviation are 92.8° and 0.24°, respectively.

excluded samples have either a not working S2P or an out-of-specification gain or insertion loss, likely due to one of the amplifiers. Phase value span is as low as 1.2°, corresponding to a standard deviation from the mean value (92.8°) of 0.24°. These results prove the very good repeatability and robustness to process variation of the designed PS.

VI. CONCLUSION

A 18-bit core-chip operating at X-band (7.6 GHz-9.1 GHz) has been designed and implemented in commercial E/D-mode GaAs MMIC technology. The design and characterization of the core functional blocks, namely the 18-bit serial-to-parallel interface and the 12-bit phase and amplitude control circuit, have been presented and discussed. To mitigate design risks and perform a topology comparative evaluation, two different phase shifter versions have been developed using standard PDK models provided by the foundry, showing that certain circuit topologies are more robust to model uncertainties. The best PS architecture achieves 1.5° lower RMS phase error and 2 dB lower insertion loss than the other one, leading to an RMS phase setting error at CC-level as low as 4°, including also the parasitic phase shift of all attenuator states. More than 150 CC samples for each version have been manufactured and tested to assess yield and repeatability. The standard deviation of the phase setting is below 0.25° for all PS states of both versions. The S2P interface, designed resorting to an ad-hoc developed simplified transistor model, achieves an ultra-low consumption of 2.2 mW/bit and more than 86% yield. The overall CC performance well compares with the state of the art, and fixes a record power consumption for the digital part.

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