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Temperature Characterization of a Fully-synthesizable Rail-to-Rail Dynamic Voltage Comparator operating down to 0.15-V

(Invited paper)

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***Abstract*— This paper deals with the performance/ temperature tradeoff in an ultra-low voltage, ultra-low power rail-to-rail dynamic voltage comparator made solely by digital standard cells. The digital nature of the comparator makes its design technology portable also enabling its operation at very low supply voltages down to deep sub-threshold. In particular, as sub-threshold circuits have a significant temperature dependence, this paper focuses on the comparator performance under different supply voltages and temperatures.**

Measurements performed on a 180nm testchip show correct operation under rail-to-rail common-mode input at a supply voltage ranging from 0.6V down to 0.15V. Moreover, the measurements under temperature variations of offset, clock-to-output delay, and power in the range from -25 °C to 75 °C show the respective performance trade-offs.

Keywords—Temperature dependence, standard cell-based, technology portable, low design effort, low area Dynamic comparator, fully-synthesizable, ultra-low voltage, ultra-low power, sensor nodes, Internet of Things.

I. INTRODUCTION

Circuit techniques for operation over a wide range of supply voltages are crucial to meet the tight power and cost constraints of always-on miniaturized self-powered sensor nodes whose need to fit the power budget of millimeter-scale harvesters targeting the Internet of Thing (IoT) applications [1][2]. For this reason, circuit solutions based on digital standard cells have been explored to push the supply voltage down to deep sub-threshold, and reduce the human design effort for a low cost. Mostly and/or fully-digital/synthesizable building blocks such as OTAs [3][4][5] Filters [6], ADCs [7][8][9] DACs[10], and comparators [11][12] recently proposed in the literature are inherently more amenable for aggressive voltage scaling, automated design and design/technology porting than their analog counterparts. These design approaches deal with the challenge of keeping reliable performance [13] while enabling other interesting capabilities such as a graceful quality degradation at overscaled voltages [10].

In particular, this paper focuses on the performance evaluation under different supply voltage and temperature conditions of a Rail-to-Rail Dynamic Voltage Comparator (RRDVC) [11][12] that thanks to its digital nature, can operate with the widest operating supply voltage (at the best of the authors' knowledge) down to 0.15V with power consumption down to the sub-picoWatts level. This makes the circuit well suited for battery-less systems that are directly powered by harvesters, which are becoming very popular due to their low cost and small form factor [1][2]. However, the aggressive voltage scaling makes the circuit highly sensitive to temperature variation. In fact, the performance of ICs operating in sub-threshold is highly affected by the temperature variation. In consideration of that, the temperature dependence of key comparator performance like offset, clock-to-output delay, and power consumption are discussed for the first time herein based on measurement results on a recent 180nm demonstrator published in [12].

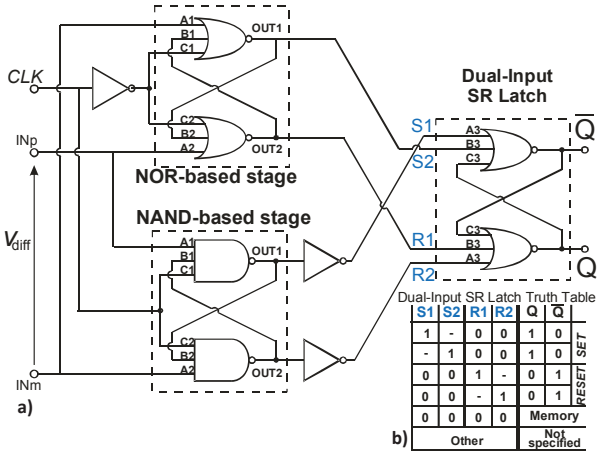

Fig. 1 Proposed fully-synthesizable RRDVC with complementary NAND/NOR input stage and dual-input SR latch: a) gate-level structure, b) truth table of the dual-input SR latch [12].

In Section II the operating principles of the RRDVC are briefly recalled. Then, in Section III the RRDVC measured performance from near-threshold (600mV) down to deep sub-threshold (150mV) of offset, clock-to-output delay, and power across the -25°C - 75°C temperature range are shown. In Section IV the conclusion will be drawn.

II. FULLY SYNTHESIZABLE RRDVC OPERATING PRINCIPLE

The RRDVC [12] considered in this paper is sketched in Fig. 1. Such a circuit combines the digital outputs of the 3-inputs NANDs-based dynamic voltage comparator (DVC) [8] (Fig. 2a) with its "complementary" 3-inputs NORs-based DVC version for rail-to-rail operation. The 3-inputs NAND gates (I4 and I5 in Fig. 1a) operate correctly and generate the expected outputs S1 and R1 when the common-mode input is closer to V_{DD} than to ground. In this case, the 3-inputs NOR gates (I2 and I3 in Fig. 1a) fail and their outputs are stuck at the pre-charged value (i.e., ground), and do not affect the DVC output. Vice versa, when the common-mode input is closer to the ground, the 3-inputs NOR gates properly operate. Both the 3-inputs NOR and the 3-inputs NAND gates operate

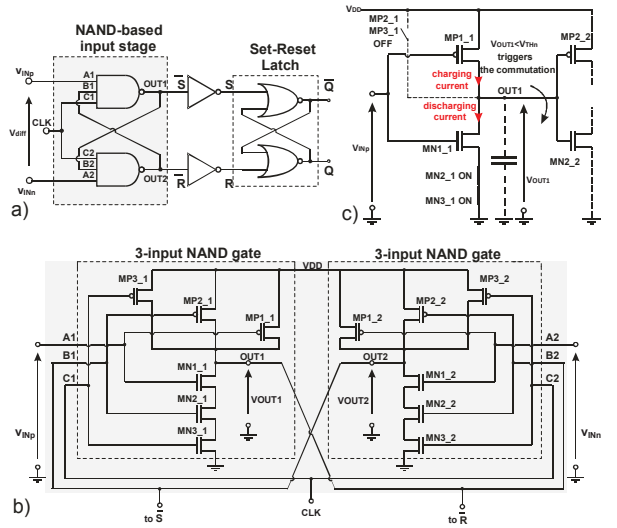

Fig.2. NAND3-based DVCs [8] (sub-block input stage of Fig.1a) a) gate-level and b) transistor-level view, c) equivalent circuit during output transition.

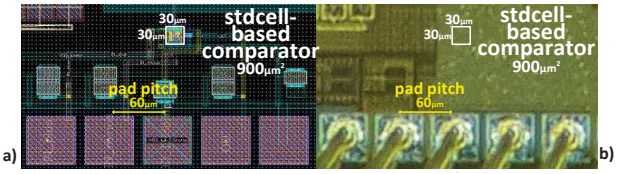

Fig.3. Proposed fully-synthesizable comparator with complementary NAND/NOR input stage and dual-input SR latch: a) layout, b) die photo

properly when the common-mode input is around the mid-range.

For sake of simplicity, the RRDVC operation is explained only referring to the NAND-based DVC sub-block referring to Fig. 2 originally proposed in [8]. The sampling clock is tied to the inputs C1 and C2 and thus connected to the gate terminals of MN3_1, MP3_1, and MN3_2, MP3_2. The inputs A1 and A2 of the NAND3 gates are at the gate terminals of transistors MN1_1, MP1_1, and MN1_2, MP1_2. These inputs represent respectively the non-inverting (v_{INp}) and inverting (v_{INm}) input of the DVC. The NAND3s terminals B1 and B2 are connected to the gate terminals of MN2_1, MP2_1, and MN2_2, MP2_2, and also respect to the outputs OUT2 and OUT1 of the NAND3 gates in a cross-coupled fashion. At the high-to-low clock transition, OUT1 and OUT2 are pre-charged to V_{DD}, and transistors MN2_1 and MN2_2 are on, due to the cross-coupled feedback connection. At the low-to-high clock transition, the transistors MP3_1 and MP3_2 are turned off, thus disabling the precharge of OUT1 and OUT2 and the sampling phase starts. The transistors MN3_1 and MN3_2 are turned on so that the pull-down networks of the two NAND gates are enabled: the transistors MN2_1 and MN2_2 are still on immediately after the rising clock edge since OUT1 and OUT2 are still at V_{DD}.

Assuming a positive input differential voltage $v_{DM} = v_{INp} - v_{INm}$, OUT1 is pulled down by MN1_1 faster than OUT2, since the gate voltage of MN1_2 is lower than the gate voltage of MN1_1. Therefore, OUT1 reaches V_{THn} before OUT2, where V_{THn} is the threshold voltage of NMOS transistors. The inherent positive feedback forces OUT1 to be latched low, and OUT2 to be latched high. Opposite considerations with a negative differential input v_{DM} can be

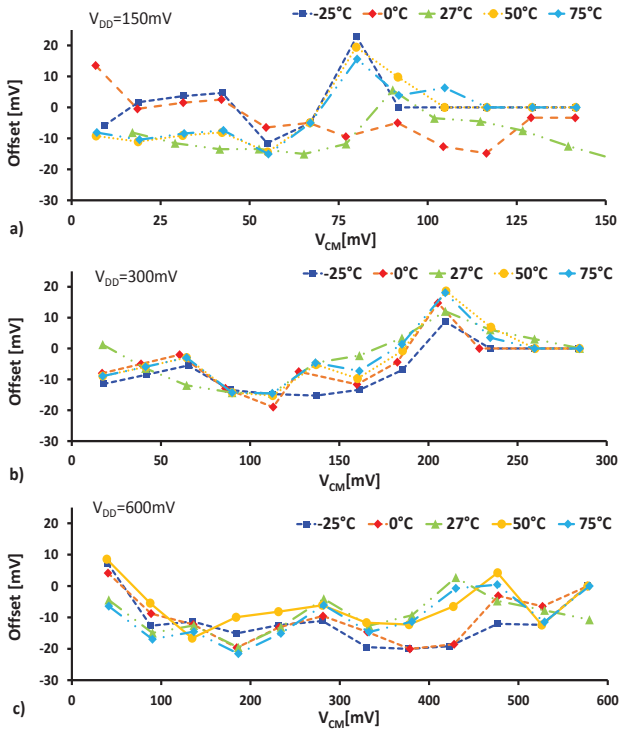

Fig.4. Measured input offset voltage vs. v_{CM} at different temperatures of the RRDVC at a) V_{DD}=0.15V, b) V_{DD}=0.3V, and c) V_{DD}=0.6V

done. This behavior constitutes the basic operation of an analog comparator although it is built by means of digital standard cells. Similarly works the NOR-based DVC for common-mode input is closer to ground.

III. Experimental Results Under Temperature Variations

The performance/temperature trade-off of the RRDVC in Fig. 1 across different supply voltage and the -25°C to -75°C temperature range is now explored referring to a demonstrator laid-out and fabricated in 180nm CMOS [12] reported in Fig. 3. Minimum-sized standard cells have been used to keep the power to a minimum, sacrificing speed and offset for the specific instance of the RRDVC. Of course, the usual wide range of area/ power/speed trade-offs can be achieved with proper cell strength. In fact, the strength of the input logic gates also affects the comparator offset, based on Pelgrom's law offset dependence on the reciprocal of the square root of the cell strength [14]. In other words, input offset reductions come at the cost of higher area and thus power [14]. Same for the propagation delay.

Fig. 4 shows the offset voltage versus the input common-mode range for supply voltages of 0.15V, 0.3V, and 0.6V and across the -25°C - 75°C temperature range for the minimum size RRDVC fabricated in 180nm. The offset has a more significant dependence on the common-mode input at the very low supply voltage of 0.15V. The worst-case offset of the proposed DVC in the rail-to-rail input range is 22mV at the supply voltages of 0.15V, 10mV at 0.3V, and 13mV at 0.6V. Although the offset increases lowering the supply voltage. From the measurement results, the temperature slightly affect the offset whenever it worsen his value.

The joint impact of temperature and differential input mode v_{DM} (common-mode input v_{CM}) on the clock-to-output

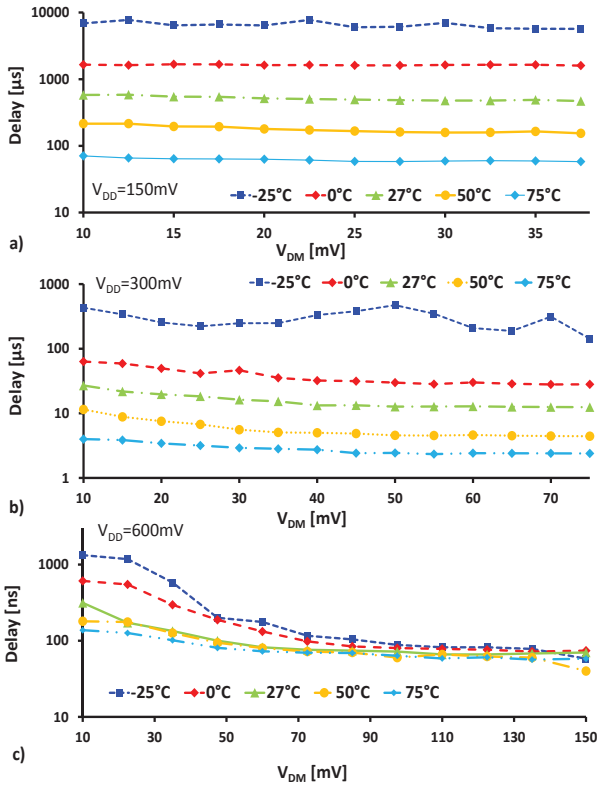

Fig. 5. Clock-to-output propagation delay of the RRDVC versus differential input voltage v_{DM} measured for v_{CM}=V_{DD}/2 and at different temperatures for a) V_{DD}=0.15V, b) V_{DD}=0.3V, and c) V_{DD}=0.6V.

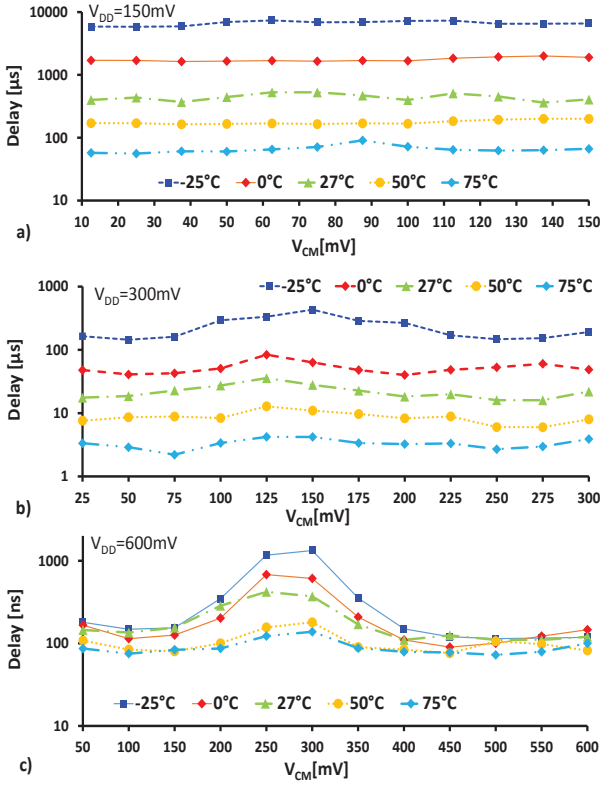

Fig. 6. Clock-to-output propagation delay of the RRDVC vs. common-mode input voltage v_{CM} measured for a differential input voltage v_{DM}=10mV and at different temperatures for a) V_{DD}=0.15V, b) V_{DD}=0.3V, and c) V_{DD}=0.6V

the lower is the delay whereas the power consumption is higher, whereas the temperature dependence delay is shown in Fig. 5 (Fig. 6). As expected, in the deep subthreshold (0.15V-0.3V V_{DD}), the higher the temperature,
is almost negligible in near-threshold (600mV V_{DD}). In particular, the impact of the differential input voltage v_{DM} on the propagation delay is plotted in Fig. 5 versus the differential input v_{DM} under v_{CM}=V_{DD}/2.

Because of the larger sensitivity of the current to the gate-source voltage in the sub-threshold and the deep sub-threshold region, the sensitivity of the propagation delay to the input differential voltage expectedly increases at lower supply voltages. The maximum slope at room temperature of the voltage-delay curve for is 25µs/V at V_{DD}=0.6V, 1.5ms/V at V_{DD}=0.3V, and reaches the highest value of 21.6ms/V at V_{DD}=0.15V and the temperature slightly affects the slope versus the differential input voltage v_{DM}

In Fig. 6, the clock-to-output propagation delay of the RRDVC was measured across the entire rail-to-rail input common-mode range for a differential input voltage v_{DM} of 10 mV. The propagation delay is expectedly maximum at v_{CM}=V_{DD}/2, due to the cross-conduction current at inputs with intermediate common-mode range. This phenomenon is more evident in near-threshold condition (at 0.6V in Fig. 6c).

The above-mentioned measurement results refer to an RRDVC with a minimum input gates' strength. Thus, the offset and the delay at room temperature could be reduce increasing the above-mentioned strength whereas the specific application will require increasing performance. Anyhow, the design choice targets an RRDVC suitable for direct powering from mm-scale harvesters under any supply voltage and temperature condition. The latter strongly affects the power consumption more and more from near-threshold (0.6V) towards a more aggressive voltage scaling in subthreshold (0.3V) and deep subthreshold (0.15V) regions.

At room temperature, the maximum power consumption is respectively 6.2pW (27pW), 24pW (89pW) and 1.95nW (2.22nW) for a supply voltage equal to 0.15V, 0.3V and 0.6V, at 10Hz (10kHz) clock frequency.

The power consumption across temperatures from -25°C to 75°C at a 10-Hz (10-kHz) clock frequency ranges from 0.3pW (0.5pW) to 0.1nW (0.1 nW) for a supply voltage of V_{DD} =0.15V from 2pW (37pW) to 0.3nW (0.36nW) for V_{DD}=0.3V and from 0.15nW (0.4nW) to 6.47nW (7.25nW) for V_{DD}=0.6V as shown by the measured plots in Fig. 7 (Fig. 8).

Comparing the power consumption in deep subthreshold at 0.15V at different clock frequencies (Fig. 7a and Fig. 8a), the temperature in the range -25°C to 75°C produces a power consumption variation of three orders of magnitude that is slightly affected by the switching activity of the clock. Thus, the leakage power consumption is the dominant one.

A more varying power consumption across the above-mentioned temperature range is progressively more evident in subthreshold (at 0.3V in Fig. 7b and Fig. 8b) and in near-threshold (at 0.6V in Fig. 7c and Fig. 8c). In other words, increasing the supply voltage the overall power consumption is dominated by the dynamic power consumption due both to the switching clock and the cross-conduction. The latter one depends both on the supply voltage V_{DD} and the input common-mode v_{CM} and it is more evident in the middle of the input dynamic range of the RRDVC (for $v_{CM} \simeq V_{DD}/2$).

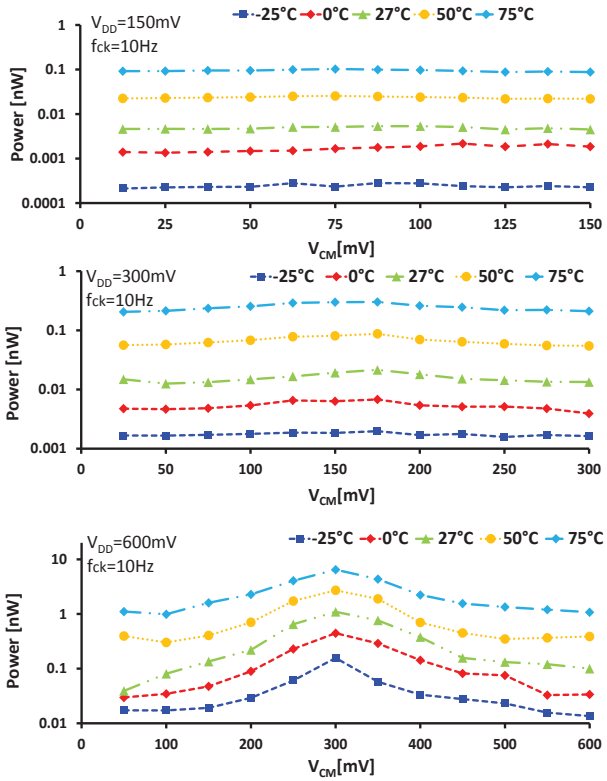

Fig.7. Power of RRDVC vs. v_{CM} measured for a clock frequency f_{CK}=10Hz at different temperatures for a) V_{DD}=0.15V, b) V_{DD}=0.3V and c) V_{DD}=0.6V.

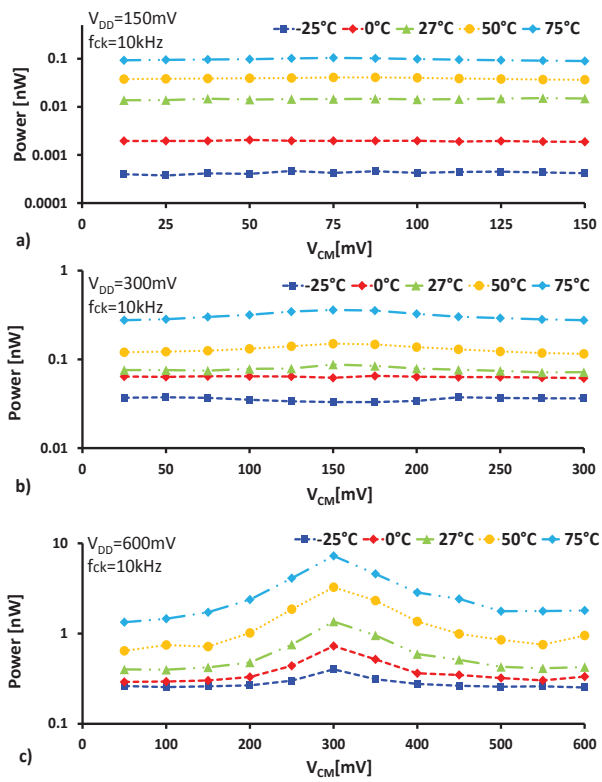

Fig.8. Power of RRDVC vs. v_{CM} measured for a clock frequency f_{CK}=10kHz at different temperatures for a) V_{DD}=0.15V, b) V_{DD}=0.3V, and c) V_{DD}=0.6V.

IV. Conclusion

The performance variation under temperature variation of an RRDVC designed and laid-out exploiting digital (automated) design tools enabling operation down to 0.15V was explored in this paper. Measurements have shown how the RRDVC performance is affected by the temperature variations in the range from -25°C to 75°C reaching up to three order of magnitude in difference. In particular, the power consumption ranges from sub-picoWatt to sub-nanoWatts at V_{DD} = 0.15 V, and from sub-nanoWatts to nanoWatts for V_{DD}=0.6 V. On this basis, the standard cell-based RRDVC is suitable to operate under unregulated supply and powered by mm-scale harvesters under any temperature condition in low-cost and ultra-compact IoT sensor nodes.

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