A Radiation-Hardened CMOS Full-Adder Based on Layout Selective Transistor Duplication

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***Abstract*— Single Event Transients have become increasingly problematic for modern CMOS circuits due to the continuous scaling of feature sizes, and higher operating frequencies. Especially when involving safety-critical or radiation-exposed applications, the circuits must be designed using hardening techniques. In this brief, we present a new radiation-hardened-by-design full-adder cell on 45 nm technology. The proposed design is hardened against transient errors by selective duplication of sensitive transistors based on a comprehensive radiation-sensitivity analysis. Experimental results show 62% reduction in the single event transient sensitivity of the proposed design with respect to the unhardened one. Moreover, the proposed hardening technique leads to improvement in performance and power overhead and zero area overhead with respect to the state-of-the-art techniques applied to the unhardened full-adder cell.**

***Index Terms*—Arithmetic circuit, fault tolerance, full-adder, radiation hardening, redundancy, single event transient.**

I. Introduction

As the technology scaled, the closeness of transistors along with the reduction of the currents and nodal capacitances led to an increase of circuits vulnerability to soft errors [1]. When an ionizing particle hits the silicon of an electronic circuit, it releases its energy causing a transient voltage pulse in the logic gates, known as Single Event Transient (SET), which can propagate through the combinational logic and be latched by memory elements, creating an error. Due to the drastic increase of SET sensitivity due to the reduction of transistor sizes in modern devices, the use of Radiation Hardening by Design (RHBD) techniques for providing robust systems against transient errors has taken on growing importance [2].

Arithmetic operations are the key operations of several ubiquitous VLSI circuits, such as Digital Signal Processors (DSPs), and microprocessors [3]. Full-adder is one of the basic blocks for implementing electronic circuits for computations, such as Arithmetic Logic Units (ALUs) and Floating-Point Units (FPUs). Therefore, enhancing a robust full-adder cell is mandatory for developing radiation-hardened system.

In this paper, we present a RHBD full-adder cell relying on selective duplication of transistors based on radiation analysis. As the main novelty, this work leverages a comprehensive radiation analysis, both in the static and transient operation state to detect the vulnerable transistors to be enhanced. In opposite to the state of the art, the analysis considers the physical description of the cell, geometry, material, and layout of the cells. The comprehensive analysis enables to limit duplication to the most vulnerable transistors of the original cell, obtaining radiation-hardness with negligible performance overhead. The rad-hard Full-Adder has been implemented with the FreePDK 45nm library providing reference circuit modeling and physical implementation in a 45nm technology and fabricable Scalable CMOS (SCMOS) [4]. We have gone further than the state of the art by performing the physical implementation of the radiation-hardened full-adder cell. Since for implementing the duplication of the vulnerable transistors, the vacant volume of the original cell is used, the area of the cell remains the same as the original one, while the sensitivity versus radiation-induced SET is reduced by 62%.

The rest of the paper is organized as follows. Section II reviews some of the contemporary radiation hardened by design techniques. In Section III, the development of the radiation-hardened full-adder cell and the physical design of the circuit are elaborated. Finally, the brief is concluded in Section IV.

II. Related Works

Radiation hardening by design is one of the major techniques for increasing the resiliency of combinational logic against soft errors. Layout-level techniques to improve the radiation-hardness capability, such as annular layout guard rings, have been applied to many CMOS circuits [5]. However, this approach introduces a wide area overhead. To overcome this issue, transistor-level techniques such as transistor resizing, and redundancy techniques have grown in importance. The design of more reliable systems by applying redundancy is one of the most common approaches [6][7]. Though, the duplication of the whole design is costly in terms of area and performance overhead. Therefore, researchers move towards using selective redundancy to protect only the part of the circuit with the highest soft error vulnerability [8]. In [14], the authors choose the gates to duplicate accordingly with the probability that a SET generated in the gate can propagate to the output. Differently, the duplication of the transistors of the gates in the last stage of the circuit is proposed in [7], assuming the last stage as the most vulnerable without taking into account the radiation profile, technology parameters, and physical layout features. Focusing on solutions based on redundancy at the transistor level, in [10], the authors proposed an asymmetric transistor sizing technique for the most sensitive nodes of the circuit but it is limited to the assumption that a particle strikes only the transistors connected to the output of the gate. In [11], the authors proposed a selective transistor redundancy technique, choosing the vulnerable transistor by calculating the probability of failure of the circuit for each transistor and protecting the transistors with the higher failure probability.

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However, the impact of the physical characteristics, electrical behavior of the circuit, and the radiation profile in the failure probability are not considered.

In this work, by combining layout-level and transistor-level hardening techniques, we propose a radiation-hardened full adder cell taking into account the radiation profile of the mission as well as the physical layout implementation and the electrical characteristics of the cell in the transient state, aiming to minimize the area, performance and power overhead.

III. Development of the Radiation Hardened Full-Adder Cell

This work is proposing a 45 nm full-adder, hardened against radiation-induced transient errors. At first, we implemented an unhardened full-adder cell, using 30 transistors composing of 5 logic gates (two *XOR*s, two *AND*s and one *OR*). The layout of the unhardened full-adder is developed using the 45 nm FreePDK physical library. We performed a comprehensive radiation analysis to characterize the expected SET pulse associated with each logic gate. Differently from the state of the art, the radiation characterization is performed taking into account both the physical structure of the original cell and the profile of the particles interacting with the cell layout. An electrical simulation setup has been developed and instrumented to analyze the effect of SET, considering not only the static state but also the transient operating state of the full-adder. Using this setup, the transistors that contribute the most to the failure rate are identified and classified as vulnerable transistors and then duplicated. In the proposed radiation-hardened cell, the vacuum volume of the original layout is exploited for duplicating the vulnerable transistors.

A. SET Characterization for the Unhardened Full-Adder Cell

In order to identify the vulnerable transistors of the original full-adder, we developed the electrical model and the layout implementation of the original full-adder on the base of the 45 nm physical library. Using the *Klayout* tool, we developed the Graphic Data System-II (GDS-II) description of the cell. Please note that in the implemented cell layout, not all the 30 transistors composing the full-adder have the same geometric dimensions. Therefore, the logic gates composing the full-adder cell have different dimensions exposed to the radiation particle, leading to different radiation sensitivity.

To perform the comprehensive radiation analysis, we developed a radiation analysis tool for simulating the passage of the radiation particles through the silicon structure of the cell. The analysis tool takes into account the layout description in terms of GDS format, the material and structure of each layer as well as the energy and type of the particle hitting the cell, and simulates the particle passing through several layers of the cell. During the passage, it calculates the released energy in each node of the cell with respect to the gate cell geometry and material. By converting the transmitted energy to voltage and calculating the amplitude and width of the voltage pulse, the developed analysis tool estimates the static error rate, i.e. the static cross-section of each logic gate of the full-adder cell. Please note that the efficiency and accuracy of the proposed radiation analysis tool are verified by the radiation test performed at the CERN radiation facility [12]. Fig. 1(a) represents the simulation of the passage of a heavy-ion crossing the full-adder cell, releasing its energy during the propagation inside the sensitive area of the cell producing disturbance voltage sources in the cell, Fig. 1(b).

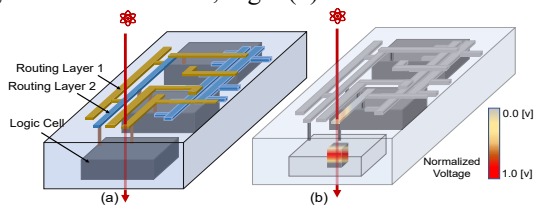

Fig. 1. (a) A Heavy-ion track releasing its energy while crossing the cell and (b) creating voltage disturbance.

The characterization of the SET affecting the unhardened full-adder cell is based on a Heavy Ion profile related to the UCL facility. The simulation involves 10,000 particles of Xe, Ni, AI, and C ions with an energy range between 995 MeV and 131 MeV and a Linear Energy Transfer (LET) between 62.5 MeV/mg/cm^2 and 1.3 MeV/mg/cm^2. Fig. 2 represents the SET static cross-section of the full-adder cell. As it can be observed, the ions with lower energy (C) lead to the same cross-section for the three gates composing the full-adder cell. Moving toward particles with higher energy (e.g, Xenon ion), it can be observed that AND and OR cells have a radiation sensitivity of 21.1% higher than the XOR cell.

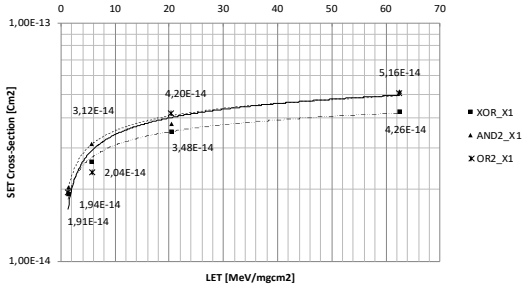

Fig. 2. SET Cross-section per logic gate of the original Full-Adder circuit for different LET values.

B. SET Propagation in Transient Operation of the Full-Adder Cell

In the previous stage, we generated a collection of SET pulses arising from the physical simulation of the interaction between the cell and 10,000 heavy ions. The SET pulses are characterized by width and amplitude, and associated with the logic gate they affect. To evaluate the contribution of each transistor to the unreliability of the cell, we developed an electrical simulation environment integrated with HSPICE. This environment is instrumented with the SETs collection. It is able to automatically modify the original netlist of the full-adder cell by inserting a transient voltage source in a specific transistor node, emulating the SET in that node, to perform the electrical simulations. During the electrical simulation, each SET pulse is inserted in the associated transistor. Thus, the disturbance generated in each transistor is different and it is corresponding to the SET calculated in the logic gate, defined by radiation analysis. Fig. 3 illustrates the emulation of a transient pulse affecting a transistor (T_{15}) of the full-adder cell caused by a particle hitting the source terminal.

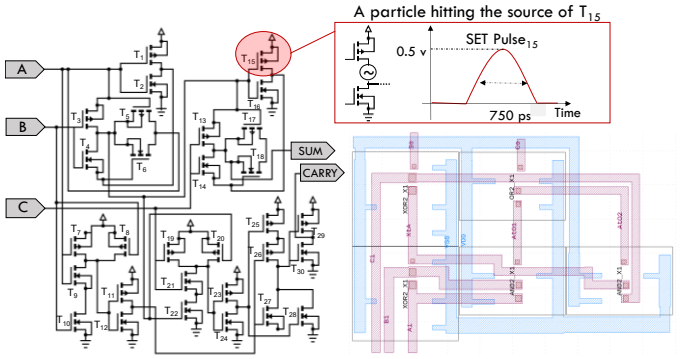

Fig 3. (a) Emulating an SET pulse identified by radiation analysis in the affected transistor node of the Unhardened full-adder (b) Layout of the Unhardened Full-adder

The electrical netlist of the full-adder is modified and the SET pulse is inserted to the source terminal of the transistor in terms of a transient voltage pulse associated with the logic gate. The effect of each SET pulse generated by the radiation analysis tool has been evaluated singularly through the electrical simulation. The full-adder has been simulated with all the input patterns and the SET has been inserted in the affected node at random time during the simulation. An emulated SET pulse may propagate to neither, or either of the outputs of the cell. If the pulse propagated to a storage element is sufficient to fulfill the requirement of the technology, it will be captured by the storage element. For the 45 nm technology, we identified that a SET pulse with an amplitude greater than 465 mV can be latched, while we observed that minimal pulse width may vary from 200 ps up to 320 ps depending on the affected cell and the pulse amplitude.

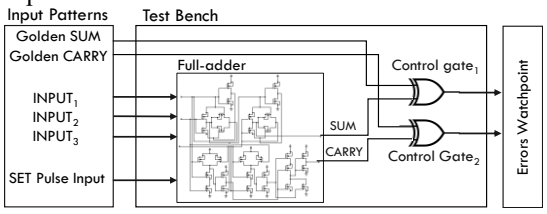

Fig. 4. The developed setup to evaluate whether the generated SET pulse inside the full-adder is creating an error.

To verify whether the propagated SET in the output of the full-adder is sufficient to be propagated to the output of the circuit and eventually create an error, we designed a setup represented in Fig. 4. The inputs of the full-adder, the SET pulse to be inserted, and the outputs of the golden full-adder (without emulated SET) are given to the test bench. The *Control Gates* monitor the mismatch between the outputs of the golden full-adder and the one affected by the SET pulse. A transition at the outputs of the control gates is caught by error watchpoint and represents the propagation of a SET pulse to the output of the full-adder cell. This SET is labeled as error-inducing SET. The transistors are ranked accordingly with the number of error-inducing SET pulses generated in their terminals. The transistors causing the higher number of errors are labeled as vulnerable transistors and selected as a critical source of failure for the whole cell. Fig. 5 represents the ratio of error-inducing SETs to the emulated SETs for each transistor, defined as Dynamic Failure Rate of each transistor in the original full-adder cell. Five of these transistors have a noticeable higher dynamic failure rate with respect to the others. In particular, they are related to the 62% of the total error-inducing SET. This is due to two main reasons: firstly, due to the specific physical structure of these transistor nodes in the layout, the hitting particles transmit enough energy to generate SET pulses with a high amplitude and long duration. Secondly, the electrical behavior of the cell allows the generated pulse to reach the output and to be latched by the measurement FFs.

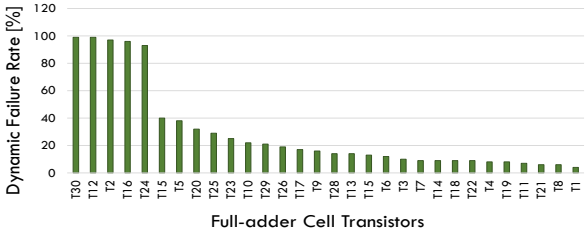

Fig. 5. Dynamic Failure Rate of each transistor of the Original Full-adder cell.

C. *Hardening of Full-Adder Cell by Duplication*

The transistors previously detected as more vulnerable (T_2, T_{12}, T_{16}, and T_{24} and T_{30}) have been selected to be hardened through duplication. The duplication of these transistors introduces the charge-sharing effect leading to a reduction of the pulse width and amplitude, accordingly with [14].

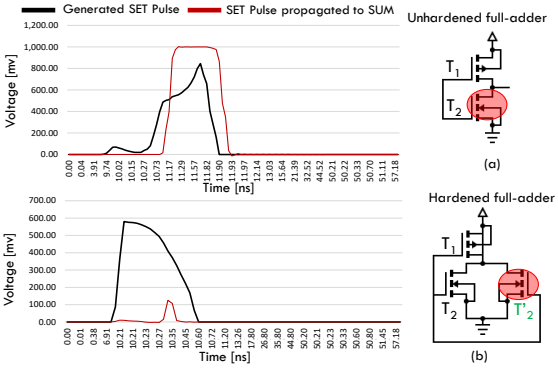

Fig. 6. The transistor in-cell duplication of the vulnerable transistors T_2

When a radiation particle hits a transistor node, it releases its energy and deposits charge. If the deposited charge is greater than the minimum charge required to create a disturbance in the circuit, defined as a critical charge, a SET is generated. The duration (i.e. width) of this disturbance is dependent on the amount of collected charge at the affected node. If the charge deposited by the particle is collected by two or more sources simultaneously, a smaller charge is collected by each node due to the charge sharing effect. Therefore, it leads to SET pulses with a smaller width and amplitude, which has a lower probability to be sampled. In our case, if the placement of the vulnerable transistors is performed to promote charge sharing between two electrically connected nodes, it leads to the mechanism known as "pulse quenching" [14][13] which is partially contributing to the mitigation of the SET pulses. Therefore, by duplicating vulnerable transistors, the charge sharing effect mitigates the SET pulse generated in the node reducing the duration and amplitude of the pulse and decreasing the probability that the generated pulse could fulfill the technology requirements to be propagated and sampled.

Fig. 6 shows the duplication of the transistors T2, previously identified as vulnerable transistor. Fig. 6.a represents the

generated SET pulse at source node of transistor T_2 with the duration of 650 ps and amplitude of 845 mv happening as an effect of the particle hitting and releasing its energy in the node of Transistor T_2. By emulating the SET pulse in the source of T_2 in the electrical simulation environment, we observed the propagated SET pulse at the *SUM* output of the unhardened full-adder with the duration of 1.2 ns and amplitude of 995 mv. We have performed the radiation analysis on the hardened full-adder cell evaluating the hardened layout implementation and, as expected, we observed a drastic change in the generated SET pulse. Fig. 6.b represents the generated source SET pulse at the same transistor node, hardened by duplication with the duration of 265 ps ns and amplitude of 580 mv, while it has been propagated to the *SUM* output of hardened full-adder as a negligible pulse which is not sufficient to be captured by the storage element and generate an error in the system.

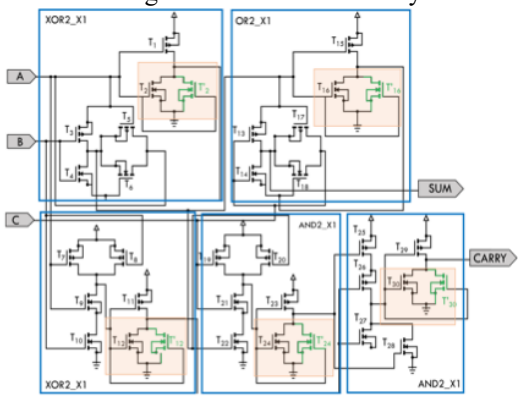

Fig. 7. The Radiation-hardened full-adder scheme with duplicated transistors highlighted.

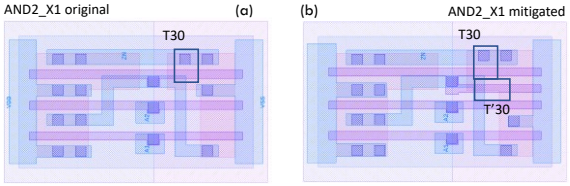

Fig. 8. An example of the duplicated transistor insertion on the AND2_X1 original (a) and mitigated (b).

TABLE I
SELECTIVE TRANSISTOR DUPLICATION SIZE

Logic Cell	Selective		Duplicated		Layer Overhead	
	W [µm]	L [µm]	W [µm]	L [µm]	PolySi [%]	Active [%]
AND	0.415	0.050	0.313	0.048	1.5	5.1
XOR	0.415	0.050	0.415	0.048	1.6	5.2
OR	0.415	0.050	0.312	0.049	1.5	5.0

To implement the selective hardening, we modified the layout of each cell by adding a duplicated transistor placed beside the radiation-sensitive ones. Inserting the duplicated transistor requires specific modifications of each gate by acting mainly on the polysilicon and the contact layers. Since the modification of the layout has been performed without increasing the area of each gate, the insertion of the duplicated transistors required to suitably shape their dimensions. Table I reports the size of original and duplicated transistors. The size of the duplicated transistors is chosen based on the available volume of the cell to avoid the introduction of area overhead in the hardened design.

Finally, we performed the place and route of the five cells interconnecting them using the *via1* and *metal2* layers. The routing of the connection points has been performed avoiding to overlap the radiation-hardened regions. Fig. 7. represents the hardened full-adder cell with duplicated transistors highlighted. Please consider that hardened full-adder does not have specific modification on metal2 and via1 layers. Fig. 8 shows an example of layout-oriented transistor duplication. We increased the active region inserting a poly silicon strip where the T'_{30} is added. In order to guarantee the minimal pitch of the Design Rule Check (DRC) on the poly-silicon we moved the vias on the T_{30}. Furthermore, the V_{SS} connections were also moved on a different point in order to minimize the parasitic capacitance generated by the inserted transistor structure. We reported in Table I the physical comparison between the unhardened and hardened layout implementation of the full-adder cell. Please note that, even if implemented with the FreePDK45 physical library, the proposed radiation-hardening methodology is applicable to other physical design kits.

IV. EXPERIMENTAL RESULTS

We compared different radiation analysis performed on the full-adder design when different radiation-hardening approaches have been adopted. We analyzed three designs using the defect tolerant technique [14], the full transistor resizing approach [15] and the annular layout transistors and guard ring [16]. The designs were implemented at the GDS layout level and analyzed with the radiation analysis simulation tool [12], adopting the Xe heavy-ion particle. The outcome of the radiation tool has been used to perform an analysis of SET during operation of full-adder using instrumented electrical simulation environment applied to the exported netlist generated from the GDS layout, with the same methodology described in subsection III.C. Table II reports the results of this comparison. To elaborate more, it shows the comparison of the static cross-section and the transient failure rate. The cross-section reports the structural sensitivity of the circuit versus the Xe radiation particles, while the error rate provides the percentage of errors introduced by the injected particles on the overall full-adder area, considering that each version has been analyzed by means of 34,620 injections with a pulse profile produced by the radiation particle simulator.

As it is noticeable, the proposed selective layout is a suitable solution since it is reducing the error rate for more than 62% with respect to the unhardened version. Besides, we observed that with lower LET values, the error rate is reaching 93% for the Al heavy ions and it is totally nullified for the C heavy ion. Considering the transient cross-section sensitivity, the full-resizing and annular versions are around one order of magnitude less sensitive than the others due to the larger contact layer and charge sharing distribution on the polysilicon layer which reduce the generation of critical transient pulses. On the contrary, the proposed version has a cross-section slightly greater than the unhardened circuit but it drastically reduces the error rate thanks to the enhanced topology of the duplicated transistors properly inserted within the layout. Moreover, even

TABLE II COMPREHENSIVE COMPARISON BETWEEN ORIGINAL AND RADIATION-HARDENED FULL-ADDER

Full-adder versions	Radiation Analysis Comparison		Energy Characterization on Sensitive Volumes		Delay and Data Comparison		
	Transient Cross-Section [cm^2]	Error Rate [%]	Distributed Energy on Gate Layer [%]	Maximal Peak [KeV]	Delay [ps]	Power Overhead [%]	Area Overhead [%]
Unhardened	2.12E-14	26.60	67.00	4,462.89	440	-	-
Full Resizing (x2) [14]	1.56E-15	10.10	42.32	2,634.16	896	43%	100.13
Defect Tolerance [15]	3.80E-14	15.86	56.64	4,314.44	560	13%	18.42
Annular and Guard Ring [16]	1.42E-15	10.05	39.13	2,510.38	850	38%	54.04
Proposed Selective Layout	2.56E-14	10.07	52.60	2,555.20	456	2%	0

though the proposed solutions obtained nearly the same error rate as the methods proposed in [14][16], it significantly improves the power and performance overheads while the achieved area overhead is zero. These results are elaborated on in Table II. To further investigate the effectiveness of our proposed hardening method, we analyzed the distribution of the energy within the silicon volumes of the full-adder versions, and we measured two parameters: the maximal peak of energy released at the sensitive volume and the percentage of energy distributed on the gate layer of the full adder. The first parameter is fundamental to evaluate the voltage amplitude of the pulse, while the second is related to the percentage distribution of the released particle energy on the sensitive layer of the full-adder. The experimental analysis on the sensitive layers indicates the transistor gate layer as the most critical one.

The data reported in Table II demonstrates that our solution reduces the maximal peak similarly to the annular and guard ring hardening method, while the distributed energy is partially reduced with respect to the unhardened version. This generates a greater distribution of voltage pulses characterized by a reduced voltage amplitude. Please notice that we have performed the radiation analysis on the hardened version of the full-adder considering the new developed layout including the duplicated transistors. Therefore, by duplicating the vulnerable transistors, the sensitive area of the cell increases while the level of sensitivity of this larger area in the hardened version decreases.

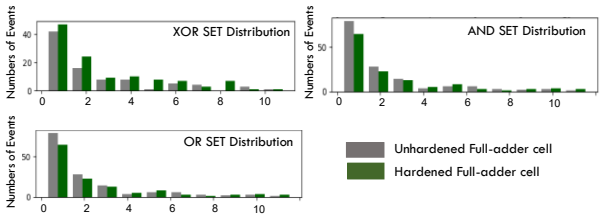

Fig. 9. Comparison of SET pulse amplitude distribution of the original and the radiation-hardened version considering a 3D simulation of 10,000 Xe Particles.

We investigated the different cross-section sensitivity results by analyzing the SET effects generated by the radiation analysis. The sensible nodes are identified on the layer contacts. Fig. 8 represents the comparison of the SET distribution in the full-adder design for the unhardened and the proposed rad-hard solution. As it is expected, by duplicating the vulnerable transistors of the cell, the area exposed to the radiation particles slightly increases. However, since duplicating the transistors, increase the charge sharing capability of the sensitive transistor nodes, the released energy leads to the SET pulses with lower amplitude. The performance of the proposed cell has a 3% reduction with respect to the original one while the power consumption varies from 3.018 µW to 3.078 µW, increasing by 2.02%. Please note that due to our adopted layout technique, we did not introduce any area overhead in the radiation-hardened cell compared to the original one since we added the duplicated transistor within the same cell layout space.

V. CONCLUSIONS

In this brief, a new radiation-hardened 45 nm full-adder cell is proposed. The design has been achieved by adopting a selective transistor duplication at the layout level applied to the radiation sensitive. This structure is reducing the impact of high-energy radiation particles without introducing area overhead and with negligible delay degradation which makes the design efficient for critical applications such as aerospace electronic circuits or high energy physics monitoring systems.

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