Digital Design Techniques for Dependable High Performance Computing

Digital Design Techniques for Dependable High Performance Computing

Sarah Azimi, Luca Sterpone
Politecnico di Torino
Torino, Italy
{sarah.azimi, luca.sterpone}@polito.it

***Abstract*—As today's process technologies continuously scale down, circuits become increasingly more vulnerable to radiation-induced soft errors in nanoscale VLSI technologies. The reduction of node capacitance and supply voltages coupled with increasingly denser chips are raising soft error rates and making them an important design issue. This research work is focused on the development of design techniques for high-reliability modern VLSI technologies, focusing mainly on Radiation-induced Single Event Transient. In this work, we evaluate the complete life-cycle of the SET pulse from the generation to the mitigation. A new simulation tool, Rad-Ray, has been developed to simulate and model the passage of heavy ion into the silicon matter of modern Integrated Circuit and predict the transient voltage pulse taking into account the physical description of the design. An analysis and mitigation tool has been developed to evaluate the propagation of the predicted SET pulses within the circuit and apply a selective mitigation technique to the sensitive nodes of the circuit. The analysis and mitigation tools have been applied to many industrial projects as well as the EUCLID space mission project, including more than ten modules. The obtained results demonstrated the effectiveness of the proposed tools.**

Keywords—EUCLID space mission, Fault tolerance, Radiation Effects, Radiation hardening, Single Event Transient, Soft errors.

I. INTRODUCTION

Advanced digital circuits play an essential role in a growing number of applications. When these devices are used in mission-critical applications, the dependability of such devices becomes an important issue. One of the most critical environmental aspects that could lead to the failure of these systems is radiation. When a charged particle interacts within a device, it may cause a voltage pulse known as Single Event Transient (SET). Once a SET pulse is generated, it may propagate through the routing and logic resources of the circuit, and it may reach to a sequential element during its latching window and be captured by it and cause a Single Event Upset (SEU). The generated SEU might propagate to the output of the circuit, causing errors and malfunctioning of the system [1]. Considering the reprogrammable devices such as Flash-based FPGAs, the shrinking of device technology makes these devices more vulnerable to SETs. Due to the reduction of the node capacitance, even a radiation particle with low energy can create a voltage pulse in the circuit. On the other hand, increasing the clock frequency of recent circuits leads to a higher probability of SET pulses being captured by the storage elements [2].

Many works have been investigating Single Event Transient effects in digital circuits [3]. Among the available studies using FPGA technologies, FPGAs with Flash-based configuration cells are mainly addressed since their configuration memory cells are essentially immune to bit-flips. Therefore, SETs in the Flash-based FPGAs logic and routing resources are the major concerns of soft errors. Many works have been investigating the characterization of radiation-induced SETs in the sequential and combinational circuits to identify the type of SET generated within the silicon structure of Flash-based FPGAs [4][5].

Several studies have focused on the evaluation of SET propagation using electrical simulation. Even though these methods are sufficient to analyze the propagation of SET pulses, they do not evaluate the broadening and filtering effect of SET pulses traversing logic and routing resources known as Propagation Induced Pulse Broadening (PIPB) effect. Besides, these approaches are time-consuming. Thus, they are not efficient in being applied to an industrial design flow with an enormous amount of resources.

On the other hand, several works have been proposed to mitigate the effect of SET. One kind of proposed method is the classical temporal or/and spatial redundancy-based fault-tolerant approaches such as Triple Modular Redundancy (TMR) and Error Detection and Correction Coding (EDCC) [6][7]. Furthermore, there exist methods acting on the placement and routing phases for improving the transient mitigation on VLSI devices [8]. Some works have investigated the effect of charge sharing on the shrinking of the SET pulses [9][10].

The main contribution of the present work is the complete identification of the SET life-cycle from generation to the mitigation of the pulse. The research work starts by focusing on the first phase, generation of SET pulses, by proposing a new simulation tool named Rad-Ray. Rad-Ray is based on the three-dimensional simulation, able to model and simulate the effects of the passage of heavy ions into the silicon matter of modern Integrated Circuits and calculates the transient voltage pulse response on the output nodes. Several works have studied the internal structure of a single cell and provide relevant results regarding the effect of heavy-ion on the fundamental physical mechanism of the cell [11]. However, they are not suitable to support an efficient analysis of the SET generation phenomena on the entire IC. Therefore, a global approach that includes a physical mechanism to model the generation of SET

978-1-7281-9113-3/20/ $31.00 ©2020 IEEE

pulse in the circuit is required. The main innovation of the Rad-Ray tool is the capability to model the heavy-ion tracks through the different volumes of digital circuit cells applicable to an entire IC. To confirm the efficiency of the proposed method, we performed a radiation test experiments at UCL, Cyclotron of Louvain-la-Neuve facility. We performed a comparison between the obtained results from the radiation test and the Rad-Ray simulation tool, which shows the efficiency of the proposed tool [12].

After the generation phase, the research continues by evaluating the impact of the generated SET pulse on the circuit functionality. To do so, a SET analyzer tool, name SETA, has been developed. SETA focuses on the propagation of the SET pulse from its generation node until the reach of the storage element. Differently from the already developed tools, SETA considers the effect of PIPB on the SET propagation in the circuits and reports the sensitive storage elements of the circuits. SETA is known as the first SET analyzer tool applicable to large industrial circuits. Thanks to SETA, the vulnerable storage elements of the circuit have been identified, which leads to the proposed mitigation technique based on the insertion of Guard Gate (GG) filtering logic. Several approaches are applying GG filtering logic to filter the SET pulses before reaching to the Flip-Flops. Taking an example, the new radiation-hardened RTG4 Flash-based FPGA provides the possibility to add the GG logic for a SET pulse with a fixed duration to all the FFs of the design. Still, it is not possible to tune the filtering capability to SET pulse with different duration. Besides, the filtering logic should be applied to all the FFs or none of them; it is not possible to apply the logic selectively to the vulnerable FFs. Our proposed method has been known as the first one that applies the filtering blocks not before all the storage elements but only to the sensitive FFs of the design. Moreover, it allows us to tune the filtering capability concerning the duration of the SET pulse. This mitigation solution leads to the drastic reduction of the area and performance overhead comparing to the previous solutions. The proposed analysis and mitigation tools have been applied to many industrial circuits [13], including an SoC mapped on Microsemi ProASIC3 Flash-based FPGA within the framework of the EUCLID space mission project for monitoring the dark space carrying by European Space Agency. The experimental results present an evaluation of SET phenomena affecting the circuit during its realistic operational lifetime of 6 years with the mitigation method applied, confirming the efficiency of our proposed analysis and mitigation tool. Moreover, the developed SET analysis and mitigation workflow have been part of the handbook *Space Product Assurance Techniques for Radiation Effect Mitigation in ASICs and FPGAs handbook*, published by the European Space Agency.

The paper is organized as follows. Section II provides the background on Single Event Transient phenomena and research works dedicated to SET. Section III describes the workflow from the generation until the mitigation of SET pulses. Section IV elaborates on the experimental result obtained on the characterization of SET on Flash-based FPGAs. Section V is dedicated to the EUCLID space mission project, the results obtained on the analysis, and mitigation of EUCLID netlist. Finally, conclusions and future works are drawn in Section VI.

II. Background and Related Works

The Single Event Transient effects in nanoscale devices are mostly caused by charged particle strike. When a highly charged particle crosses the silicon junction, the produced free mobile carriers are concentrated within the depletion region of a p-n junction in one of the sensitive transistor nodes, illustrated in Figure 1.

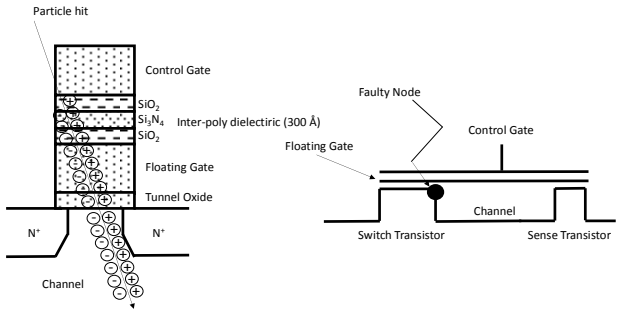


Fig. 1. Floating Gate Transistor layout in the 130 nm Flash-based FPGA and the sensitive correspondent node generating a transient pulse.

This phenomenon can cause a spurious variation, or glitch, of the voltage level at the output of the transistor that is called Single Event Transient (SET). The SET shape depends not only on the incident particle but also on the device technology node, which it strikes. Indeed, it is a function of not only LET of the particles and its incident angle but also the materials encountered in its path inside the device and the electric field present at the moment [14]. Transient errors may cause two significant issues. In a case that a storage element junction is affected, it may create a Single Event Upset (SEU), which consists of the flipping of the original logic value of the storage element. On the other hand, if it hits a transistor as part of the combinational logic generating a SET, the pulse can propagate through routing and logic resources in the circuit until a sequential element captures it, typically a Flip-Flop (FF), becoming a bit error thus propagating its effect during the circuit execution [15].

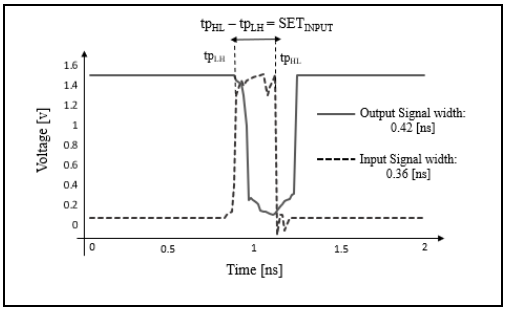


Fig. 2. The SET pulse propagating through an Inverter Gate, broadening due to the PIPB effect.

However, when SET pulses are traversing the logic and routing resources, they undergo a severe pulse width modulation. Such a phenomenon is known as Propagation Induced Pulse Broadening (PIPB) effects [9]. Figure 2

represents a SET pulse of 0.36 ns propagating through an Inverter gate, which is broadening due to the difference between the propagation delays.

III. On the Generation, Analysis and Mitigation of SET

The target of the proposed environment is to provide an effective methodology for the analysis of the SET sensitivity of an industrial circuit considering the radiation profile of the mission and the effect of the layout and geometry of the circuit implemented on Flash-based FPGAs and applying a tunable mitigation mechanism based on the performed analysis. The developed tools chain is integrated with the standard FPGA design flow, as represented in Figure 3.

Starting from the Hardware Description of the design, going forward through synthesis, mapping, and place and route, the commercial design flow generates the post-layout netlist along with the Physical Design Constraints (PDC) and Standard Delay Format (SDF) file. These exported files, together with the layout description of the circuit in terms of Graphic Data System-II (GDS-II), layer, and material and radiation profile of the mission, have been provided to the developed toolchain.

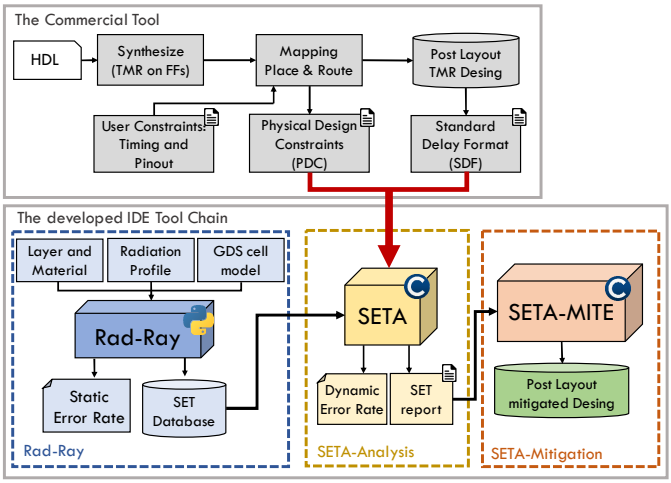


Fig. 3. The developed workflow for the accurate evaluation of the SET effects on SoC implemented on Flash-based FPGAs.

As a first step, the Rad-Ray tool has been developed to perform a radiation analysis of the circuit under the test concerning the radiation profile of the mission and geometry and layout of the implemented circuit. Rad-Ray is a newly developed simulation approach that can model and simulate the effect of the passage of heavy ions into the silicon matter of the modern Integrated Circuit and generate the transient voltage pulse response on the output node. As a result, Rad-Ray computes the features of the expected SET pulse in terms of duration and amplitude of the pulse.

The predicted SET distribution is used in the next phase to perform an adequate SET characterization on Flash-based FPGAs. The behavior of the SET pulse traversing through different logic gates in different technology nodes is different, which leads to different PIPB values. Exploiting internal electrical injection, the predicted source SET pulse has been generated inside the device, and the behavior of the pulse propagating through several logics gate and routing interconnection is identified in terms of the PIPB value for each logic gates. This PIPB characterization, together with the netlist and physical design constraints of the circuit, is provided to SETA to perform SET analysis of the circuit under the test automatically. SETA considered the pulse propagation behavior through the routing and logic resources of the design, taking into account the PIPB effect. As a result, it generates the SET sensitivity report for all the FFs in the design. The sensitivity report is used to apply a selective mitigation technique. The mitigation tool modifies the original netlist of the circuit by inserting the Guard Gate (GG) structure at the inputs of the sensitive FF reported by the SET analyzer and provide the mitigated netlist.

A. *Rad-Ray Radiation Analysis*

Rad-Ray is an in-house-developed tool for simulating the passage of radiation particles through the silicon matter of modern integrated circuits and generating the transient voltage pulse response. The tool receives the layout, layer material, and depth of each layer together with the radiation profile of the mission as inputs. Rad-Ray starts with the GDS-II of the circuit and generated the 3D mesh structure of the layout of the circuit. Based on the size and shape of metallization and volumes of the cells concerning the radiation profile of the mission which includes the type of ions existing in the environment under the study, the energy and flux of the particles, the tool simulates the effects of highly charged particles traversing the silicon junction of the device.

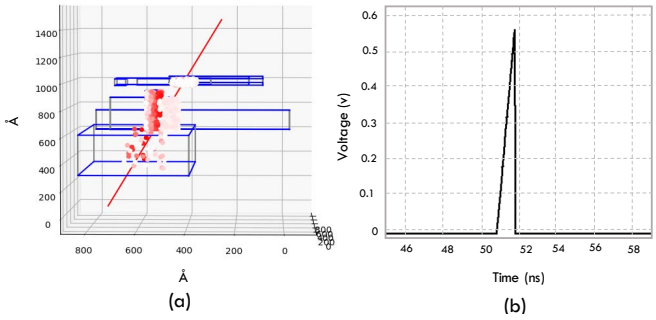


Fig. 4. Single Heavy-Ion particle strike within the cell under the analysis (a) releasing charge during its propagation. Colored spots provide the value of the corresponding released charge distributed for each cell volume. (b) The outcome of the Rad-Ray method visualized, thanks to the HSPICE simulation.

The produced free mobile carriers are concentrated within the depletion region of a p-n junction in the transistor sensitive parts individuated by the Rad-Ray algorithm. The eV transmitted by the particles, depending on the traverse section of the cell, can cause a voltage glitch that is propagated to the output of the transistor and finally to the output of the cell, generating a SET effect into the circuit.

Rad-Ray mimics the track passage of ion ray by generating a list of starting and ending coordinates of each particle and calculates the amount of energy loss during this passage in each node. Figure 4 (a) represents the heavy-ion releasing its

energy during its propagation in the cells. The propagation of particles terminates by reaching to the final coordinates. Finally, Rad-Ray converts the transmitted energy in volts and plots the voltage value of each cell. Figure 4 (b) shows the generated SET pulse within the cell under the analysis. The result is a report which elaborates the generated transient pulse in terms of duration and amplitude of the voltage pulse at the output of the analyzed cell.

To confirm the efficiency of the developed simulation tool, we performed a radiation test campaign at the Université Catholique de Louvain (UCL) Heavy Ions Facility. Conducting a comparison between the obtained result from the radiation test scenario and the Rad-Ray simulation tool shows a close alignment between the two results [12].

B. *Effective Characterization of SET*

The behavior of the SET pulse in the circuit, the broadening, and filtering, is dependent on the technology of the implemented design. To evaluate the life-cycle of SET from its generation to the reach of a storage element, we developed a methodology for the comprehensive characterization of SET within the technology under the study to investigate the broadening and filtering of a SET pulse propagating through different logic gates knowing as PIPB effect. The proposed method is based on two parts: the internal electrical injection of the SET pulse and the characterization of the pulse propagation. To generate the SET pulse, we used an in-circuit internal electrical pulse generator. The pulse generator structure has been implemented in the FGPA architecture by programming logic cells with the corresponding pulse generator scheme illustrated in Figure 5. Using this approach, it is possible to control the parameters of the generated pulse as well as the location and time of generating SET pulse while avoiding the filtering effect of the I/O structure.

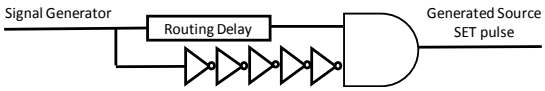


Fig. 5. The developed logic scheme for the in-circuit Internal Pulse Generation.

The propagation has been analyzed considering two conditions: the former consists of the presence of different logic gates after the SET pulse injection; the latter is related to the possibility that the propagation traverses several nodes with various fan-out gates. The basic principle of the developed characterization method is represented in Figure 6. This principle assumes that any kind of SET generated in sensitive nodes and propagated in different position encounter different points. At any point in its logic gate traversing, the SET propagation is dependent on two main factors: the subsequent combinational logic gates observable in front of the pulse and the fan-out gates present in a given position during the pulse propagation. To study the life-cycle of the SET from its generation to the reach of a destination point such as Flip-Flop or an I/O pin, we observed the behavior of the SET by configuring different test setup while the SET has been injected using the same logic topology and evaluating the PIPB effect for the technology under the study.

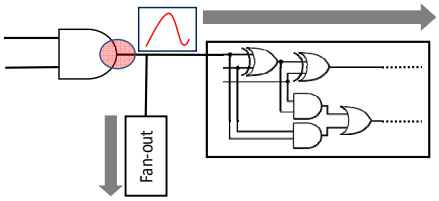
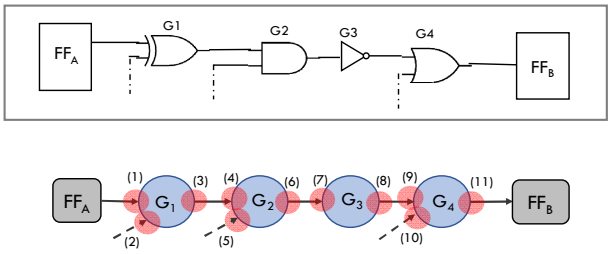


Fig. 6. The characterization main method conditions with two observability points: toward next logic gates and fan-out

C. *Analysis of SET*

SETA is a developed tool for evaluating the impact of the SET on the circuit functionality considering the PIPB effect, targeting large scale industrial design. To do so, SETA starts with elaborating on the Physical Design Constraint (PDC) file containing the placement information of the logic resources used in the circuit. Together with logic information extracted from the post-layout netlist, SETA generates a Physical Design Description (PDC) file for storing the elaborated circuit. In this file, I/O pins, FF, RAM, or ROM ports are identified and considered as terminal nodes, and combinational logics are categorized as intermediate nodes connected through routing segments. SETA inserts the SET pulse in all the inputs and outputs of every single intermediate node of the design. The features of the inserted SET pulse in terms of amplitude and duration are reported by radiation analysis performed by the Rad-Ray tool. SETA propagates the inserted pulse until it reaches a terminal node of the design. During this propagation, SETA takes into account the PIPB value dedicated to each logic gate. The type of the gates and routing interconnection is provided in the PDD file, while the behavior of the pulse propagating through each of this gate is provided in the PIPB characterization reported from the previous stage. Therefore, SETA propagates the pulse until the storage element considering the PIPB effect. In the end, SETA reports the SET sensitivity for each terminal node, in terms of the probability of SET causing bitflip for each Flip-Flop.



Injection [#]	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)
SET reach to FF [ns]	0.4	0.42	0.3	0.29	0.45	0.3	0.32	0.3	0.4	0.42	0.42

Fig. 7. An Example of SETA applied to a portion of the circuit considering Source SET of 0.35 ns. Node 5 causes the biggest SET pulse at FF_B.

Figure 7 represents a small portion of a circuit. SETA inserts SET pulses reported by Rad-Ray in the inputs and outputs of each logic gates represented by *Red-Cycle* in Figure 7 and propagates the inserted pulse until the terminal node, FF_B, in the figure. In the end, it reports the biggest SET pulse in terms of the duration of the pulse for each FF. in the case

represented in Figure 7, the SET pulse inserted at point 5 introduces the biggest SET pulse duration in the FF_B which has been reported by SETA.

D. Mitigation of SET

The SET mitigation is realized through modifying the original circuit netlist by inserting proper GG structure, as illustrated in Figure 8. Each GG structure is composed of three 2-input NAND gate and parameterized number of inverter gates determined by desired SET filtering capability.

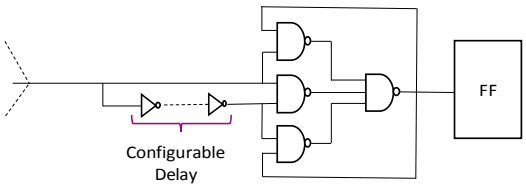


Fig. 8. The GG scheme for filtering SET at the input of sensitive Flip-Flop.

The mitigation algorithm firstly calculates the maximal PIPB coefficient for each used resource according to the results generated by SETA. The coefficient is computed for each logic gate as $\Delta B_{logicgate}$ and each routing net as $\Delta B_{Routing}$. The final PIPB coefficient ($\Delta B_{logicpath}$) of path reaching FF is the combination of all logic gates and routing segments coefficients. The positive value of the coefficient corresponds to a broadening effect, while a negative value correlates with the filtering of the SET pulse.

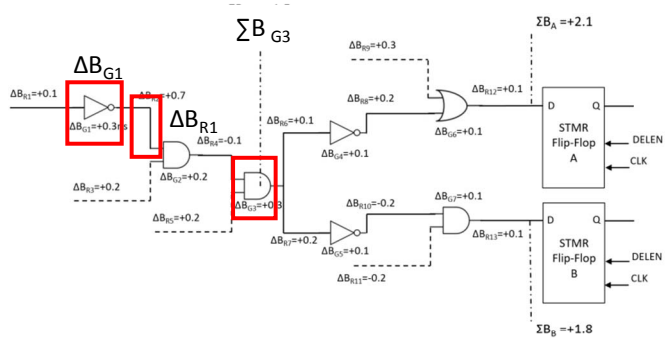


Fig. 9. Identification of gate and routing for Guard-Gate insertion.

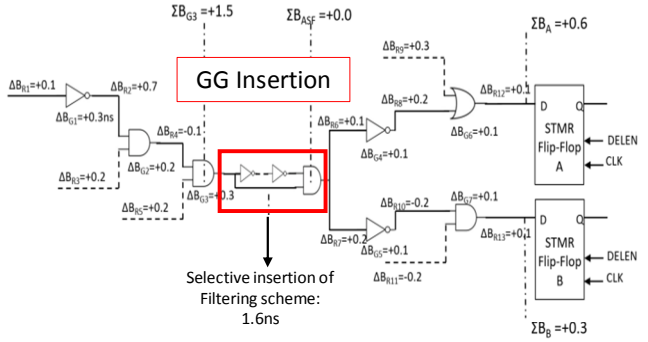


Fig. 10. A generic insertion of the SET filtering element within a circuit structure.

IV. Experimental Results on SET Characterization on Flash-based FPGAs

To study the life-cycle of the SET traversing different logic gates, we developed several test setups, focusing on the behavior of the pulse traversing different logic gates. The in-circuit electrical injector is used to generate SET pulse internally. We collect results by injecting SET pulses at the start of the developed test setup and observing the SET pulse reaching the end of the test setup in terms of the duration and amplitude of the pulse reaching and calculating the PIPB effect.

Four types of test structures have been implemented for the SET characterization. According to the circumstances of the typical circuit design, the first scenario has been dedicated to the combinational logic, represented by a gate-string, while in the second scenario, the fan-out has been added to the gate strings. Going into details of the typical circuits, we notice the existence of divergence and convergence of a combinational path in the design. Therefore, we continued the analysis, modifying the implemented design to study the effect of chain convergence and divergence in the SET propagation. These scenarios have been performed for the basic logic gates such as INV, AND, NAND, OR, NOR, and XOR. However, in this document, due to the limited space, the obtained result regarding the SET characterization of Inverter gates have been reported. The Experimental analysis has been executed on a Microsemi ProASIC3 A3P250 Flash-based FPGA. For the entire performed test, we analyzed the result obtained from the observed SET at the end of the gate string. We classified the results in terms of the ratio between the output SET at the end of the chain and the source SET at the start of the chain, calculating the PIPB effect. Also, we measured the delay between the source SET injected at the start of the chain, and output SET reached to the end of the string [16].

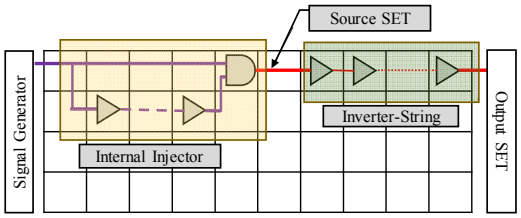


Fig. 11. An overview of the developed setup and placement layout for the chain of inverters

A. First Scenario: Inverter-string

The first analysis consists of the characterization of the logical gates chain concerning the injected SETs. For this purpose, we used inverter gates as logical gates while we used the different lengths of inverter-string, as it is illustrated in Figure 11.

Using in-circuit electrical injection, we generated the SET pulse with different durations of the pulse internally. We injected the generated pulse to the start of the chain while observing the pulse propagating to the end of the chain.

As it is represented in Figure 12, by increasing the length of the string, the PIPB is increasing. Besides, the delay is progressively increasing regarding the number of INVs in the chain.

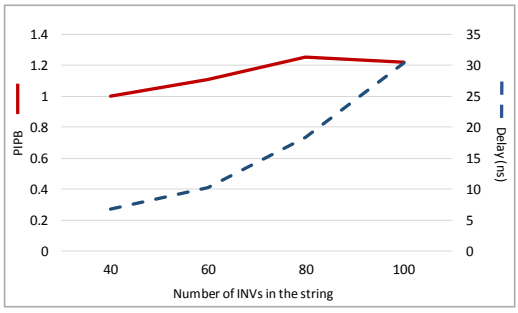


Fig. 12. Propagation Induced Pulse Broadening and Delay with source SET of 0.65ns

B. *Second scenario: Inverter-string and fan-out*

The second scenario is an extension of the first one, which includes various inverter gates as a fan-out connected to the beginning of the string, represented in Figure 13.

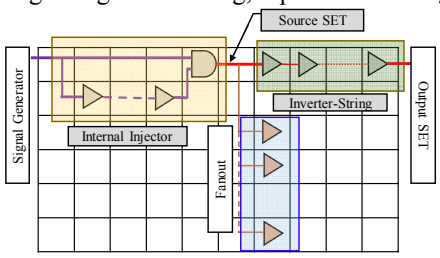


Fig. 13. An overview of the placement and layout for the simultaneous analysis of loads and chain of gates.

The design of the place and route of fan-out provides the minimal distance connection between each cell. As represented in Figure 14, the PIPB is progressively attenuated by increasing fanout, while for a fixed number of gates in the chain, the delay of the circuit is not changing. Therefore, it opens a window to a new mitigation mechanism to evaluate the fan-out as the filtering part of the architecture to modify the PIPB without introducing a delay to the circuit.

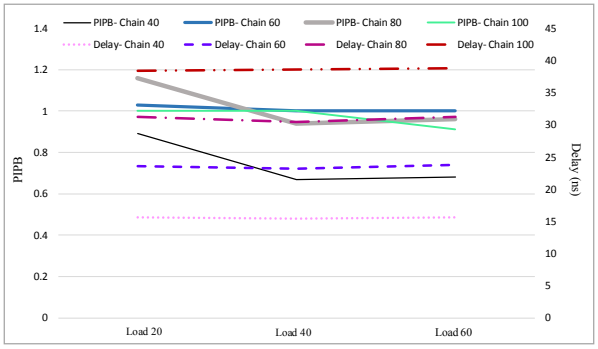


Fig. 14. PIPB and delay report of the source SET and output SET

A mitigation solution based on adding charge sharing logics into the circuit netlist is proposed. For nanometer Flash-based FPGAs, the proximity of device nodes results in charge collection in multiple logic switches when a single heavy ion strikes a node. The phenomenon results in different transient pulse shapes related to the LET absorbed by the switch junction. The proposed mitigation acts by inserting programmed logic gates in ad-hoc netlist nodes [18], represented in Figure 15.

This method has been known as the first one able to implement SET tolerant circuits on Flash-based FPGAs with zero timing overhead. The effectiveness of the proposed algorithm has been evaluated on several benchmark circuits by means of SET fault injection using a Flash-based FPGA development board, which shows an improvement of resilience of 4 times with respect to the state of the art solution with no timing degradation.

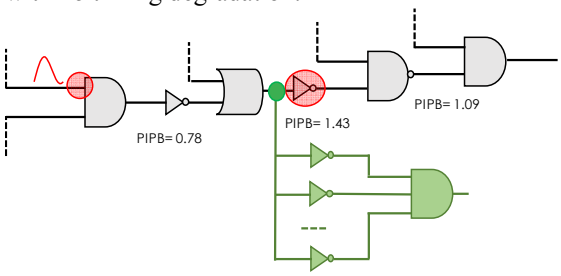


Fig. 15. Adding charge sharing logic for filtering SET pulse

C. *Third Scenario: analysis of chain divergence*

For the next step, we moved forward toward the conditions of typical logical designs and considering the characteristics of the SET while there is an occurrence of divergence of combinational paths. If we consider the typical *Adder* structure, the SET pulse generated or propagated to the divergence node, might propagate to both outputs of the adder and create multiple SEU, as represented in Figure 16 (a). Therefore, we modified the previous test structure to reconstruct the SET characterization in divergence point, Figure 16 (b).

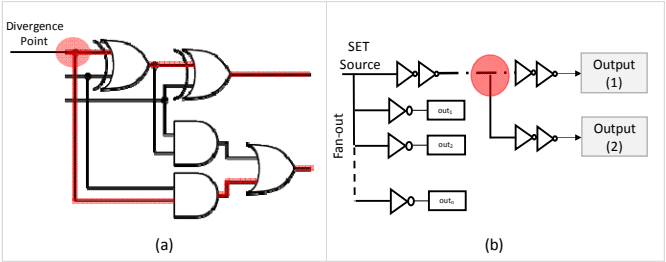


Fig. 16. (a) Logical scheme of full adder affected by SET in the divergence point. (b) Test setup for divergence scenario

D. *Fourth Scenario: Chain convergence*

After divergence point in the circuit, the following typical condition is when the SET traverse through divergence point, propagate through different logical path and routing, and reach to the convergence point of the circuit as represented in Figure

17 (a), a typical full adder circuit. To reconstruct this phenomenon, we design a simple circuit, illustrated in Figure 17 (b).

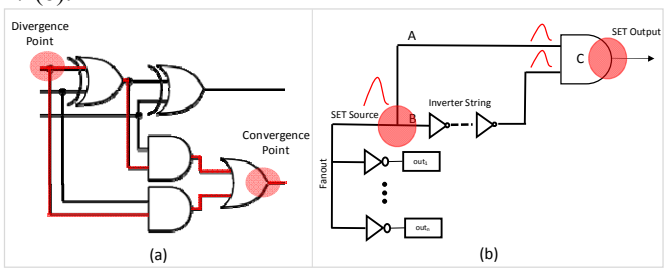


Fig. 17. (a) The logical scheme of full adder affected by SET at the divergence point propagated until the convergence point. (b) Test setup for convergence scenario

Figure 18 represents the obtained results, demonstrating that the respective counterpart only marginally influences the PIPBs of the two strings. However, we also identify a particularly relevant phenomenon happening due to the overlapping of the outcome of one SET. As represented in Figure 18, the SET can propagate through two convergence paths. If there is a massive difference between the propagation delay of the two paths, paths 1 and 2, the two SET shapes are provided as two separate pulses, Figure 18 (a). Vice versa, in case the delay between the paths is minimal, a convergence SET is obtained, which is characterized by a considerable width, which is typically the case of combinational arithmetic structures, represented in Figure 18 (b).

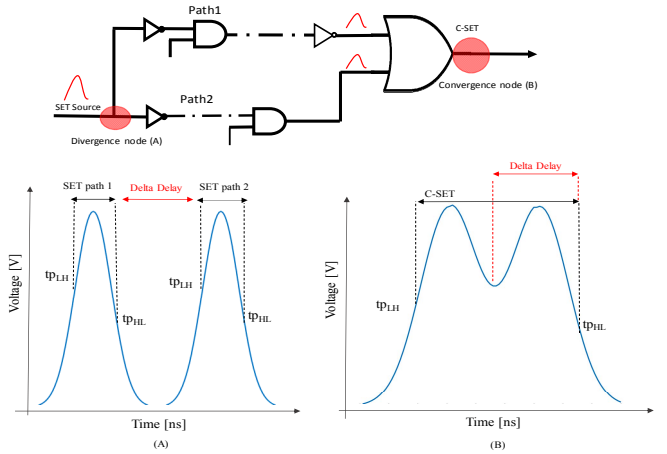


Fig. 18. An example of SET propagated through two convergence paths and generating: two independent SET pulse (left) and a convergence-SET pulse (right).

To evaluate the behavior of implemented circuits toward Convergence-SET phenomena automatically, in collaboration with European Space Agency, an efficient tool has been developed which takes into account the timing analysis of the circuit and provides the sensitivity of the circuit regarding this phenomenon [17]. Thanks to the developed method, we are able to cover the specific cased of the circuit while there is an occurrence of divergence and convergence points.

V. Experimental Results on EUCLID Space Mission Project

The proposed analysis and mitigation methodology have been performed on a System-on-Programmable-Chip (SoPC) embedded in the EUCLID space mission designed for monitoring dark space to study the geometry and nature of the dark universe.

A. EUCLID Space Environment

EUCLID space segment will be spacecraft placed into an orbit around L2 (around 1.5 million kilometers from the earth) with a duration of 6.25 years with the launch planned for 2021. EUCLID spacecraft will host two instruments: Near-Infrared Spectrometer Photometer (NISP) and VISible Imager (VIS). Both instruments make significant use of functions implemented in FPGA devices, while the controller part of the units is adopting RTAX devices, the elaboration part is essentially adopting Radiation tolerant ProASIC Flash-based FPGA. For this device family, in particular, we considered that the technology is guaranteed to be Single Event Latchup (SEL) immune up to 68MeV/cm2/gm, the Total Ionizing Dose (TID) can be up to 30 krad while no SEU effects are expected in the configuration memory. Considering this scenario, a radiation profile has identified as the maximum exposure of 4krad, which leads to the generation of SET pulses with a duration between 0.43 ns and 0.52 ns [19].

B. EUCLID Design

Microsemi ProASIC3 A3P3000 Flash-based FPGA device has been used for implementing the EUCLID netlist, while Microsemi Libero SoC 11.7 is used as the design tool to implement the EUCLID design and export the input files for SETA tool.

To evaluate the mentioned circuit regarding SET, we start from the original netlist. The netlist has been implemented using the VHDL, while TMR has been applied to all the FFs. The netlist with TMR FFs has been through place and route for the target FPGA, performed with Microsemi Designer. The post-layout netlist has been provided to SETA flow to perform the SET analysis and mitigation based on the performed analysis.

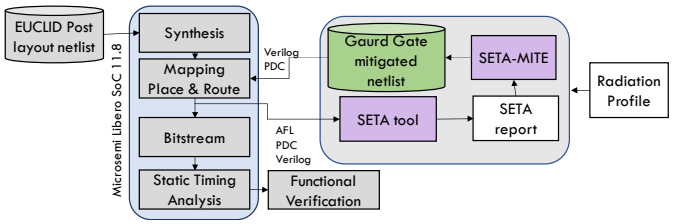


Fig. 19. The EDA flow adopted integrated both commercial tools (Microsemi Libero SoC 11.8) and the SET analysis and mitigation flow.

The EDA flow we adopted is illustrated in Figure 19, showing each step, including the Static Timing Analysis, which in the experiment, we need to run the tool for several iterations due to timing failure. At the first iteration, SETA evaluates the

impact of SETs on the circuit functionality by calculating the SET propagation in all the circuit nodes and the maximal SET pulse width at the input of each Flip-Flop, while mitigation tool focuses on the filtering of the SET reaching to the FFs by inserting GGs. The following concept has been categorized into three sections. The first part is dedicated to reporting the SET sensitivity analysis of the EUCLID original netlist. While the second part is dedicated to elaborating the steps for mitigating the netlist, and the third part is presenting the SET analysis result of the mitigated netlist.

C. *Analysis of EUCLID original netlist sensitivity to SET*

The characteristics of the EUCLID netlist are reported in Table I concerning resource usage and Table II concerning the timing characteristics. In Table II, the components *CLK_60M*, *CLK_20M*, *Clk_60M_buff* and *Clk_30M* are the components in the design corresponding to different clock domains whose frequencies are as indicated in the name, while *SPW_CTLR0* and *SPW_CTRL1* are two SpaceWire controllers implemented in the design.

The SETA tool has been applied to individuate the most sensitive node location. Considering the radiation profile features which report the SET characteristics, SET pulses width equal to 0.519, 0.488, 0.462, and 0.437 ns are used by SETA flow to evaluate the sensitivity of the design against SETs. The computational time required by the SETA tool for three different SET pulses has been of approximately 65 hours, while the used resource area on the A3P3000RT is 63.65%. Please note this time depends on the performance of the computer the tool is executed on, in our case is a VirtualBox machine on the mid-range laptop PC, while considering running the tool on a more powerful workstation/server, the computational time should be able to shorten more.

TABLE I. CIRCUIT RESOURCES OF THE EUCLID NETLIST BY TYPE

Type	*Core Tiles [#]*
Combinational Logic	30,190
Sequential Elements (FFs)	17,718

TABLE II. CIRCUIT RESOURCES OF THE EUCLID NETLIST BY TYPE

Reference Name	*Period [ns]*	*Frequency [MHz]*
CLK_60M	12.097	82.665
CLK_20M	30.156	33.161
SPW_CTRL0	11.177	89.469
SPW_CTRL1	13.437	74.421
Clk_60M_buff	12.097	82.665
Clk_30M	28.022	35.686

Table III is reporting the sensitivity of EUCLID design regarding SET where *Filtered* is reporting the number of FF in which the SET pulses that have been filtered before reaching to a FF excluding FFs implemented on I/Os*; Partially Filtered* is reporting the number of FF that are fronting SET pulses that the width of the pulse has been reduced, however, not completely filtered. Therefore, since the width of the pulse reaching to FFs is shorter, the probability of the pulses to be sampled by FFs is reduced. While Broadened is reporting the number of FF that are facing the SET pulses that during their propagations until reaching to FFs, their pulse widths have been increased, this kind of pulses is creating the most critical situation since by increasing the width of the pulse, the probability of the pulse being sampled by storage elements and/or FFs is also increased.

TABLE III. SINGLE EVENT TRANSIENT ANALYSIS FOR SET RANGING FROM 0.43 NS TO 0.52NS

Source SET [ns]	*Filtered [#]*	*Partially Filtered [#]*	*Broadened [#]*
0.520	11,130	0	6,542
0.488	11,130	0	6,542
0.4462	11,130	0	6,542
0.437	11,162	6,510	0

Figure 20 reports the SET distribution of the original netlist. In this figure, the horizontal axis is representing of the ID of the FFs in the original netlist that is partially filtered or broadened, while the vertical axis is showing the maximal SET pulse width reaching the corresponding FF.

As can be observed, for shorter SETs such as 0.43 ns, the source SETs have been electrically filtered before reaching to the FFs or are not broadened while propagating through the logics and routing nets of the circuit. Therefore, the SET pulse reaching the FFs are almost the same width as the source SETs. This phenomenon is happening due to the target technology's behavior regarding SET.

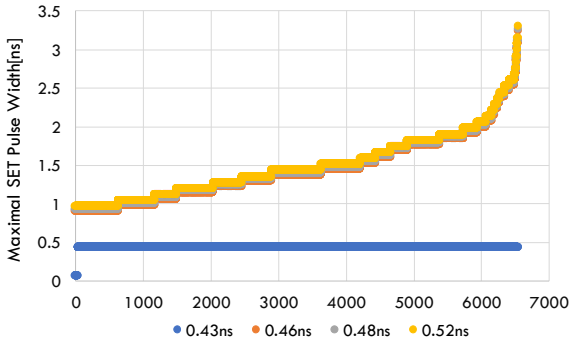


Fig. 20. The SET distribution obtained on the original EUCLID netlists

On the other hand, with higher source SET pulse width, such as 0.52 ns, the SET pulses are facing a drastic increase of the width while traversing the circuit, which causes these SETs to be more critical for the mission.

D. *Mitigating the EUCLID design netlistGaurd Gate Delay Coefficient*

After performing the SET analysis, the netlist, together with the report of the SET sensitivity evaluation, is provided

to the mitigation tool to insert GG logic for filtering the SETs. In Figure 21, it is illustrated a demonstration of GG insertion within the Euclid design.

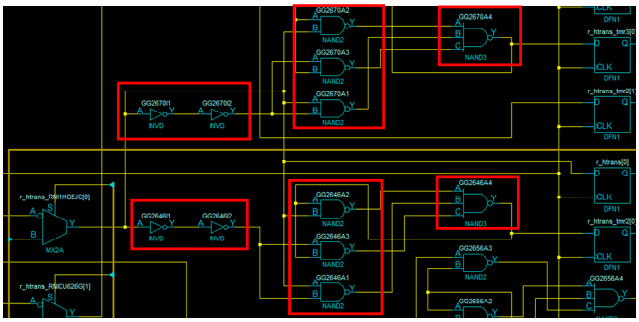


Fig. 21. An example of Guard Gate automatic insertion on a portion of the EUCLID design.

Based on the sensitivity report by SETA, we firstly set the filtering capability of the GG mitigation tool to 1.350 ns to provide the maximal broadening reduction and filter all the SETs before reaching to FFs. Even though this filtering capability is efficient for removing propagated SETs, timing closure regarding the 30 MHz clock domain fails. Therefore, we reduced the GG mitigation insertion to 1.2 ns.

TABLE IV. TIMING ANALYSIS FOR THREE INTERACTION OF GUARD GATE MITIGATION TOOL

Guard Gate Delay coefficient			
Reference Name	***1.4 ns***	***1.2 ns***	***1.0 ns***
	Frequency [MHz] @ 4krad		
CLK_60M	69,845	68,304	69.793
CLK_20M	36,480	32,234	35,045
SPW_CTRL0	76,430	74,234	79,764
SPW_CTRL1	81,832	80,024	83,043
Clk_60M_buff	61,430	64,780	69,793
Clk_30M	27,640	29,550	31,248

TABLE V. AREA OVER-HEAD REPORT FOR THREE ITERATION OF GUARD GATE MITIGATION TOOL

Guard Gate Delay Coefficient [ns]	***Area Over-head [%]***
1.4	8
1.2	3.8
1.0	1.4

However, static analysis reports the timing closure failure regarding the 30MHz clock domain again. As the final step, the GG mitigation insertion has been reduced to 1.0 ns maximal broadening reduction to achieve the successful timing closure. In Table IV, three iterations of the GG mitigation tool, implementation, and timing analysis have been reported, while Table V reports the area overhead of three iterations.

E. Analysis of EUCLID mitigated netlist sensitivity to SET

We evaluated the sensitivity of the mitigated circuit regarding SET pulses whose widths are between 0.43 ns and 0.5 ns. Figure 22 reports the SET distribution of the mitigated netlist. As it can be observed, the SET pulses below 0.4 ns will be electrically filtered before reaching the FF inputs.

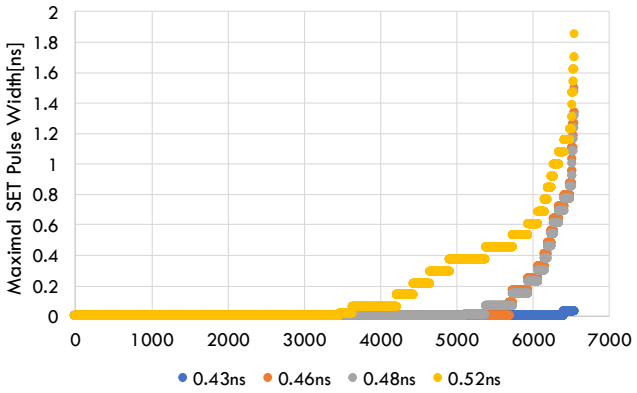


Fig. 22. The SET distribution for mitigated netlists

Figure 23 represents a SET mitigation comparison between the original netlist and the mitigated netlist. As can be observed, the results report removal of 97% of broadened SETs while the 3% remain with reduced pulse width around 50%. For example, a pulse with a width of 3.2 ns in the original netlist has been partially filtered down to 1.9 ns in the mitigated version.

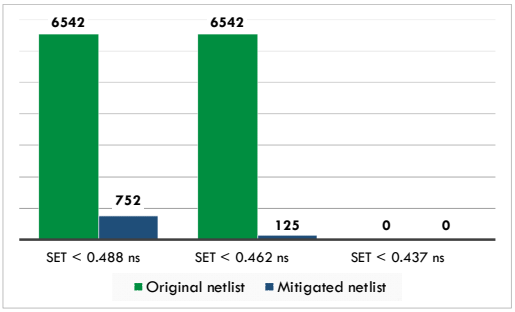


Fig. 23. A Comparison of SET distribution between the original netlist and the mitigated netlist.

VI. CONCLUSIONS AND FUTURE WORKS

In this research work, a comprehensive analysis and mitigation flow of Single Event Transient has been developed and applied to the EUCLID space mission project in collaboration with the European Space Agency and OHB Company. The workflow has been known as the *Best EDA tool for improving design automation for integrated circuit and system* by the IEEE Council on Electronic Design Automation (CEDA). Several radiation tests have been performed on modern devices at CERN and UCL facility in collaboration with European Space Agency, CERN, Thales Alenia Space, OHD Italia, and IROC in order to confirm the

reliability of the developed toolchains [20][21]. The developed tools are going to be used for performing radiation analysis of the HERA spacecraft project with the launch in 2024 in collaboration with the European Space Agency.

Even though the main part of this thesis has been dedicated to the study of transient fault, the second part is dedicated to permanent focusing on Single Event Latch-up (SEL) [22] and Total Ionizing Dose (TID) [23].

Further research activates have been planned for extending the current work to ASIC designs in collaboration with the IHP company, where the placement of logic gates and layout of routing segments have much higher controllability than FPGA devices. Therefore, more options and possibilities for optimization regarding SEE sensitivity and overall reliability of the system need to be investigated and exploited.

However, radiation effect is not only a critical issue for avionic and space applications, but considering High Performance Computing applied in the automotive field, the dependability of these devices is becoming an important issue [24]. Therefore, I have been involved in several projects in collaboration with General Motors Company in order to evaluate the reliability of High Performance Computing devices such as GPGPU for automotive application.

ACKNOWLEDGMENT

I would like to thank my supervisor, Professor Luca Sterpone, for his exceptional support during my Ph.D. program and all the colleagues from the CAD and Reliability group of Politecnico di Torino. I would also like to thank all the colleagues I had the honor to collaborate with, especially Davide Merodio Codinacs, From the European Space Agency for providing me the unique opportunity to be part of the EUCLID spacecraft team.

REFERENCES

[1] V. Ferlet-Cavrois, L. W. Massengill and P. Gouker, "Single Event Transients in Digital CMOS—A Review," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1767-1790, June 2013.

[2] A. Dixit and A. Wood, "The impact of new technology on soft error rates," in *International Reliability Physics Symposium*, Monterey, CA, 2011, pp. 5B.4.1-5B.4.7.

[3] S.Sayil, "A survey of circuit-level soft error mitigation methodologies," in *Analog Integrated Circuits and Signal Processing*, 2019, pp. 63-70, doi: 10.1007/s10470-018-1300-8.

[4] N. Battezzati *et al*., "On the Evaluation of Radiation-Induced Transient Faults in Flash-Based FPGAs," *14th IEEE International On-Line Testing Symposium*, Rhodes, 2008, pp. 135-140, doi: 10.1109/IOLTS.2008.47.

[5] S. Rezgui, J. J. Wang, E. C. Tung, B. Cronquist and J. McCollum, "New Methodologies for SET Characterization and Mitigation in Flash-Based FPGAs," in *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2512-2524, Dec. 2007.

[6] M. P. Baze, S. P. Buchner and D. McMorrow, "A digital CMOS design technique for SEU hardening," in *IEEE Transactions on Nuclear Science*, vol. 47, no. 6, pp. 2603-2608, Dec. 2000.

[7] M. D. Berg, H. S. Kim, A. D. Phan, C. M. Seidleck, K. A. LaBel and J. A. Pellish, "Single Event Induced Multiple Bit Errors and the Effects of Logic Masking," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 6, pp. 4192-4199, Dec. 2013, doi: 10.1109/TNS.2013.2290753.

[8] C. Liu, X. He, R. Liang, Y. Guo, "Detailed placement for pulse quenching enhancement in anti-radiation combinational circuit design" in *Integration, the VLSI Journal*, Vol. 62, March, 2018.

[9] S. Azimi, B. Du and L. Sterpone, "On the mitigation of single event transients on flash-based FPGAs," *IEEE 23rd European Test Symposium (ETS*), Bremen, 2018, pp. 1-2, doi: 10.1109/ETS.2018.8400715.

[10] S. Azimi, C. Desio, W. Yang and L. Sterpone, "A New Single Event Transient Hardened Floating Gate configurable logic circuit," in *IEEE 18th International NEWCAS conference*, 2020.

[11] H. Jiang, H. Zhang, J. S. Kauppila, L. W. Massengill and B. L. Bhuva, "An Empirical Model for Predicting SE Cross Section for Combinational Logic Circuits in Advanced Technologies," in *IEEE IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 304-310, Jan. 2018.

[12] L. Sterpone, F. Luoni, S. Azimi, and B. Du, "A 3D Simulation-based Approach to Analyze Heavy Ions-induced SET on Digital Circuits," in *IEEE Transactions on Nuclear Science*, doi: 10.1109/TNS.2020.3006997.

[13] L. Sterpone, S. Azimi, B. Du, D.M. Codinachs, R. Grimoldi, "Effective Mitigation of Radiation-induced Single Event Transient on Flash-based FPGAs", in *the ACM Great Lakes Symposimum on VLSI (GLSVLSI),* pp 203-208, May 2017.

[14] R. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Transaction on Device and Materials Reliability*., vol. 5, no. 3, pp. 305-316, Dec. 2005.

[15] M. J. Gadlage, P. J. Eaton, J.M. Benedetto, M. Carts, V. Zhu, T. L. Turflinger, "Digital device error rate trends in advanced CMOS technologies," *IEEE Transaction on Nuclear Science*., vol. 53, no. 6, pp. 3466-3471, Dec. 2006.

[16] L. Sterpone and S. Azimi, "Effective Characterization of Radiation-induced SET on Flash-based FPGAs," *17th European Conference on Radiation and Its Effects on Components and Systems (RADECS),* 2017, pp. 1-4, doi: 10.1109/RADECS.2017.8696255.

[17] L. Sterpone and S. Azimi, "Analysis of Convergence Single Event Traisents Effects in Flash-based FPGAs," *18th European Conference on Radiation and Its Effects on Components and Systems (RADECS),* 2018.

[18] S. Azimi, B. Du and L. Sterpone, "On the mitigation of single event transients on flash-based FPGAs," *IEEE 23rd European Test Symposium (ETS)*, 2018, pp. 1-2, doi: 10.1109/ETS.2018.8400715.

[19] S. Azimi, B. Du, L. Sterpone, "On the prediction of radiation-induced SETs in flash-based FPGAs, ", in *Microelectronics Reliability*, vol. 64, pp. 230-234, 0026-2714, 2016.

[20] L. Sterpone et al., "A Novel Error Rate Estimation Approach forUltraScale+ SRAM-based FPGAs," *NASA/ESA Conference on Adaptive Hardware and Systems (AHS),* Edinburgh, 2018, pp. 120-126.

[21] . Du, L. Sterpone, S. Azimi, D.M. Codinachs, V. F. Cavorios, C. Boatella, R.A. Garcia, "Ultra High Energy Heavy Ion Test Beam on Xilinx Kintex-7 SRAM-based FPGA" In *Transaction on Nuclear Science*, -ISSN 0018-9499, 2019.

[22] S. Azimi and L. Sterpone, "Micro Latch-Up Analysis on Ultra-Nanometer VLSI Technologies: A New Monte Carlo Approach," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2017, pp. 338-343, doi: 10.1109/ISVLSI.2017.66.

[23] Q. Zhang, S. Azimi, G. La Vaccara, L. Sterpone, B. Du, "A new approach for Total Ionizing Dose effect analysis on Flash-based FPGA,", in *Microelectronic Reliability*, vol. 67, pp, 58-63, ISSN 0026-2714, 2017.

[24] S. Azimi, A. Moramarco and L. Sterpone, "Reliability evaluation of heterogeneous systems-on-chip for automotive ECUs," *IEEE 26th International Symposium on Industrial Electronics (ISIE),* Edinburgh, 2017, pp. 1291-1296, doi: 10.1109/ISIE.2017.8001431.