

Re-thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era

Original

Re-thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era / Pedro, T., Rubino, R., Musolino, F., Crovetto, P.S.. - In: IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS. II, EXPRESS BRIEFS. - ISSN 1549-7747. - STAMPA. - 68:3(2021), pp. 816-822. [10.1109/TCSII.2021.3049680]

Availability:

This version is available at: 11583/2860335 since: 2021-06-25T12:36:26Z

Publisher:

IEEE

Published

DOI:10.1109/TCSII.2021.3049680

Terms of use:

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright

IEEE postprint/Author's Accepted Manuscript

©2021 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collecting works, for resale or lists, or reuse of any copyrighted component of this work in other works.

(Article begins on next page)

Re-thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era

Pedro Toledo, *Graduate Student Member, IEEE*, Roberto Rubino, *Graduate Student Member, IEEE*,
 Francesco Musolino, *Member, IEEE* and Paolo Crovetto, *Senior Member, IEEE*

Abstract—A steady trend towards the design of mostly-digital and digital-friendly analog circuits, suitable to integration in mainstream nanoscale CMOS by a highly automated design flow, has been observed in the last years to address the requirements of the emerging Internet of Things (IoT) applications. In this context, this tutorial brief presents an overview of concepts and design methodologies that emerged in the last decade, aimed to the implementation of analog circuits like Operational Transconductance Amplifiers, Voltage References and Data Converters by digital circuits. The current design challenges and application scenarios as well as the future perspectives and opportunities in the field of digital-based analog processing are finally discussed.

Index Terms—Digital-based analog processing, Analog and Mixed Signal Circuits, Dyadic Digital Pulse Modulation (DDPM), Digital-to-Analog Converter (DAC), Virtual Voltage Reference, Digital Operational Transconductance Amplifier (DIGOTA), Relaxation DAC (ReDAC).

I. INTRODUCTION

THE Internet of Things (IoT) is the vision of the world in which integrated circuits (ICs) are embedded in everyday life objects for gathering, processing, and exchanging useful information. The design of cubic-centimeter down to cubic-millimeter-scale [1], energy autonomous, pervasive sensor nodes envisioned in the IoT paradigm [2], however, raises stringent constraints on IC area (sub mm²), average power budget (from the low microWatt down to nanoWatt scale for nodes operated by tiny batteries or energy harvesters) and cost.

The IoT requirements are particularly difficult to be met for analog interfaces, which do not take advantage of CMOS geometrical scaling [3–5] and face specific design challenges due to the poor analog features of nanoscale transistors (as the feature size is shrunk from 0.5 μm to 22nm node, the transistor intrinsic gain drops from 180 to 6 V/V, while the transistor f_T increases by 25X, from 16 GHz to 400 GHz) [4] and to the reduced signal swing at sub-1V power supply voltage.

These drawbacks entirely offset the potential benefits of scaling in terms of reduced parasitics and negatively impact on area, performance, energy efficiency, and especially on design effort of analog cells in advanced technology nodes. In view of that, there has been almost no net power advantage [3] and no area reduction in analog cells like Operational Transconductance Amplifiers (OTAs) or bandgap references when moving from older to more recent technologies [5].

Last, but not least, analog ICs are characterized by a limited reconfigurability and portability across technology nodes compared to digital ICs, and require a significant time and effort in design, transistor-level optimization, simulation, full-custom layout, physical verification and prototyping [4], [6].

In view of these limitations, there has been a strong research interest towards the implementation of traditionally analog

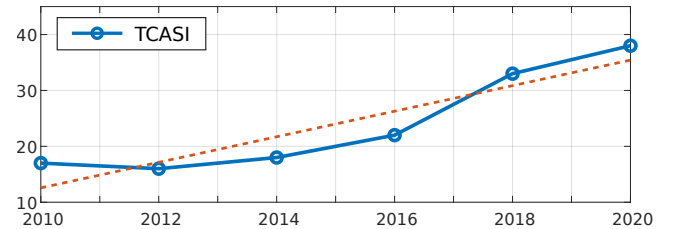


Fig. 1. Digital intensive analog/RF building block published in TCASI transactions over the last 10 years.

blocks by digital friendly and digital intensive replacements in the last years, which can be also observed in the number of CAS Transactions papers on related topics reported in Fig.1, which are more than doubled in the last decade.

Following this trend, fully digital phase-locked loops (PLLs) [7–9], synthesizable A/D converters (ADCs) based on successive approximation registers (SARs) [10–12] and on domino logic [13], stochastic flash ADCs [14], [15] and VCO-Based ADCs [16–23] have been proposed, extensively investigated and are increasingly employed in applications. Highly digital D/A converters (DACs) [24–28], voltage comparators [29–31], oscillators [32], low-dropout regulators (LDOs) [33–38], buck converters [39], [40], filters [41], [42], voltage references, [43–45], temperature sensors [46] and OTAs [47–52] have also been proposed. This trend can be noticed not only at block-level, but also at system-level, considering that mostly-digital RF transmitters [53–57], receivers [7], [58], [59], and biomedical front-ends [60], [61] have also been introduced.

While most of the above solutions address the challenges of analog interfaces by more “digital friendly” analog cells based on traditional design concepts [62], the possibility to implement analog functions with true digital circuits, which fully take advantage of scaling and of the benefits of a digital design flow, is also emerging as a promising alternative and will be specifically covered in this tutorial brief.

After a general background on information representation and processing in Section II, the implementation of the functions of OTAs, voltage references, and DACs will be covered in section III revealing that digital-based analog building blocks can take advantage of CMOS scaling with minimal design effort. Finally, the current design challenges in digital-based analog processing, new perspectives and application scenarios are discussed in Section IV, and some concluding remarks are drawn in Section V.

II. INFORMATION REPRESENTATION AND DESIGN FLOW

Despite the intrinsically analog and smooth perception of our surrounding environment, stated with Leibniz’s words

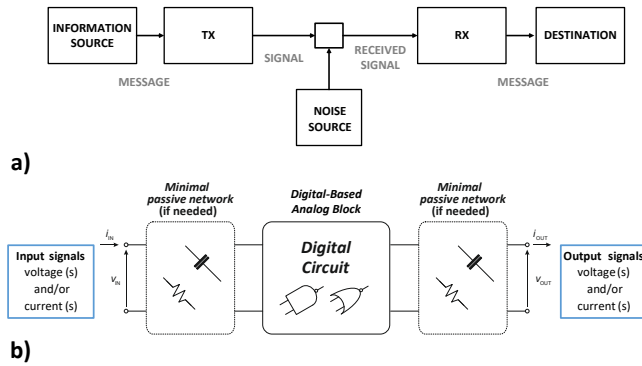


Fig. 2. a) Block diagram of a communication channel [64]. b) Block diagram of digital-based analog block.

as *"Natura non facit saltus"* (*"Nature does not jump"*), the achievements of science and technology in the last two centuries have extensively shown that, at an in-depth analysis, what appears to be continuous proves to be discrete in a variety of forms: matter is indeed composed by atoms, and all fundamental physical quantities from electric charge to electromagnetic field and angular momentum are also quantized.

Not only the inanimate world proves to be discrete, but also in animals and in humans information is processed and transmitted as discrete pulses, as discovered and modeled by Hodgkin and Huxley [63]. Then, we may conclude that our everyday life analog feeling is based on an underlying discrete structure.

Moreover, as shown by C.E.Shannon in his groundbreaking work [64], *information* is discrete in itself. In a channel with bandwidth B and background noise power N (Fig. 2a), which could be regarded, in wide sense, as a model of any information transmission and processing equipment, under a fixed signal power budget S , the maximum amount of information that can be reliably transferred in the unit time (expressed in bit/s) is finite and upper-bounded by the capacity $C = B \log_2(1 + S/N)$ of the channel [64], no matter if analog signals, whose value at each time instant is a real number and - as such - is expected to carry in theory an infinite amount of information, or digital signals are adopted.

In practice, the amount of information that can be transferred over the channel by analog means proves to be much less than the theoretical limit C , whereas, by digital encoding, the Shannon limit can be almost achieved [65]. The full awareness and understanding of this result and its application in information and communication systems have paved the way to the "digital revolution", which has been so profoundly impacting our lives and technology [66], [67].

Shannon's results, however, do not apply just to computers and communication networks. Actually, they also suit any kind of information, including information processed in sensors, actuators, interfaces, and analog circuits like OTAs and voltage references. This consideration suggests that even these circuits could take advantage of a better awareness of the discrete nature of information, and that digital circuits can possibly perform their functions.

Looking at Fig. 1, indeed, it is reasonable to state that a "digital revolution" in analog blocks is now happening, and it

can be clearly observed in two common threads, which can be noticed in recent publications.

The first, is the effort in moving information processing from the amplitude to the time domain [20], [21], [68–71], which has an intrinsic advantage in nanoscale CMOS where timing resolution, as opposed to amplitude resolution, is steadily increasing in more advanced nodes, due to the smaller delays of digital gates (the fan-out-of-4 (FO4) delay of an inverter has decreased by from 140ps (0.5 μ m) to 6ps (22nm node), i.e. by 23X [4]).

The second, is the effort aimed to extend digital automated design techniques to analog and RF systems. Although promising semi-automatic analog design techniques like procedure-based layout generation and optimization-based layout synthesis have been proposed in the last years [72], the synthesis-friendly analog circuits that use the existing digital flow tools for designing seem to be the most attractive ones.

These two threads, indeed, are closely related to each other - since analog circuits based on time-domain information processing are inherently more suitable to automated synthesis, and the functional/logical decomposition and abstraction required for automated design naturally lead to time-domain, algorithmic processing - and both converge towards the implementation of the functions of analog circuits by *true digital circuits*, as illustrated in Fig.2b, i.e. circuits in which information is internally processed in the form of two-level digital signals (i.e. *without* using digital gates as analog amplifying stages, as in [73]), possibly preceded and/or followed by minimal, non-critical, passive networks, that can grasp relevant information from any finite-amplitude, band-limited input signals (voltages and/or currents), and can generate the desired band-limited output voltages/currents at a pre-fixed degree of accuracy.

III. DIGITAL-BASED ANALOG BUILDING BLOCKS

In this section, the possibility to translate into digital the functions of fundamental analog building blocks like OTAs, voltage references and data converters following the paradigm in Fig.2b, which has been recently explored, will be reviewed with reference to four digital-based analog circuit topologies presented in the last years.

A. Digital-Based analog differential circuit

In [50], the possibility to translate into digital the operation of an MOS differential pair has been explored. In a traditional MOS differential pair [74], as shown in Fig. 3a, the Common-Mode (CM) signal is tracked by node V_S , and is subtracted from the external inputs in the gate-source voltages of the input devices, so that the control voltages of the input devices are CM-voltage independent and their drain currents are proportional to the differential mode input v_d [75]. In [50] it has been shown that a similar behavior can be obtained by using two digital buffers to sense the analog input signal (Differential-Mode (DM) *Amplifier* in Fig. 3b), and operating two three-state buffers according to their digital outputs $OUT = (OUT+, OUT-)$, which can take four values: 11, 00, 10, 01. Fig. 3c shows explicitly the relationship between each

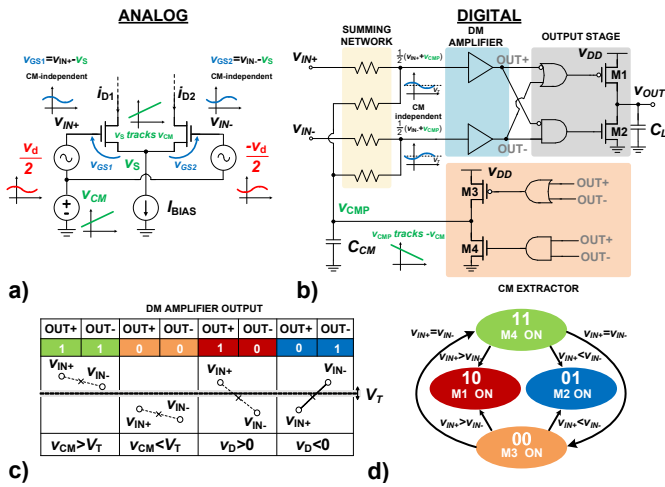


Fig. 3. a) Analog NMOS differential pair b) DIGOTA schematic proposed in [50] and its integrated version in [48], [49]. (c) Relationship between each state (OUT+,OUT-) and the voltage level of the inputs (v_{IN+}, v_{IN-}). (d) DIGOTA state transition diagram.

state and the voltage level of both inputs (v_{IN+}, v_{IN-}) referred to the buffer trip point (V_T).

Whenever OUT is 10, in fact, it can be concluded that $v_d > 0$ and similarly, OUT = 01 implies that $v_d < 0$ and the three-state output stage can be driven accordingly so that to charge or discharge the output capacitor. On the other hand, for OUT = 00 or OUT = 11, no information of the differential input can be obtained, but it can be concluded that the CM input is below or above the trip point of the buffers and this can be exploited to generate a compensation signal, to be added to the external inputs so that bring their CM component close to the buffer trip point, at which they are sensitive to the differential input.

This is indeed similar to what happens in the differential pair of Fig.3a in which V_S tracks the CM signal and removes it from the input signal through the *summing network* [50]. This digital CM cancellation generates an internal self-oscillation within the DIGOTA where all the logic gates works digitally decreasing considerably the total power consumption (no DC bias). Fig.3d reveals the state transition diagram of the DIGOTA in the function of the inputs, where the transition moments occur obeying the V_T -crossing events dictated by its intrinsic self-oscillation (no external clock is needed).

A proof-of-concept DIGOTA was first implemented by off-the-shelf components in [50] and simulations results for an integrated version of the same architecture were presented in [48], [49]. However, issues such as mismatch and intrinsic -6dB loss from the summing network limit the circuit robustness under Process-Voltage-Temperature (PVT) conditions requiring then static or dynamic calibration [76].

Recently, such issues have been substantially mitigated by replacing the passive summing network by Muller-C elements [47] revealing state of the art energy efficiency figures of merit $FOM_S = GBW \cdot C_L / \text{Power}$ and $FOM_L = SR \cdot C_L / \text{Power}$ for ultra low voltage applications. Even more interestingly, unlike in traditional OTAs, both FOM_S and FOM_L have been shown to increase in finer technology nodes [47], [48], as expected in view of the digital nature of the circuit.

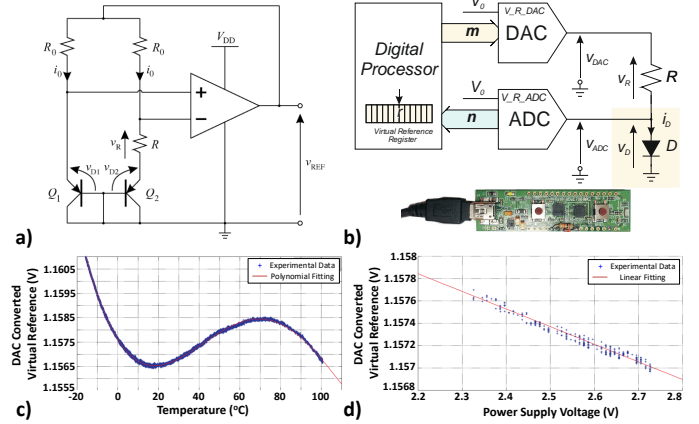


Fig. 4. a) Kujik's Bandgap voltage reference. b) Microcontroller-based proof of concept prototype c) V_{REF} vs. temperature d) V_{REF} vs. V_{DD} [43].

B. Virtual Voltage Reference Concept

Reference voltages and currents which are insensitive to PVT variations are essential building blocks in ICs and are often generated by bandgap references, like Kujik's circuit in Fig. 4a [77], taking advantage of the complementary-to-absolute-temperature (CTAT) thermal drift of a forward voltage v_D of a silicon *pn* junction biased at a constant current density and of the proportional-to-absolute-temperature (PTAT) drift of the voltage difference $\Delta v_D = v_{D1} - v_{D2}$ of two *pn* junctions biased at different current densities, so that to get a first-order temperature independent reference voltage

$$v_{REF} = v_D + \chi \Delta v_D \quad (1)$$

for an appropriate value of χ (equal to the ratio R_0/R_1 in the Kujik circuit in Fig. 4a).

Aiming to translate the above operation into digital, the virtual voltage reference concept has been introduced in [43], [78]. A virtual voltage reference is defined in a microprocessor (μP)-based system including a DAC and an ADC, both referenced to a possibly inaccurate and PVT dependent pseudo-reference V_0 , as shown Fig.4b. In this system, a virtual voltage reference is defined as the binary number r , which depends in general on PVT, that, if converted by the DAC referenced to the pseudo-reference V_0 , gives an output voltage V_{REF} which is PVT-independent within 1 LSB of the DAC resolution.

To get r , the behavior of a bandgap circuit can be translated into an algorithm to be run by the μP fed by the ADC acquisitions of a physical voltage. With reference to the digital platform in Fig.4b, in order to get a temperature independent V_{REF} , a diode, used as physical standard, is biased through a resistor R by the output voltage of the DAC. By converting two different values $m^{(1)}$ and $m^{(2)}$ into analog by the DAC, indeed, the diode is biased at two different current densities and its forward voltages are acquired and converted into the binary numbers $n^{(1)}$ and $n^{(2)}$ by the ADC referenced to V_0 , so that, neglecting quantization error, $n^{(i)} = v_D^{(i)} 2^N / V_0$ where $i \in \{1, 2\}$ and N is the DAC resolution.

As in Kujik circuit and in other bandgap references (including MOSFET-only references [79]) an appropriate weight χ^* ,

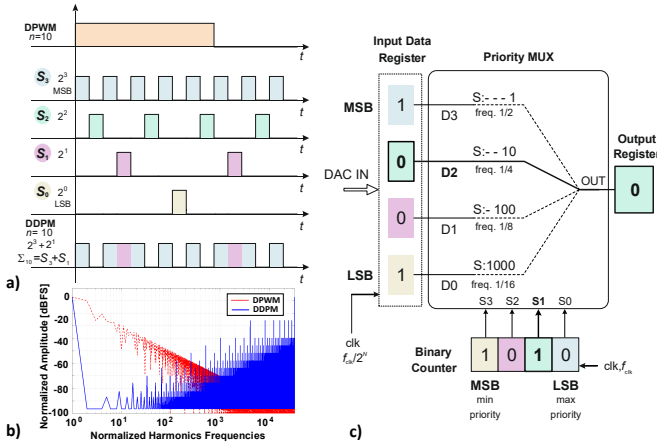


Fig. 5. a) DDPM and DPPM waveforms for $N = 4$ and $n = 10$ [24] b) DPWM vs. DDPM spectrum for a input word ($n = 29365$) and resolution ($N = 16$ bits) [76] c) Priority multiplexer hardware [24].

can be found to balance the CTAT behavior of $v_D^{(1)}$ and PTAT behavior of $v_D^{(2)} - v_D^{(1)}$ so that the voltage

$$v_{REF} = v_D^{(1)} + \frac{\chi^*}{\log h} (v_D^{(1)} - v_D^{(2)}) \quad (2)$$

where $h = \frac{m^{(1)} - n^{(1)}}{m^{(2)} - n^{(2)}}$, is first-order temperature independent. In a virtual voltage reference, however, v_{REF} is not obtained by summing physical voltages, but its definition in (2) is exploited to evaluate the virtual voltage reference r .

By expressing $v_D^{(1)}$ and $v_D^{(2)}$ in (2) in terms of the ADC acquisitions $n^{(1)}$ and $n^{(2)}$, in fact, one gets that (2) can be expressed as

$$v_{REF} = \left[n^{(1)} + \chi \frac{\log h^*}{\log h} (n^{(1)} - n^{(2)}) \right] \frac{V_0}{2^N} = \frac{V_0}{2^N} r \quad (3)$$

where the quantity in the square brackets, which can be calculated algorithmically inside the digital processor, can be immediately identified as the virtual voltage reference and can be possibly converted into analog by the DAC in Fig.4b. An effective temperature coefficient $TC_{eff} = 18 \text{ ppm}/^\circ\text{C}$, Fig. 4c, and line sensitivity $LS = 0.15\%/V$, Fig. 4d, have been achieved by this approach in a microcontroller-based proof of concept prototype.

Since processing is moved to the digital domain in a virtual reference circuit, this approach is well suited to implement complex, high order temperature-compensation strategies, which would not be suitable to an analog implementation, and it has been adopted indeed in a precision virtual voltage reference which achieves a measured $TC_{eff} = 5 \text{ ppm}/^\circ\text{C}$ [78]. Two years after, a circuit based on a similar approach has been implemented on silicon [44] achieving a $TC_{eff} = 18 \text{ ppm}/^\circ\text{C}$ which is fully in line with the results obtained by the microcontroller based prototype.

C. Highly Digital DAC

Bitstream D/A conversion is a key enabling concept for digital-based analog processing, since it can be directly adopted in digital-based analog blocks in Fig.2b to implement analog outputs and also analog inputs, when used in a feedback configuration with a gate-based comparator [11].

In this framework, Digital Pulse-Width Modulation (DPWM) [80], [81] and single-bit sigma-delta ($\Sigma\Delta$) [82], [83] are well known bitstream D/A conversion techniques: single-bit $\Sigma\Delta$ is suitable to achieve high resolution thanks to noise shaping, but it is not well suited to DC conversion, it requires rather complex digital hardware and careful design is needed to avoid stability issues and idle tones. Digital PWM, by contrast, requires very simple digital HW and does not suffer of stability issues, but it poses stringent requirements on the output filter, since most of the spurious spectral content of DPWM signals is close to the baseband. In view of these limitations, two new D/A conversion techniques, the Dyadic Digital Pulse Modulation (DDPM) and Relaxation Digital to Analog Converter (ReDAC) have been recently proposed to address the demand for ultra low-cost and energy efficient D/A conversion in digital-based analog interfaces for the IoT.

1) *Dyadic Digital Pulse Modulation*: The DDPM modulation proposed in [24] associates to a digital input code n on N bits, expressed in terms of its binary representation $B_n[N-1:0] = (b_{N-1}, b_{N-2}, \dots, b_1, b_0)$ as $n = \sum_{i=0}^{N-1} b_i 2^i$, the periodic bitstream

$$\Sigma_n(t) = \sum_{i=0}^{N-1} b_i S_i(t) \quad (4)$$

obtained by superposition of orthogonal dyadic basis signals (ODBSs) $S_i(t)$ ($i = 0, \dots, N-1$) shown in Fig.5a for $N=4$, which are non-overlapping, periodically repeated digital streams of 2^N clock cycles, organized so that S_{N-1} is high (i.e. at V_{DD}) every other clock cycle (i.e., in 2^{N-1} cycles per period), S_{N-2} is high every other cycle in which S_{N-1} is low (i.e., in 2^{N-2} cycles), S_{N-3} is high every other cycle in which both S_{N-1} and S_{N-2} are low (i.e., in 2^{N-3} cycles per period) and so on, till S_0 , which is high just in one cycle per period, as shown in Fig.5a. Being ODBSs S_i non-overlapping and high in 2^i clock cycles per period, DDPM streams Σ_n defined in (4) are high for exactly n clock cycles per period and their time average is therefore $n/2^N V_{DD}$, as observed in the same Fig.5a, where the construction of a DDPM stream by superposition of ODBSs is illustrated for $n = 10$.

In practice, DDPM streams can be generated by a priority multiplexer [24], i.e. a tiny digital hardware as in DPWM, but they show much more favorable spectral features compared to DPWM as shown in Fig.5b. This is due to the fact that ODBS related to the i -th MSB are by construction periodic with a frequency 2^{N-i} times higher than the fundamental. Other than in baseband D/A and A/D conversion [11], [24], [27], the favorable spectral properties of DDPM have also been exploited in band-pass D/A conversion [54] and in digitally controlled switching mode power converters [84] to avoid the onset of limit cycle oscillations.

2) *Relaxation DAC*: A Relaxation DAC [85], whose principle schematic is shown in Fig.6a exploits the time response of a first-order RC network driven by the bitstream corresponding to the digital input code (LSB-first) by a shift register operated at clock cycle T , to perform D/A conversion. After the conversion of the MSB of the input code is completed, the

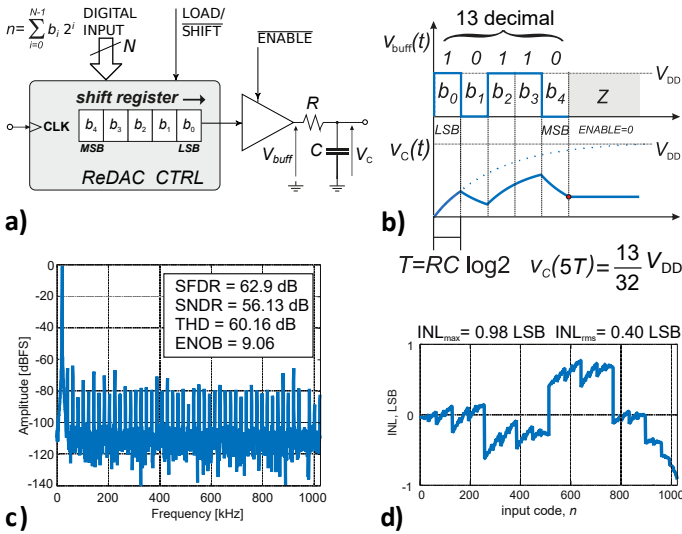


Fig. 6. a) ReDAC converter [85] b) ReDAC conversion waveforms example [85] c) Self-calibrated ReDAC dynamic performance at 20kHz, 90% swing [26]. d) Self-calibrated ReDAC INL

voltage across the capacitor of the RC network, which is in general expressed by first-order linear transient analysis as:

$$v_c(NT) = V_{DD} \left(1 - e^{-\frac{T}{\tau}}\right) \cdot \sum_{i=0}^{N-1} b_i e^{-\frac{(N-i)T}{\tau}} \quad (5)$$

becomes just

$$v_c(NT) = \frac{V_{DD}}{2^N} \sum_{i=0}^{N-1} b_i 2^i \quad (6)$$

provided that the relation $T = \tau \log 2$ between the clock period T and time constant $\tau = RC$ is satisfied. Fig. 6b shows the ReDAC conversion waveform example for $N = 5$ and $n = 13$.

The condition $T = \tau \log 2$, can be imposed by tuning the clock period so that to enforce the equality of the ReDAC output voltages corresponding to $2^{N-1} - 1$ and 2^{N-1} inputs at a conveniently high resolution, since the maximum INL error always appears between these two codes and it is found to be proportional to the relative timing error ($INL_{\max} \approx 2^{N-1} \log 2 \cdot \frac{\Delta T}{T}$, where $\Delta T = T - \tau \log 2$). A 2MS/s, 10bit ReDAC featuring digital background self-calibration achieves less than 1LSB of INL_{\max} and DNL_{\max} and 9.06 ENOB (Fig. 6c,d) [85].

With respect to switched-capacitor DACs, a ReDAC is matching-insensitive and its operation relies on a single parameter to be calibrated. As a consequence the ReDAC capacitance can be chosen close to the thermal noise limit, thus enabling ultra-low energy per conversion of 0.73pJ/conv at 2MS/s, as demonstrated in post-layout simulations [86] performed in 40nm CMOS technology of a 10bit ReDAC occupying an area of $910\mu\text{m}^2$. These features make the ReDAC concept very well suited to IoT applications.

IV. CHALLENGES AND FUTURE OPPORTUNITIES

The feasibility of all-digital and mostly digital implementations of analog interfaces has been conceptually proven and demonstrated on silicon over the last decade, revealing significant advantages in terms of area and power compared to more traditional approaches, as show in Fig. 7 for ADC [24],

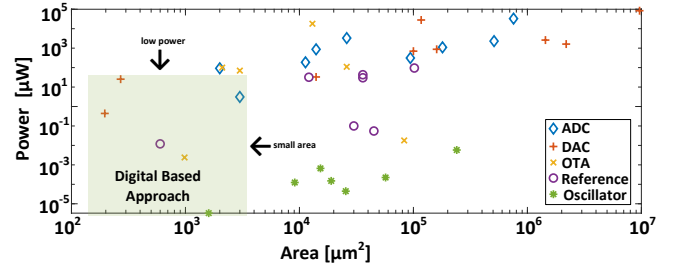


Fig. 7. Power vs Area for for ADCs [24], DACs [27], OTAs [47], voltage reference [43] and oscillators [32].

DAC [27], OTA [47], voltage reference [43] and oscillator [32]. Such solutions are now mature enough to address the requirements of a number of applications in the IoT field, and have been already adopted in fact in systems like frequency synthesizers [8], [9], biomedical signal acquisition front-ends [60], [87] and smart sensors [46], [88–90], achieving relevant performance. Their potential in applications, however, is far from being fully exploited and it could be expected that, in a foreseeable future, general-purpose, fully synthesizable and re-configurable digital architectures with direct sensing and actuator driving features can be developed to target an increasing number of applications.

At the same time, it should be observed in most of the cases the performance of digital-based implementations of analog interfaces is not yet competitive with the best traditional analog implementations in the state of the art (e.g., digital-based OTAs show lower DC gain and common-mode rejection, standalone DDPM DAC and ReDAC bandwidth and effective resolution should be enhanced, just rather elementary virtual references have been demonstrated so far). This is reasonable considering that most of such techniques have been proposed only in the last ten years and are still in their childhood, whereas traditional analog ones have been constantly refined and improved over the last 60 years. By the way, considerations on the discrete nature of information lead to conclude that there is no fundamental limit in digital-based analog processing compared to traditional analog approaches.

Since digital-based analog circuits process the signal in time-domain and time resolution improves as technology scale, any improvement in digital technology makes it reasonable to expect that the performance gap with traditional analog implementations can be rapidly filled in the next few years.

V. CONCLUSION

The current trend in CMOS digital-based analog circuit design over the last decade and its foundations have been reviewed in this tutorial brief, with a special emphasis on the implementation of analog functions by fully digital circuits. Under this perspective, digital-based OTAs, virtual voltage references and bitstream DDPM and Relaxation DACs proposed in the last years, have been reviewed, highlighting their suitability to emerging IoT applications. The current challenges of digital-based analog processing and their potential application scenarios have been finally considered and future perspectives have been discussed.

REFERENCES

- [1] S. Oh et al., "Dual-slope capacitance to digital converter integrated in an implantable pressure sensing system," in *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, 2014, pp. 295–298.
- [2] M. Alioto, *Enabling the Internet of Things – from Integrated Circuits to Integrated Systems*, 1st ed. Springer, 2017.
- [3] P. R. Kinget, "Scaling analog circuits into deep nanoscale CMOS: Obstacles and ways to overcome them," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015, pp. 1–8.
- [4] B. Xu, S. Li, N. Sun, and D. Z. Pan, "A scaling compatible, synthesis friendly VCO-based delta-sigma ADC design and synthesis methodology," in *2017 54th ACM/EDAC/IEEE Design Automation Conference (DAC)*, 2017, pp. 1–6.
- [5] O. Aiello, P. Crovetto, and M. Alioto, "Ultra-low power and minimal design effort interfaces for the internet of things: Invited paper," in *2019 IEEE International Circuits and Systems Symposium (ICSys)*, 2019, pp. 1–4.
- [6] P. S. Crovetto, F. Musolino, O. Aiello, P. Toledo, and R. Rubino, "breaking the boundaries between analogue and digital," *Electronics Letters*, vol. 55, no. 12, pp. 672–673, 2019.
- [7] R. B. Staszewski et al., "All-digital TX frequency synthesizer and discrete-time receiver for bluetooth radio in 130-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, 2004.
- [8] Y. Park and D. D. Wentzloff, "An all-digital PLL synthesized from a digital standard cell library in 65nm CMOS," in *2011 IEEE Custom Integrated Circuits Conference (CICC)*, 2011, pp. 1–4.
- [9] W. Deng et al., "A fully synthesizable all-digital pll with interpolative phase coupled oscillator, current-output DAC, and fine-resolution digital varactor using gated edge injection technique," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 1, pp. 68–80, 2015.
- [10] M. Seo et al., "A reusable code-based SAR ADC design with CDAC compiler and synthesizable analog building blocks," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 12, pp. 1904–1908, 2018.
- [11] O. Aiello, P. Crovetto, and M. Alioto, "Fully synthesizable low-area analogue-to-digital converters with minimal design effort based on the dyadic digital pulse modulation," *IEEE Access*, vol. 8, pp. 70890–70899, 2020.
- [12] J. Park, Y. Hwang, and D. Jeong, "A 0.5V fully synthesizable SAR ADC for on-chip distributed waveform monitors," *IEEE Access*, vol. 7, pp. 63686–63697, 2019.
- [13] S. Weaver, B. Hershberg, N. Maghari, and U. Moon, "Domino-logic-based ADC for digital synthesis," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 11, pp. 744–747, 2011.
- [14] S. Weaver, B. Hershberg, and U. Moon, "Digitally synthesized stochastic flash adc using only standard digital cells," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 1, pp. 84–91, 2014.
- [15] A. Fahmy, J. Liu, T. Kim, and N. Maghari, "An all-digital scalable and reconfigurable wide-input range stochastic ADC using only standard cells," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 8, pp. 731–735, 2015.
- [16] A. Waters and U. Moon, "A fully automated verilog-to-layout synthesized ADC demonstrating 56dB-SNR with 2MHz-BW," in *2015 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2015, pp. 1–4.
- [17] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time $\Sigma\Delta$ ADC with a 5-bit, 950 – MS/s VCO-based quantizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, 2008.
- [18] G. Taylor and I. Galton, "A mostly-digital variable-rate continuous-time delta-sigma modulator ADC," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2634–2646, 2010.
- [19] V. Nguyen, F. Schembari, and R. B. Staszewski, "A 0.2-V 30-MS/s 11b-ENOB open-loop VCO-based ADC in 28-nm CMOS," *IEEE Solid-State Circuits Letters*, vol. 1, no. 9, pp. 190–193, 2018.
- [20] G. G. E. Gielen, L. Hernandez, and P. Rombouts, "Time-encoding analog-to-digital converters: Bridging the analog gap to advanced digital cmos-part 1: Basic principles," *IEEE Solid-State Circuits Magazine*, vol. 12, no. 2, pp. 47–55, 2020.
- [21] —, "Time-encoding analog-to-digital converters: Bridging the analog gap to advanced digital cmos-part 2: Architectures and circuits," *IEEE Solid-State Circuits Magazine*, vol. 12, no. 3, pp. 18–27, 2020.
- [22] V. Unnikrishnan and M. Vesterbacka, "Time-mode analog-to-digital conversion using standard cells," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 12, pp. 3348–3357, 2014.
- [23] A. Jayaraj, M. Danesh, S. Tannirkulam Chandrasekaran, and A. Sanyal, "76-dB-DR, 48fJ/Step second-order VCO-based current-to-digital converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 4, pp. 1149–1157, 2020.
- [24] P. S. Crovetto, "All-digital high resolution d/a conversion by dyadic digital pulse modulation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 573–584, 2017.
- [25] E. Ansari and D. D. Wentzloff, "A 5mW 250MS/s 12-bit synthesized digital to analog converter," in *Proceedings of the IEEE 2014 Custom Integrated Circuits Conference*, 2014, pp. 1–4.
- [26] P. S. Crovetto, R. Rubino, and F. Musolino, "Relaxation digital-to-analog converter with foreground digital self-calibration," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–5.
- [27] O. Aiello, P. Crovetto, and M. Alioto, "Standard cell-based ultra-compact daacs in 40-nm cmos," *IEEE Access*, vol. 7, pp. 126479–126488, 2019.
- [28] O. Aiello, P. S. Crovetto, and M. Alioto, "Fully synthesizable low-area digital-to-analog converter with graceful degradation and dynamic power-resolution scaling," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 8, pp. 2865–2875, 2019.
- [29] O. Aiello, P. Crovetto, and M. Alioto, "Fully synthesizable, rail-to-rail dynamic voltage comparator for operation down to 0.3 V," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1–5.
- [30] X. Zou and S. Nakatake, "A fully synthesizable, 0.3V, 10nW rail-to-rail dynamic voltage comparator," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2020, pp. 199–202.
- [31] X. Li, T. Zhou, Y. Ji, and Y. li, "A 0.35 V-to-1.0 V synthesizable rail-to-rail dynamic voltage comparator based OAI&AOI logic," *Analog Integrated Circuits and Signal Processing volume*, vol. 104, p. 351–357, 2020.
- [32] O. Aiello, P. Crovetto, L. Lin, and M. Alioto, "A pw-power hz-range oscillator operating with a 0.3–1.8-V unregulated supply," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1487–1496, 2019.
- [33] Yasuyuki Okuma et al., "0.5-v input digital ldo with 98.7% current efficiency and 2.7- μ a quiescent current in 65nm cmos," in *IEEE Custom Integrated Circuits Conference 2010*, 2010, pp. 1–4.
- [34] S. Bang et al., "25.1 a fully synthesizable distributed and scalable all-digital ldo in 10nm cmos," in *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2020, pp. 380–382.
- [35] G. Cai, C. Zhan, and Y. Lu, "A fast-transient-response fully-integrated digital ldo with adaptive current step size control," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 9, pp. 3610–3619, 2019.
- [36] J. Tang, C. Zhan, G. Wang, and Y. Liu, "A 0.7V fully-on-chip pseudo-digital LDO regulator with 6.3 μ A quiescent current and 100mV dropout voltage in 0.18 – μ m cmos," in *ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, 2018, pp. 206–209.
- [37] Y. Lu, F. Yang, F. Chen, and P. K. T. Mok, "A distributed power delivery rail based on analog-assisted digital LDOs with cooperative regulation and IR-drop reduction," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 8, pp. 2859–2871, 2020.
- [38] L. Qian et al., "A fast-transient response digital low-dropout regulator with dual-modes tuning technique," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 2943–2947, 2020.
- [39] S. J. Kim et al., "A 4-phase 30–70MHz switching frequency buck converter using a time-based compensator," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2814–2824, 2015.
- [40] V. C. Krishna Chekuri et al., "A fully synthesized integrated buck regulator with auto-generated gds-ii in 65nm cmos process," in *2020 IEEE Custom Integrated Circuits Conference (CICC)*, 2020, pp. 1–4.
- [41] B. Drost, M. Talegaonkar, and P. K. Hanumolu, "A 0.55V 61dB – SNR 67dB – SFDR 7MHz 4th-order butterworth filter using ring-oscillator-based integrators in 90nm cmos," in *2012 IEEE International Solid-State Circuits Conference*, 2012, pp. 360–362.
- [42] J. Liu, B. Park, M. Guzman, A. Fahmy, T. Kim, and N. Maghari, "A fully synthesized 77-dB sfdr reprogrammable srmc filter using digital standard cells," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 6, pp. 1126–1138, 2018.
- [43] P. S. Crovetto, "A digital-based virtual voltage reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 5, pp. 1315–1324, 2015.
- [44] Z. Cai, et al., "A cmos readout circuit for resistive transducers based on algorithmic resistance and power measurement," *IEEE Sensors Journal*, vol. 17, no. 23, pp. 7917–7927, 2017.

- [45] M. Eberlein, H. Pretl, and Z. Georgiev, "Time-controlled and FinFET compatible sub-bandgap references using bulk-diodes," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 10, pp. 1608–1612, 2019.
- [46] A. Tejasvi, K. Makinwa, and P. Hanumolu, "A vco based highly digital temperature sensor with 0.034°C/mV supply sensitivity," *IEEE Solid-State Circuits Journal*, vol. 11, no. 7, pp. 2651 – 2663, 2016.
- [47] P. Toledo, P. Crovetto, O. Aiello, and M. Alioto, "Fully-digital rail-to-rail ota with sub-1,000 μm^2 area, 250-mv minimum supply and nw power at 150-pf load in 180nm," *IEEE Solid-State Circuits Letters*, pp. 1–1, 2020.
- [48] P. Toledo, P. Crovetto, H. Klimach, and S. Bampi, "A 300mv-supply, 2nw-power, 80pf-load cmos digital-based ota for iot interfaces," in *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2019, pp. 170–173.
- [49] P. Toledo, O. Aiello, and P. S. Crovetto, "A 300mv-supply standard-cell-based ota with digital pwm offset calibration," in *2019 IEEE Nordic Circuits and Systems Conference (NORCHIP and International Symposium of System-on-Chip (SoC))*, 2019, pp. 1–5.
- [50] P. S. Crovetto, "A digital-based analog differential circuit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 12, pp. 3107–3116, 2013.
- [51] S. Kalani and P. R. Kinget, "Zero-crossing-time-difference model for stability analysis of vco-based otas," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 3, pp. 839–851, 2020.
- [52] S. Kalani, A. Bertolini, A. Ricchelli, and P. R. Kinget, "A 0.2v 492nw VCO-based OTA with 60khz UGB and 207 μVrms noise," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, pp. 1–4.
- [53] Y. Park and D. D. Wentzloff, "An all-digital 12pJ/Pulse ir-uwv transmitter synthesized from a standard cell library," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1147–1157, 2011.
- [54] P. S. Crovetto, "Spectral characteristics of ddpn streams and their application to all-digital amplitude modulation," *Electronics Letters*, vol. 62, no. 3, 2020.
- [55] T. Buckel *et al.*, "A novel digital-intensive hybrid polar-I/Q RF transmitter architecture," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 12, pp. 4390–4403, 2018.
- [56] K. Un *et al.*, "Design considerations of the interpolative digital transmitter for quantization noise and replicas rejection," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 1, pp. 37–41, 2020.
- [57] F. T. Gebreyohannes, A. Frappé, P. Cathelin, A. Cathelin, and A. Kaiser, "All-digital transmitter architecture based on two-path parallel 1-bit high pass filtering DACs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3956–3969, 2018.
- [58] F. Opteynde, "A maximally-digital radio receiver front-end," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2010, pp. 450–451.
- [59] F. Kuo *et al.*, "A bluetooth low-energy transceiver with 3.7-mW all-digital transmitter, 2.75-mW high-if discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1144–1162, 2017.
- [60] J. Huang *et al.*, "A 0.01-mm² mostly digital capacitor-less afe for distributed autonomous neural sensor nodes," *IEEE Solid-State Circuits Letters*, vol. 1, no. 7, pp. 162–165, 2018.
- [61] P. S. Crovetto, "Acquisition front-end immune to emi," *Electronics Letters*, vol. 48, no. 18, pp. 1114–1115, 2012.
- [62] B. Murmann, "Digitally assisted analog circuits; fifth ieee dallas circuits and systems workshop," in *2006 IEEE Dallas/CAS Workshop on Design, Applications, Integration and Software*, 2006, pp. 23–30.
- [63] A. L. Hodgkin and A. F. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," *The Journal of physiology*, vol. 117, no. 4, pp. 500–544, Aug 1952, 12991237[pmid]. [Online]. Available: <https://pubmed.ncbi.nlm.nih.gov/12991237/>
- [64] C. E. Shannon, "A mathematical theory of communication," *The Bell System Technical Journal*, vol. 27, no. 3, pp. 379–423, 1948.
- [65] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near shannon limit error-correcting coding and decoding: Turbo-codes. 1," in *Proceedings of ICC '93 - IEEE International Conference on Communications*, vol. 2, 1993, pp. 1064–1070 vol.2.
- [66] I. Bojanova, "The digital revolution: What's on the horizon?" *IT Professional*, vol. 16, no. 1, pp. 8–12, 2014.
- [67] J. Bryzek, "Impact of mems technology on society," *Sensors and Actuators A: Physical*, vol. 56, no. 1, pp. 1 – 9, 1996. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/0924424796012848>
- [68] F. Yuan and P. Parekh, "Analysis and design of an all-digital $\delta\sigma$ TDC via time-mode signal processing," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 6, pp. 994–998, 2020.
- [69] E. Rahiminejad *et al.*, "A low-voltage high-precision time-domain winner-take-all circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 1, pp. 4–8, 2020.
- [70] D. Kim, K. Kim, W. Yu, and S. Cho, "A second-order $\Delta\Sigma$ time-to-digital converter using highly digital time-domain arithmetic circuits," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 10, pp. 1643–1647, 2019.
- [71] A. Ricchelli, L. Colalongo, and Z. M. Kovács-Vajna, "EMI effect in voltage-to-time converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, pp. 1–1, 2020.
- [72] H. Chen, M. Liu, X. Tang, K. Zhu, N. Sun, and D. Pan, "Challenges and opportunities toward fully automated analog layout design," *Journal of Semiconductors*, 2020.
- [73] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, 1992.
- [74] P. R. Gray and R. G. Meyer, "MOS operational amplifier design-a tutorial overview," *IEEE Journal of Solid-State Circuits*, vol. 17, no. 6, pp. 969–982, 1982.
- [75] P. Toledo *et al.*, "CMOS transconductor analysis for low temperature sensitivity based on ZTC MOSFET condition," in *2015 28th Symposium on Integrated Circuits and Systems Design (SBCCI)*, 2015, pp. 1–7.
- [76] P. Toledo, P. Crovetto, H. klimach, and S. Bampi, "Dynamic and static calibration of ultra-low-voltage, digital-based operational transconductance amplifiers," *Electronics*, 2020.
- [77] K. E. Kuijk, "A precision reference voltage source," *IEEE Journal of Solid-State Circuits*, vol. 8, no. 3, pp. 222–226, 1973.
- [78] P. S. Crovetto, "Very low thermal drift precision virtual voltage reference," *Electronics Letters*, vol. 51, no. 14, pp. 1063–1065, 2015.
- [79] P. Toledo, D. Cordova, H. Klimach, S. Bampi, and P. S. Crovetto, "A 0.3–1.2 V schottky-based cmos ztc voltage reference," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 10, pp. 1663–1667, 2019.
- [80] M. De Martino *et al.*, "A standard-cell-based all-digital PWM modulator with high resolution and spread-spectrum capability," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3885–3896, 2018.
- [81] X. Cheng *et al.*, "A high resolution DPWM based on synchronous phase-shifted circuit and delay line," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 8, pp. 2685–2692, 2020.
- [82] J. M. de la Rosa, "Sigma-delta modulators: Tutorial overview, design guide, and state-of-the-art survey," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 1–21, 2011.
- [83] M. Honarparvar, J. M. de la Rosa, and M. Sawan, "A 0.9-v 100- μ w feedforward adder-less inverter-based MASH $\Delta\Sigma$ modulator with 91-dB dynamic range and 20-kHz bandwidth," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3675–3687, 2018.
- [84] P. S. Crovetto, M. Usmonov, F. Musolino, and F. Gregoretti, "Limit-cycle-free digitally controlled DC–DC converters based on dyadic digital PWM," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 11 155–11 166, 2020.
- [85] P. S. Crovetto, R. Rubino, and F. Musolino, "Relaxation digital-to-analogue converter," *Electronics Letters*, vol. 55, no. 12, pp. 685–688, 2019.
- [86] R. Rubino, P. S. Crovetto, and O. Aiello, "Design of relaxation digital-to-analog converters for internet of things applications in 40nm CMOS," in *2019 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2019, pp. 13–16.
- [87] R. Mohan *et al.*, "A 0.6-V, 0.015-mm², time-based ECG readout for ambulatory applications in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 1, pp. 298–308, 2017.
- [88] K. Niitsu *et al.*, "A self-powered supply-sensing biosensor platform using bio fuel cell and low-voltage, low-cost CMOS supply-controlled ring oscillator with inductive-coupling transmitter for healthcare iot," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 9, pp. 2784–2796, 2018.
- [89] O. Olabode *et al.*, "Time-based sensor interface for dopamine detection," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 10, pp. 3284–3296, 2020.
- [90] C. Ku and T. Liu, "A voltage-scalable low-power all-digital temperature sensor for on-chip thermal monitoring," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 10, pp. 1658–1662, 2019.